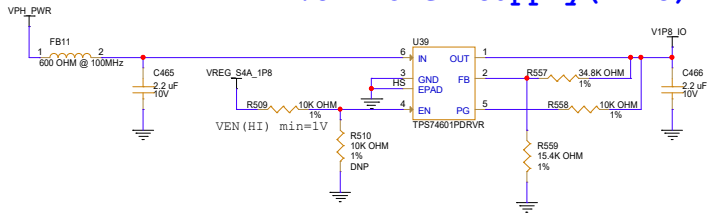


DSI to Dual LVDS

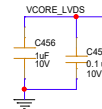
1.8V Power Supply (LVDS)



DESIGN NOTE
LVDS Controller bypass option

1	MIP1_DSIO_LANE0_P	R489	DNP	0 OHM	LVD0_A_LANE0_P	1.2,3
1	MIP1_DSIO_LANE0_N	R490	DNP	0 OHM	LVD0_A_LANE0_N	1.2,3
1	MIP1_DSIO_LANE1_P	R491	DNP	0 OHM	LVD0_A_LANE1_P	1.2,3
1	MIP1_DSIO_LANE1_N	R492	DNP	0 OHM	LVD0_A_LANE1_N	1.2,3
1	MIP1_DSIO_LANE2_P	R493	DNP	0 OHM	LVD0_A_LANE2_P	1.2,3
1	MIP1_DSIO_LANE2_N	R494	DNP	0 OHM	LVD0_A_LANE2_N	1.2,3
1	MIP1_DSIO_LANE3_P	R495	DNP	0 OHM	LVD0_A_LANE3_P	1.2,3
1	MIP1_DSIO_LANE3_N	R496	DNP	0 OHM	LVD0_A_LANE3_N	1.2,3
1	MIP1_DSIO_CLK_P	R497	DNP	0 OHM	LVD0_A_CLK_P	1.2,3
1	MIP1_DSIO_CLK_N	R498	DNP	0 OHM	LVD0_A_CLK_N	1.2,3

SMARC LVDS PORT-A (AS DSI)



DESIGN NOTE
VCORE power supply pin must have a 100-nF capacitor to ground connected as close as possible to the SN65DSI84 device. It is recommended to have one bulk capacitor (1 μ F to 10 μ F) on it.

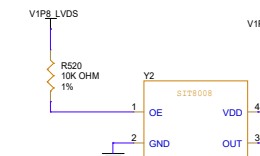
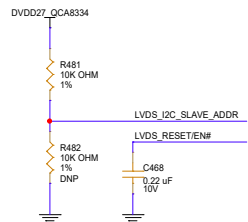
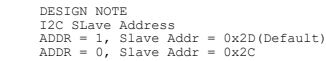
1	MPLI_DSIO_LANE0_P	R589	0 OHM	SN6DS0184	DA0_P	H3	DA0P
1	MPLI_DSIO_LANE0_N	R590	0 OHM	SN6DS0184	DA0_N	J3	DA0N
1	MPLI_DSIO_LANE1_P	R595	0 OHM	SN6DS0184	DA1_P	H4	DA1P
1	MPLI_DSIO_LANE1_N	R591	0 OHM	SN6DS0184	DA1_N	J4	DA1N
1	MPLI_DSIO_LANE2_P	R592	0 OHM	SN6DS0184	DA2_P	H6	DA2P
1	MPLI_DSIO_LANE2_N	R593	0 OHM	SN6DS0184	DA2_N	J6	DA2N
1	MPLI_DSIO_LANE3_P	R596	0 OHM	SN6DS0184	DA3_P	H7	DA3P
1	MPLI_DSIO_LANE3_N	R594	0 OHM	SN6DS0184	DA3_N	J7	DA3N
1	MPLI_DSIO_CLK_P	R597	0 OHM	SN6DS0184	DAC_P	H5	DACP
1	MPLI_DSIO_CLK_N	R598	0 OHM	SN6DS0184	DAC_N	J5	DACN

A_Y0N	C9	»»	LVDS_A_LANE0_N	1,2,3
A_Y0P	C8			
A_Y1N	D9	»»	LVDS_A_LANE1_N	1,2,3
A_Y1P	D8			
A_Y2N	E9	»»	LVDS_A_LANE2_N	1,2,3
A_Y2P	E8			
A_CLKN	F9	»»	LVDS_A_CLK_N	1,2,3
A_CLKP	F8			
A_Y3N	G9	»»	LVDS_A_LANE3_N	1,2,3
	G8			

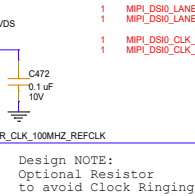
SMARC LVDS PORT-A

B_Y0N	A3		>>	LVD5_B_LANE0_N	2,3
B_Y0P	B3		>>	LVD5_B_LANE0_P	2,3
B_Y1N	A4		>>	LVD5_B_LANE1_N	2,3
B_Y1P	B4		>>	LVD5_B_LANE1_P	2,3
B_Y2N	A5		>>	LVD5_B_LANE2_N	2,3
B_Y2P	B5		>>	LVD5_B_LANE2_P	2,3
B_CLKP	B6		>>	LVD5_B_CLK_P	3
B_CLKN	A6		>>	LVD5_B_CLK_N	3
B_Y3N	A7		>>	LVD5_B_LANE3_N	2,3
	B7		>>	LVD5_B_LANE3_P	2,3

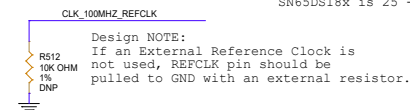
SMARC LVDS PORT-A



Design NOTE: 100MHZ
The LVDS CLK freq range for the
SN65DSI8x is 25 - 154 MHz

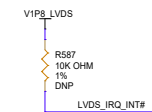
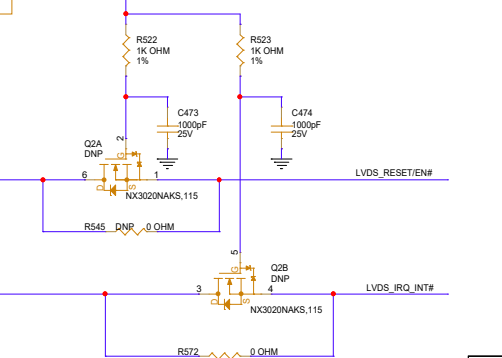
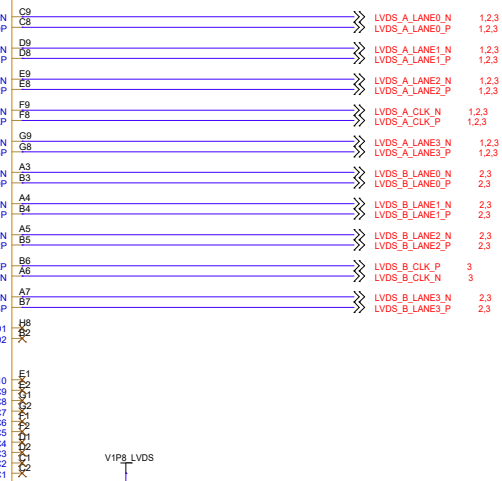
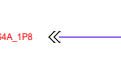
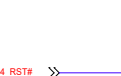
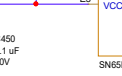
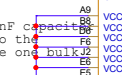
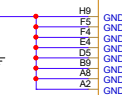
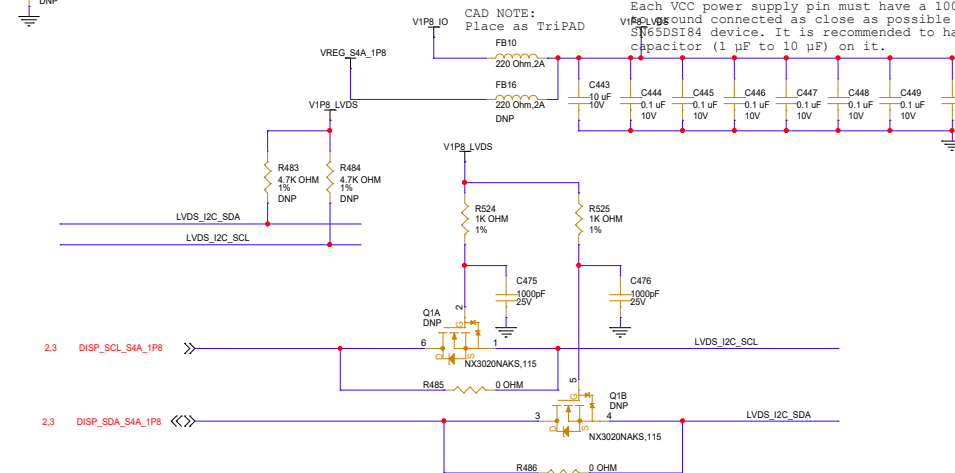


Design NOTE:
Optional Resistor
to avoid Clock Ringing

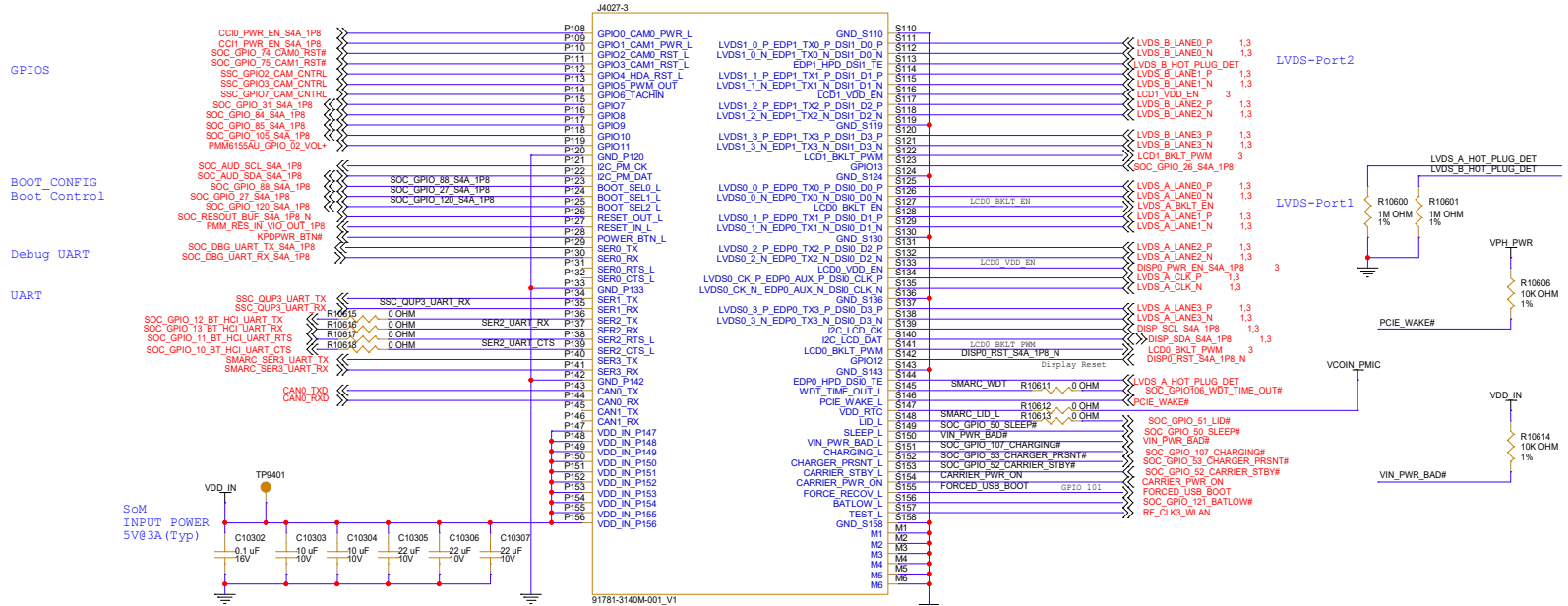


DESIGN NOTE

Each VCC power supply pin must have a 100-nF capacitor connected as close as possible to the SN6DSI84 device. It is recommended to have one bulk J2 capacitor (1 μF to 10 μF) on it.



SoM Interface-2

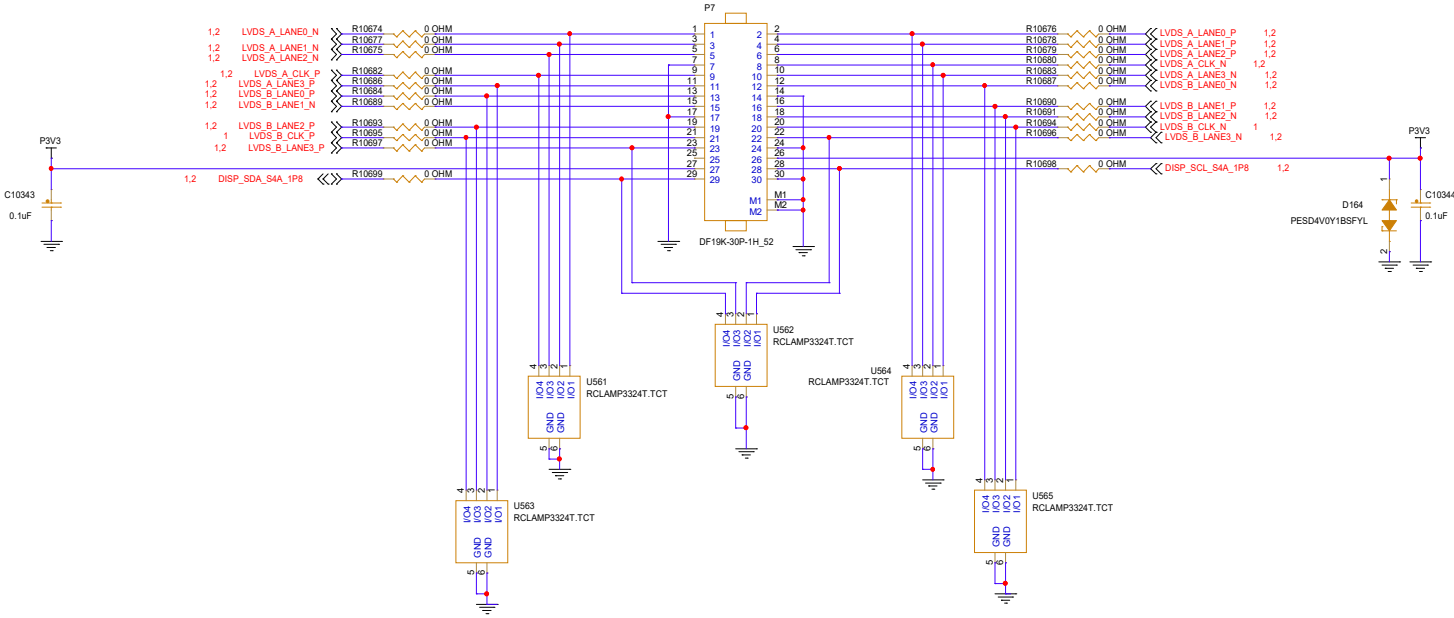


LVDS CONNECTOR 1

Module	13.3"FHD Color TFT-LCD with backlight driver
Manufacturer PN	G133HAN01.0
Manufacturer	FORTEC

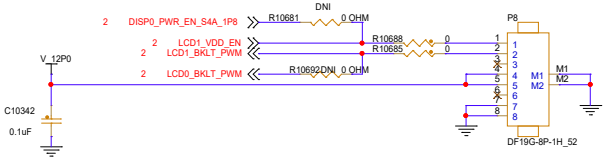
LCD MODULE CONNECTOR(DUAL LVDS)

Pinout is based on the following Display panel
<https://www.fortec-integrated.de/en/products/tft-components/tft-displays/detail/auo/g133han011/>



LED DRIVER CONNECTOR

NEED 12V



Title			
ITERA_Gateway_Application_Board			
Size	Document Number	Rev	
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Date:	Monday, February 03, 2025	Sheet	3 of 3