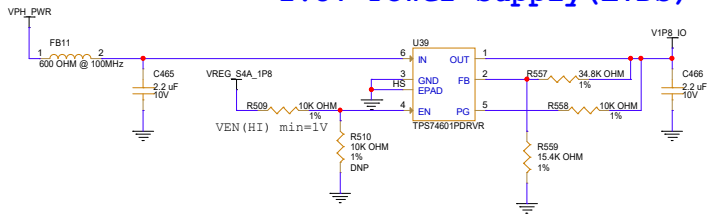
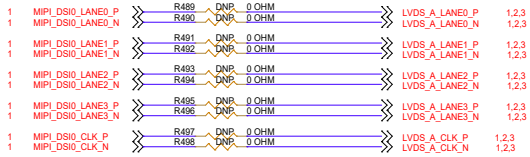
DSI to Dual LVDS

1.8V Power Supply(LVDS)

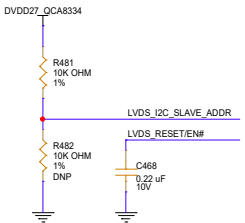


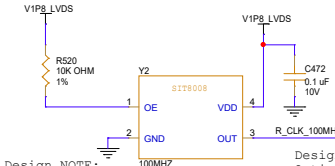
DESIGN NOTE
LVDS Controller bypass option



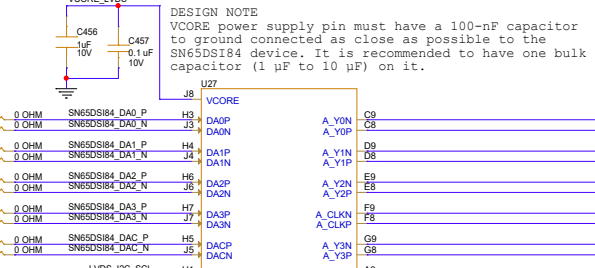
SMARC LVDS PORT-A(AS DSI)

DESIGN NOTE
I2C SLave Address
ADDR = 1, Slave Addr = 0x2D(Default)
ADDR = 0, Slave Addr = 0x2C

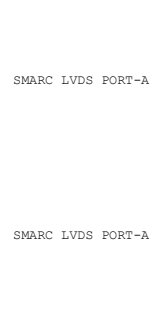




Design NOTE:
The LVDS CLK freq range for the SN65DSI8x is 25 - 154 MHz



Design NOTE:
Optional Resistor
to avoid Clock Ringing

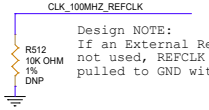


SMARC LVDS PORT-A

SMARC LVDS PORT-A

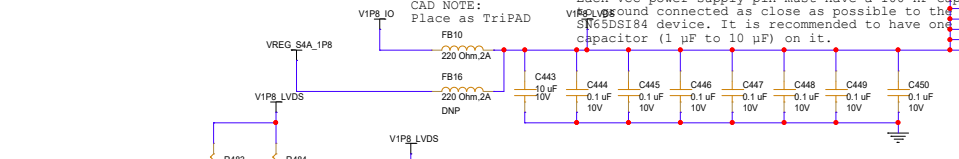
DESIGN NOTE
VCORE power supply pin must have a 100-nF capacitor to ground connected as close as possible to the SN65DSI84 device. It is recommended to have one bulk capacitor (1 µF to 10 µF) on it.

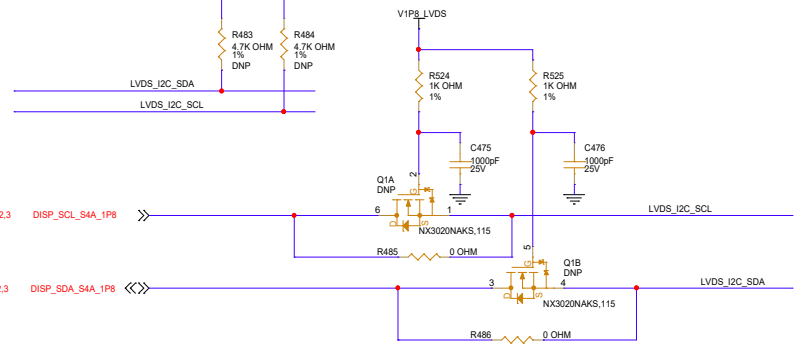
DESIGN NOTE
Each VCC power supply pin must have a 100-nF capacitor to ground connected as close as possible to the SN65DSI84 device. It is recommended to have one bulk capacitor (1 µF to 10 µF) on it.

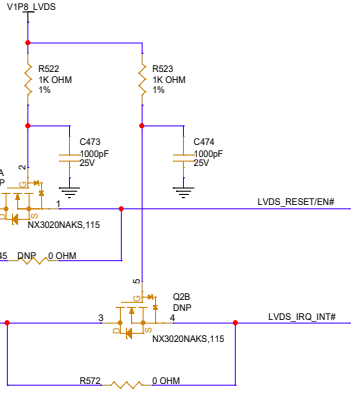


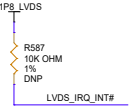
Design NOTE:
If an External Reference Clock is not used, REFCLK pin should be pulled to GND with an external resistor.

CAD NOTE:
Place as TriPAD



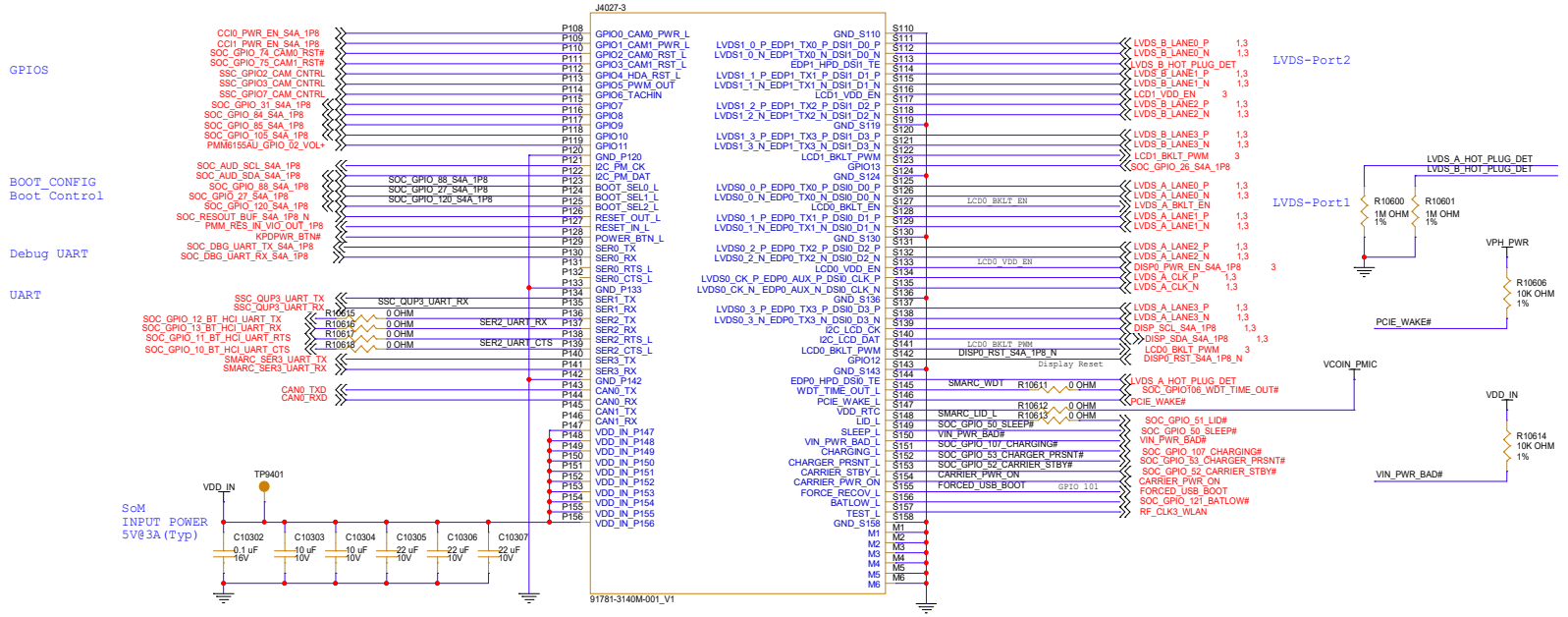






DSI to Dual LVDS			
Title: QCS615_SMARC_SoM			P0
Size: C	Document Number: 24090051-100-030		Rev: V0.12
Date: Monday, February 03, 2025	Sheet 1 of 3		

SoM Interface-2



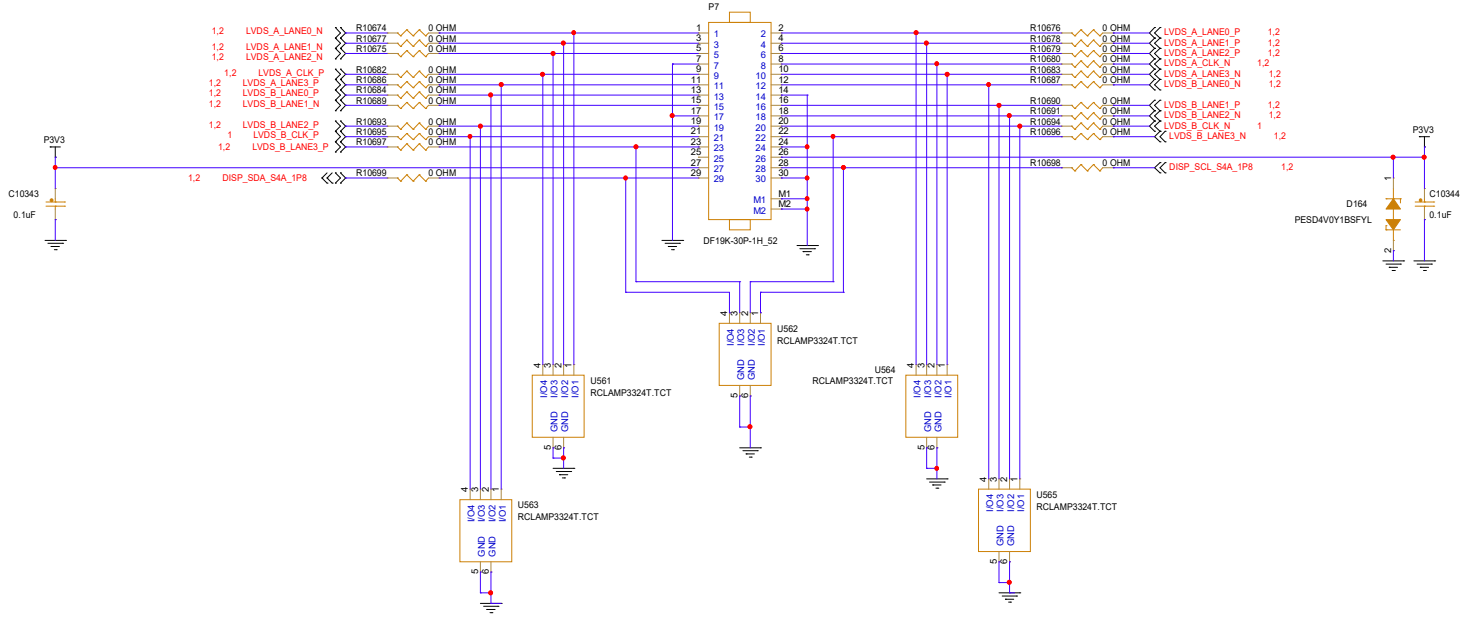
Title	iTERA_Gateway_Application_Board	
Size C	Document Number 24010046-100-030	Rev V1.0
Date: Monday, February 03, 2025	Sheet 2 of 3	

LVDS CONNECTOR 1

Module	13.3”FHD Color TFT-LCD with backlight driver
Manufacturer PN	G133HAN01.0
Manufacturer	FORTEC

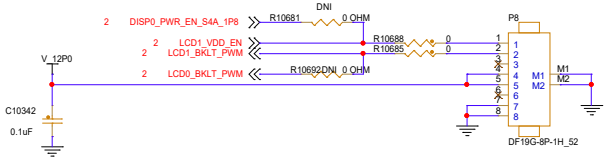
LCD MODULE CONNECTOR(DUAL LVDS)

Pinout is based on the following Display panel
https://www.fortec-integrated.de/en/products/tft-components/tft-displays/detail/auo/g133han011/



LED DRIVER CONNECTOR

NEED 12V



Title	DSI to HDMI iTERA_Gateway_Application_Board	
Size C	Document Number 24010046-100-030	Rev V1.0
Date: Monday, February 03, 2025	Sheet 3 of 3	