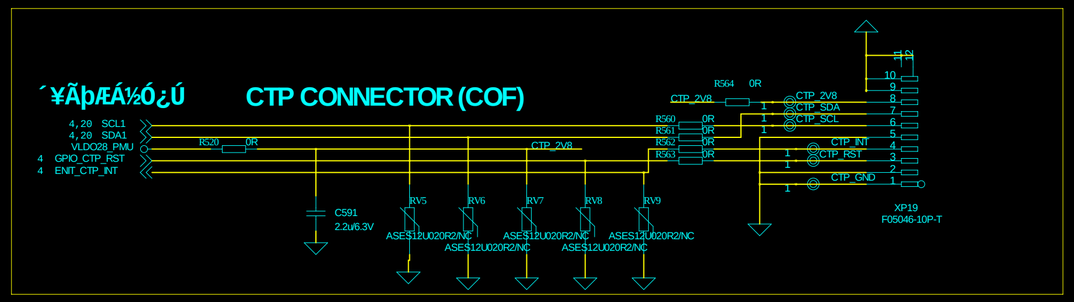
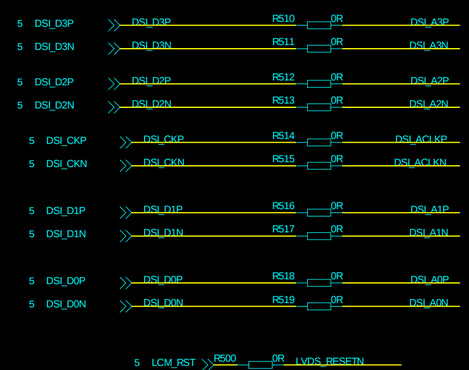
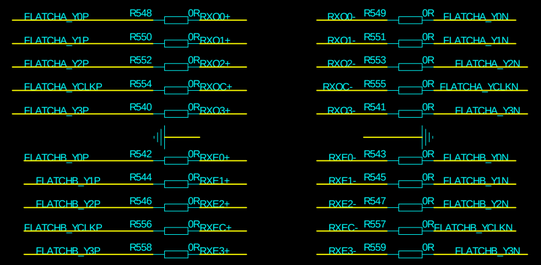
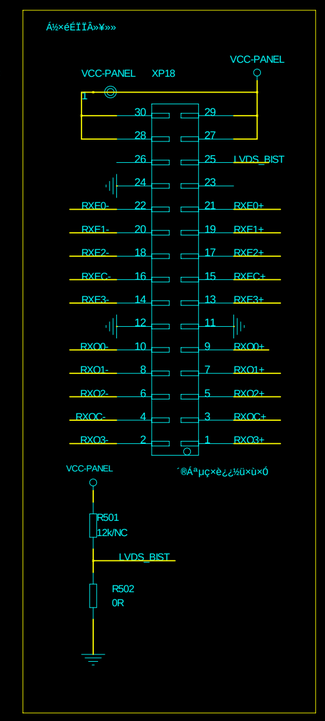
´¥ÃþÆÁ½Ó¿Ú CTP CONNECTOR (COF)

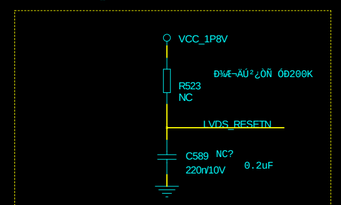




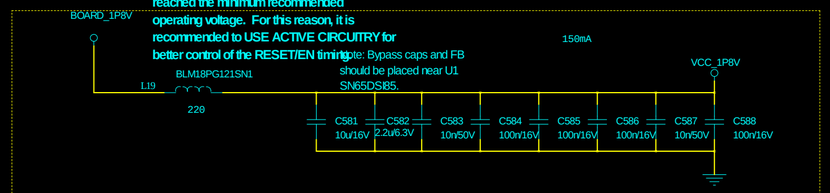




Reset Implementation

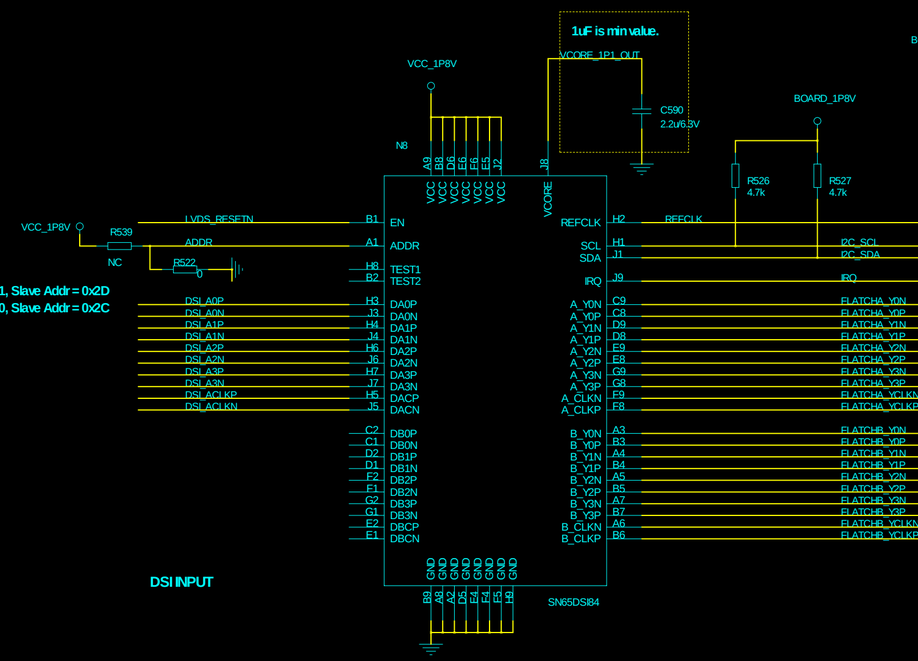


Reset(EN) can be implemented with passive components as shown or active circuitry. In case of using passive components, the values of the RC circuitry need to be adjusted to make sure the low to high transition occurs after the Vcc supply has reached the minimum recommended operating voltage. For this reason, it is recommended to USE ACTIVE CIRCUITRY for better control of the RESET/EN timing.

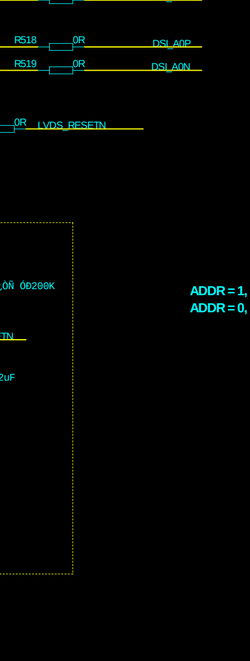


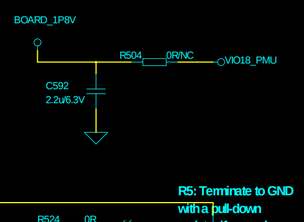
Note: Bypass caps and FB should be placed near U1 SN65DSI85.

The number of capacitors and their values may vary depending on the system implementation

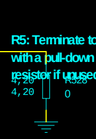


DSI INPUT



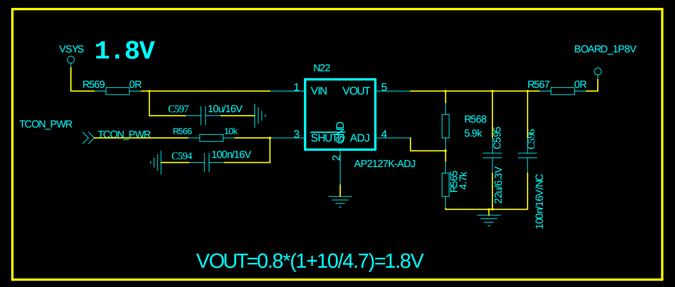


R5: Terminate to GND with a pull-down resistor if unused



IMPORTANT
If REFCLK is to be used, the CLK trace length between the REFCLK terminal and the source of the REF CLK(OSC or Xtal) should be kept as possble.

LVDS OUTPUT



********Layout Notes*******

For all differential pairs(DSI and LVDS) in this design follow the guidelines decribed below:
Route together with controlled differential 100ohm impedance and controlled single ended 50ohm impedance. Keep away from other high speed signals especially all FlatA/FlatB* signals. Keep lengths within 5mil of each other. Keep traces on layers adjacent to the ground plane. Keep the number of VIAS to minimum. If VIAS used, make it symetrical through all signals. Keep diff pairs separated at least by x3 of the trace width.
NO STUBS on the signal path, components should be placed such that the signals can routed in pass-thru manner.

				版本号 Ver.A
审核	宽俊斌			
标准化	曲春			RS67.820.xx
		郑理翔	阶段	第 1张 共 2张
				深圳电器股份有限公司
制图：				幅面： C