Schematic Review Form

Pin #	Name	Info	Violations	*Description*
A1	ADDR	When it is pulled high, ADDR must be tied to the device VCCIO such that this pin does not remain high when the device power is removed. This bit should be pulled high or low through a resistor depending on the I2C address the system chooses to use for the SN65DSIX6. When this pin is pulled low, the device address is 0x2C. When this pin is pulled high, the device address is 0x2D.		CMOS Input/Output Local I2C interface target address select. See Table 8-4. In normal operation, this pin is an input. When the ADDR pin is programmed high, it must be tied to the same 1.8-V power rails where the SN65DSI86 VCCIO 1.8-V power rail is connected.
H8	AUXP	The SN65DSIX6 supports a Manchester-II encoded 1-Mbps AUX interface. FAUX (Fast AUX) is not supported. Source detection pull-up and pull-down resistors are optional. Some DisplayPort sinks will require source detection resistors while others will not.	AUXP/N pins require AC coupling capacitors between the SN65DSIX6 and the DisplayPort sink. Place these capacitors close to the eDP receptacle. The AC-coupling capacitor must be in the range of 75 nF to 200 nF. A value of 100 nF is recommended. A package size of 0201 is recommended but a 0402 is acceptable.	Auxiliary-channel differential pair

H9	AUXN	The SN65DSIX6 supports a Manchester-II encoded 1-Mbps AUX interface. FAUX (Fast AUX) is not supported. Source detection pull-up and pull-down resistors are optional. Some DisplayPort sinks will require source detection resistors while others will not.	AUXP/N pins require AC coupling capacitors between the SN65DSIX6 and the DisplayPort sink. Place these capacitors close to the eDP receptacle. The AC-coupling capacitor must be in the range of 75 nF to 200 nF. A value of 100 nF is recommended. A package size of 0201 is recommended but a 0402 is acceptable.	Auxiliary-channel differential pair
H3	DA0P	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		LVDS Input (HS) CMOS Input/Output (LS) MIPI D-PHY channel A data lane 0; data rate up to 1.5 Gbps.
J3	DA0N	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		LVDS Input (HS) CMOS Input/Output (LS) MIPI D-PHY channel A data lane 0; data rate up to 1.5 Gbps.
H4	DA1P	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		LVDS Input (HS) CMOS Input/Output (LS) MIPI D-PHY channel A data lane 1; data rate up to 1.5 Gbps.
J4	DA1N	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		LVDS Input (HS) CMOS Input/Output (LS) MIPI D-PHY channel A data lane 1; data rate up to 1.5 Gbps.

H6	DA2P	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		LVDS Input (HS) CMOS Input/Output (LS) MIPI D-PHY channel A data lane 2; data rate up to 1.5 Gbps.
J6	DA2N	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		LVDS Input (HS) CMOS Input/Output (LS) MIPI D-PHY channel A data lane 2; data rate up to 1.5 Gbps.
H7	DA3P	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		LVDS Input (HS) CMOS Input/Output (LS) MIPI D-PHY channel A data lane 3; data rate up to 1.5 Gbps.
J7	DA3N	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		LVDS Input (HS) CMOS Input/Output (LS) MIPI D-PHY channel A data lane 3; data rate up to 1.5 Gbps.
H5	DACP	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		MIPI D-PHY channel A clock lane; operates up to 750 MHz. Under proper conditions, this clock can be used instead of REFCLK to feed DisplayPort PLL.
J5	DACN	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		MIPI D-PHY channel A clock lane; operates up to 750 MHz. Under proper conditions, this clock can be used

				instead of REFCLK to feed DisplayPort PLL.
C2	DB0P	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		MIPI D-PHY channel B data lane 0; data rate up to 1.5 Gbps.
C1	DB0N	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		MIPI D-PHY channel B data lane 0; data rate up to 1.5 Gbps.
D2	DB1P	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		MIPI D-PHY channel B data lane 1; data rate up to 1.5 Gbps.
D1	DB1N	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		MIPI D-PHY channel B data lane 1; data rate up to 1.5 Gbps.
F2	DB2P	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		MIPI D-PHY channel B data lane 2; data rate up to 1.5 Gbps.

F1	DB2N	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		MIPI D-PHY channel B data lane 2; data rate up to 1.5 Gbps.
G2	DB3P	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		MIPI D-PHY channel B data lane 3; data rate up to 1.5 Gbps.
G1	DB3N	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		MIPI D-PHY channel B data lane 3; data rate up to 1.5 Gbps.
E2	DBCP	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		MIPI D-PHY channel B clock lane; operates up to 750 MHz
E1	DBCN	DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).		MIPI D-PHY channel B clock lane; operates up to 750 MHz
B1	EN			Chip enable and reset. Device is reset (shutdown) when EN is low. Deassertion (low) of EN will cause all internal CSRs and functions to

				be reset to default state.
A8	GND			Reference ground for digital and analog circuits.
D8	GND			Reference ground for digital and analog circuits.
E4	GND			Reference ground for digital and analog circuits.
E5	GND			Reference ground for digital and analog circuits.
F4	GND			Reference ground for digital and analog circuits.
F5	GND			Reference ground for digital and analog circuits.
F6	GND			Reference ground for digital and analog circuits.
G8	GND			Reference ground for digital and analog circuits.
B4	GPIO[4]			CMOS Input/Output General-purpose I/O. See Section 8.3.3 section for details on GPIO functionality. When these pins are set high, tie the pins to the same 1.8-V power rail that the

				SN65DSI86 VCCIO 1.8-V power rail is connected to.
A6	GPIO[3]			CMOS Input/Output General-purpose I/O. See Section 8.3.3 section for details on GPIO functionality. When these pins are set high, tie the pins to the same 1.8-V power rail that the SN65DSI86 VCCIO 1.8-V power rail is connected to.
A5	GPIO[2]		When a GPIO is pulled-up, it should be pulled-up to the VCCIO supply. Unused GPIOs should be pulled-down or tied to GND.	CMOS Input/Output General-purpose I/O. See Section 8.3.3 section for details on GPIO functionality. When these pins are set high, tie the pins to the same 1.8-V power rail that the SN65DSI86 VCCIO 1.8-V power rail is connected to.
A4	GPIO[1]			CMOS Input/Output General-purpose I/O. See Section 8.3.3 section for details on GPIO functionality. When these pins are set high, tie the pins to the same 1.8-V power rail that the SN65DSI86 VCCIO 1.8-

				V power rail is connected to.
J8	HPD			CMOS Input with internal pulldown. (Failsafe) HPD input. This input requires a 51-kΩ 1% series resistor
A3	IRQ			CMOS Output Interrupt signal
F8	ML0P		All physical DisplayPort pins require AC coupling capacitors between the SN65DSIX6 and the DisplayPort Sink The AC coupling capacitor must be in the range of 75 nF to 200 nF. A value of 100 nF is recommended. A package size of 0201 is recommended but a 0402 is acceptable.	LVDS output (DP) DisplayPort lane 0 transmit differential pair. Supports 1.62 Gbps, 2.16 Gbps, 2.43 Gbps, 2.7 Gbps, 3.24 Gbps, 4.32 Gbps, and 5.4 Gbps. All DisplayPort lanes transmit at the same data rate
F9	ML0N		All physical DisplayPort pins require AC coupling capacitors between the SN65DSIX6 and the DisplayPort Sink The AC coupling capacitor must be in the range of 75 nF to 200 nF. A value of 100 nF is recommended. A package size of 0201 is recommended but a 0402 is acceptable.	LVDS output (DP) DisplayPort lane 0 transmit differential pair. Supports 1.62 Gbps, 2.16 Gbps, 2.43 Gbps, 2.7 Gbps, 3.24 Gbps, 4.32 Gbps, and 5.4 Gbps. All DisplayPort lanes transmit at the same data rate

E8	ML1P		All physical DisplayPort pins require AC coupling capacitors between the SN65DSIX6 and the DisplayPort Sink The AC coupling capacitor must be in the range of 75 nF to 200 nF. A value of 100 nF is recommended. A package size of 0201 is recommended but a 0402 is acceptable.	LVDS output (DP) DisplayPort lane 1 transmit differential pair. Supports 1.62 Gbps, 2.16 Gbps, 2.43 Gbps, 2.7 Gbps, 3.24 Gbps, 4.32 Gbps, and 5.4 Gbps. All DisplayPort lanes transmit at the same data rate
E9	ML1N		All physical DisplayPort pins require AC coupling capacitors between the SN65DSIX6 and the DisplayPort Sink The AC coupling capacitor must be in the range of 75 nF to 200 nF. A value of 100 nF is recommended. A package size of 0201 is recommended but a 0402 is acceptable.	LVDS output (DP) DisplayPort lane 1 transmit differential pair. Supports 1.62 Gbps, 2.16 Gbps, 2.43 Gbps, 2.7 Gbps, 3.24 Gbps, 4.32 Gbps, and 5.4 Gbps. All DisplayPort lanes transmit at the same data rate
C8	ML2P		All physical DisplayPort pins require AC coupling capacitors between the SN65DSIX6 and the DisplayPort Sink The AC coupling capacitor must be in the range of 75 nF to 200 nF. A value of 100 nF is recommended. A package size of 0201 is recommended but a 0402 is acceptable.	LVDS output (DP) DisplayPort lane 2 transmit differential pair. Supports 1.62 Gbps, 2.16 Gbps, 2.43 Gbps, 2.7 Gbps, 3.24 Gbps, 4.32 Gbps, and 5.4 Gbps. All DisplayPort lanes transmit at the same data rate

C9	ML2N		All physical DisplayPort pins require AC coupling capacitors between the SN65DSIX6 and the DisplayPort Sink The AC coupling capacitor must be in the range of 75 nF to 200 nF. A value of 100 nF is recommended. A package size of 0201 is recommended but a 0402 is acceptable.	LVDS output (DP) DisplayPort lane 2 transmit differential pair. Supports 1.62 Gbps, 2.16 Gbps, 2.43 Gbps, 2.7 Gbps, 3.24 Gbps, 4.32 Gbps, and 5.4 Gbps. All DisplayPort lanes transmit at the same data rate
B8	ML3P		All physical DisplayPort pins require AC coupling capacitors between the SN65DSIX6 and the DisplayPort Sink The AC coupling capacitor must be in the range of 75 nF to 200 nF. A value of 100 nF is recommended. A package size of 0201 is recommended but a 0402 is acceptable.	LVDS output (DP) DisplayPort lane 3 transmit differential pair. Supports 1.62 Gbps, 2.16 Gbps, 2.43 Gbps, 2.7 Gbps, 3.24 Gbps, 4.32 Gbps, and 5.4 Gbps. All DisplayPort lanes transmit at the same data rate
B9	ML3N		All physical DisplayPort pins require AC coupling capacitors between the SN65DSIX6 and the DisplayPort Sink The AC coupling capacitor must be in the range of 75 nF to 200 nF. A value of 100 nF is recommended. A package size of 0201 is recommended but a 0402 is acceptable.	LVDS output (DP) DisplayPort lane 3 transmit differential pair. Supports 1.62 Gbps, 2.16 Gbps, 2.43 Gbps, 2.7 Gbps, 3.24 Gbps, 4.32 Gbps, and 5.4 Gbps. All DisplayPort lanes transmit at the same data rate

A7	REFCLK		A series resistor is recommended near the RECLK source to reduce EMI. If possible, bury the REFCLK trace in the inner layer or minimize the trace length from the REFCLK terminal to CLK source by placing the source near the SN65DSIX6 REFCLK terminal.	Reference clock. Frequency determined by value programmed in I2C register or value of GPIO[3:1] latched at rising edge of EN. Supported frequencies are: 12 MHz, 19.2 MHz, 26 MHz, 27 MHz, and 38.4 MHz. This pin must be tied to GND when DACP/N feeds the DisplayPort PLL
H1	SCL		The I2C interface (SDA and SCL pins) requires external pull-up resistors to VCCIO for proper operation.	OpenDrain Input/Output (Failsafe) Local I2C interface clock.
J1	SDA		The I2C interface (SDA and SCL pins) requires external pull-up resistors to VCCIO for proper operation.	OpenDrain Input/Output (Failsafe) Local I2C interface bidirectional data signal.
B3	TEST1			Used for Texas Instruments internal use only. This pin must be left unconnected or tied to ground

B5	TEST2		TEST2 must be pulled up to VCCIO when performing DisplayPort compliance testing.	CMOS Input/Output with internal pulldown Used for internal test, HBR2 compliance eye, and symbol error rate measurement pattern. For normal operation, pull down this pin to GND or leave unconnected. See Table 8-15 for information on HBR2 compliance eye and symbol error rate measurement patterns.
B7	TESt3			Used for Texas Instruments internal use only. This pin must be left unconnected or tied to GND through a 0.1-µF capacitor.
D6	VCC		needs 100nF decoupling capacitor between power plane and pin	1.2-V power supply for digital core
D5	VCC		needs 100nF decoupling capacitor between power plane and pin	1.2-V power supply for digital core
J2	VCC		needs 100nF decoupling capacitor between power plane and pin	1.2-V power supply for digital core
J9	VCC		needs 100nF decoupling capacitor between power plane and pin	1.2-V power supply for digital core

A9	VCCA		These supply pins should be connected to a power plane and each pin should have a 100-nF or 10-nF decoupling capacitor.	1.2-V power supply for analog circuits. AVCC and VCC can be applied simultaneously.
G9	VCCA		These supply pins should be connected to a power plane and each pin should have a 100-nF or 10-nF decoupling capacitor.	1.2-V power supply for analog circuits. AVCC and VCC can be applied simultaneously.
E6	VCCA		These supply pins should be connected to a power plane and each pin should have a 100-nF or 10-nF decoupling capacitor.	1.2-V power supply for analog circuits. AVCC and VCC can be applied simultaneously.
B2	VCCA		These supply pins should be connected to a power plane and each pin should have a 100-nF or 10-nF decoupling capacitor.	1.2-V power supply for analog circuits. AVCC and VCC can be applied simultaneously.
H2	VCCA		These supply pins should be connected to a power plane and each pin should have a 100-nF or 10-nF decoupling capacitor.	1.2-V power supply for analog circuits. AVCC and VCC can be applied simultaneously.
B6	VCCIO		Using a 100-nF capacitor on each VCCIO pin is recommended.	1.8-V power supply for Digital I/O
A2	VCCIO		Using a 100-nF capacitor on each VCCIO pin is recommended.	1.8-V power supply for Digital I/O
D9	VPLL		For optimal performance, it is critical this pin is well filtered. A 1-µF, 100-nF, and 10-nF decoupling capacitor is recommended.	1.8-V power supply for DisplayPort PLL

Comments