Texas Instruments Incorporated

DS75176B to SN75176B Transition Document

This document outlines the differences between DS75176B and SN75176B. The SN75176B incorporates all of the features of the DS75176B and it can works as direct replacement with better performance.

1 MAIN DIFFERENCE BETWEEN DS75176B AND SN75176B

1.1 Pin out differences.

Figure 1 shows the differences between both devices externally. It should be noted that the only difference are the names. Table 1 shows the description of names.

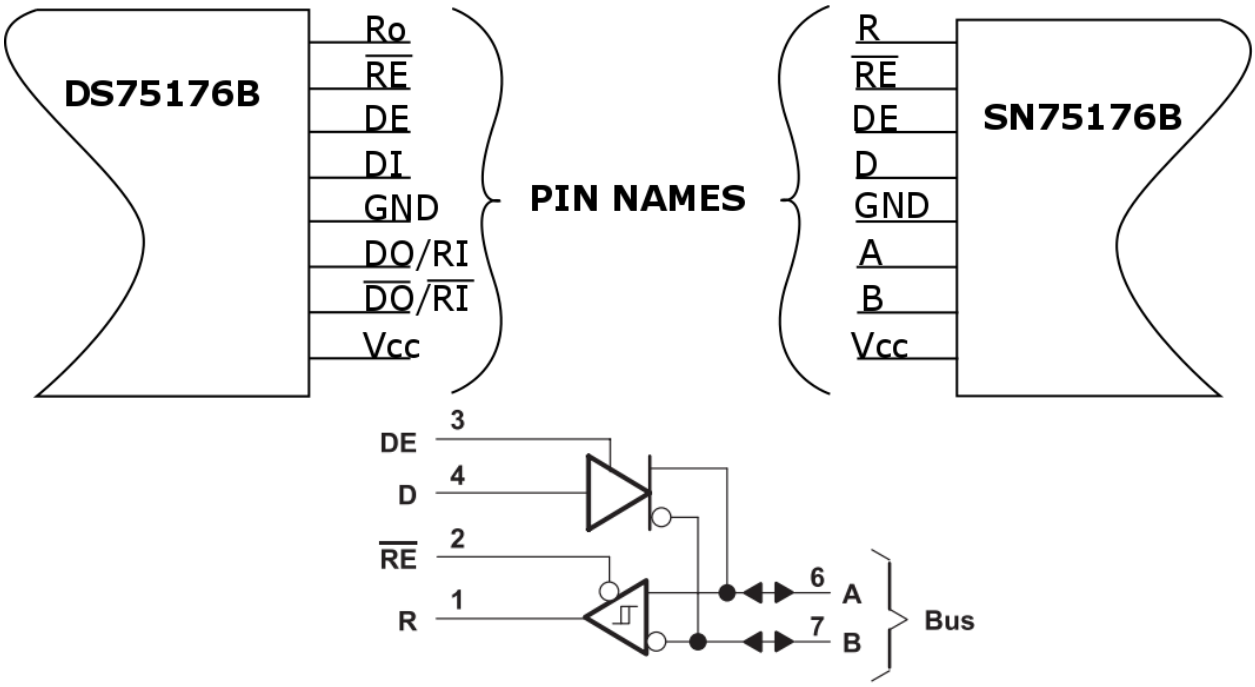


Figure 1. Pins' compatibility

Table 1. Pin names Compatibility

DS75176B	SN75176B	DESCRIPTION
Ro **1**	**R** **1**	Logic Data Output from RS-485 Receiver
/RE **2**	**/RE** **2**	Receive Enable (active low)
DE **3**	**DE** **3**	Driver Enable (active high)
DI **4**	**D** **4**	Logic Data Input to RS-485 Driver
GND **5**	**GND** **5**	Device Ground pin
DO/RI **6**	**A** **6**	RS-422 or RS-485 Data Line
/DO-/RI **7**	**B** **7**	RS-422 or RS-485 Data Line
Vcc **8**	**Vcc** **8**	Power input. Connect to 5 V Power Source.

1.2 Electrical Parameters

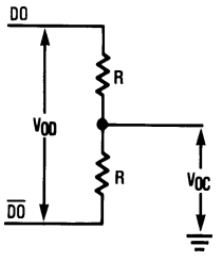
This section shows the main differences regarding electrical parameters between both devices.

		Parameter	
Absolute Maximum Ratings		**DS75176B**	**SN75176B**
Supply Voltage, VCC		7 V	7 V
Control Input Voltages		7 V	5.5 V
Driver Input Voltage		7 V	+15V/ −10V
Driver Output Voltages		+15V/ −10V	+15V/ −10V
Receiver Input Voltages (DS75176B)		+15V/ −10V	+15V/ −10V
Receiver Output Voltage		5.5V	+15V/ −10V
Continuous Power Dissipation @ 25°C	for SOIC Package	675 mW	
	for PDIP Package	900 mW	
Storage Temperature Range		−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds) (in case of version SN75176B lead temperature 1.6 mm from case for 10 seconds)		260°C	260°C
Operating virtual junction temperature			150°C
ESD Rating (HBM)		500V	2000V

Recommended Operating Conditions		**DS75176B**			**SN75176B**		
		Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
Supply Voltage, Vcc		4.75 V	5 V	5.25 V	4.75 V	5 V	5.25 V
Voltage at Any Bus Terminal, (Separate or Common Mode)		−7 V		12 V	−7 V		12 V
VIH High-level input voltage	D, DE, and /RE	2 V			2 V		
VIL Low-level input voltage				.8 V			.8 V
VID Differential input voltage				±12 V			±12 V
Operating Free Air Temperature TA		0 °C		70 °C	0 °C		70 °C
IOH High-level output current	Driver						–60 mA
	Receiver						–400 uA
IOL Low-level output current	Driver						60 mA
	Receiver						8 mA
RθJA Junction-to-ambient thermal resistance	Package BD						97 °C/W
	Package BP						85 °C/W
	Package BPS						95 °C/W

Electrical Characteristics -- Driver		DS75176B			SN75176B		
	Test Condition	Min	Typ	Max	Min	Typ	Max
VCL/VIK Input clamp voltage	II = –18 mA						–1.5 V
IIL Input Low Current	VI = 0.4 V			–200 uA			–400 uA
IIH High-level input current	VI = 2.4 V			20 uA			20 uA
|VOD1| Differential output voltage	IO = 0			5 V	1.5 V	3.6 V	6 V
|VOD2| Differential output voltage	RL = 100 Ω	2V			2 V	2.7 V	
	RL = 54 Ω	1.5V			1.5 V	2.5 V	5 V
Δ|VOD| Change in magnitude of differential output voltage	RL = 54 Ω			0.2 V			±0.2 V
Δ|VOC| Change in magnitude of common-mode output voltage	RL = 54 Ω			0.2 V			±0.2 V
VOC Common-mode output voltage	RL = 54 Ω or 100 Ω, see Figure 8			3 V	–1 V		3 V
IO Output current	Output disabled, VO = 12 V						1 mA
	Output disabled, VO = 12 V						–0.8 mA
IOS Short-circuit output current	VO = –7 V			–250 mA			–250 mA
	VO = 0						–150 mA
	VO = VCC						250 mA
	VO = 12 V			250 mA			250 mA
ICC Supply current (total package)	No load. Outputs enabled			55 mA		42 mA	70 mA
	No load. Outputs disabled			35 mA		26 mA	35 mA

Electrical Characteristics -- Receiver		DS75176B			SN75176B		
	Test Condition	Min	Typ	Max	Min	Typ	Max
VIT+ Positive-going input threshold voltage	VO = 2.7 V, IO = –0.4 mA			0.2 V			0.2 V
VIT– Negative-going input threshold voltage	VO = 0.5 V, IO = 8 mA	−0.2 V			−0.2 V		
Vhys Input hysteresis voltage (VIT+ – VIT-)	VCM = 0V		70 mV			50 mV	
VIK Enable clamp voltage	II = –18 mA			–1.5 V			–1.5 V
VOH High-level output voltage	VID = 200 mV, IOH = –400 µA See Figure 9	2.7 V			2.7 V		
VOL Low-level output voltage	VID = 200 mV, IOL = 8 mA See Figure 9			IOL = 16 mA, .5 V			.45 V
IOZR/IOZ High-impedance-state output current	VO = 0.4 V to 2.4 V						±20 uA
	VCC = Max 0.4V ≤ VO ≤ 2.4V			±20 uA			±20 uA
II Line input current	Other input = 0 V, VI = 12 V						1 mA
	Other input = 0 V, VI = –7 V						–0.8 mA
IIH High-level enable input current	VIH = 2.7 V			20 uA			20 uA
IIL Low-level enable input current	VIL = 0.4 V			–200 uA			–100 uA
ri Input resistance	−7V ≤ VCM ≤ +12V	12 kΩ			12 kΩ		
IOS Short-circuit output current	VO = 0V	–15 mA		–85 mA	–15 mA		–85 mA
ICC Supply current (total package)	No load, Outputs enabled			55 mA		42 mA	55 mA
	No load, Outputs disabled			35 mA		26 mA	35 mA



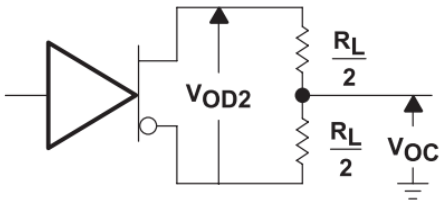


Figure 8. Driver V_{OD} and V_{OC}

Figure 2.

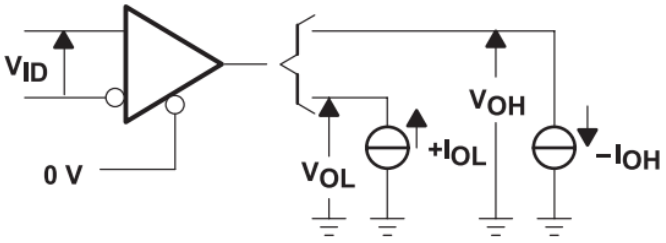


Figure 9. Receiver V_{OH} and V_{OL}

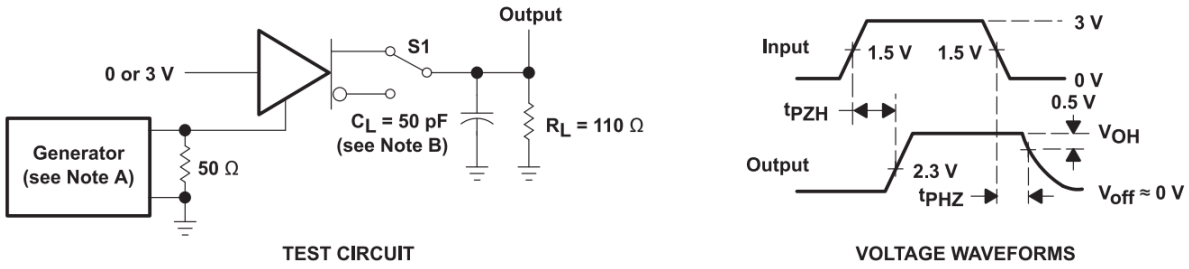
1.3 Switching Characteristics

This section shows the differences regarding of switching time.

Switching characteristics -- Driver	**VCC = 5 V, TA = 25°C**	**DS75176B**			**SN75176B**		
Parameter	Test Conditions	Min	Typ	Max	Min	Typ	Max
td(OD) Differential-output delay time	RL = 54 Ω, See Figure 12					15 nS	22 nS
tt(OD) Differential-output transition time						20 nS	30 nS
tPZH Output enable time to high leve	RL = 110 Ω, See Figure 11		CL = 100 pF 29 nS	CL = 100 pF 100 nS		85 nS	120 nS
tPZL Output enable time to low level	RL = 110 Ω, See Figure 14		CL = 100 pF 31 nS	CL = 100 pF 60 nS		40 nS	60 nS
tPHZ Output disable time from high level	RL = 110 Ω, See Figure 11		CL = 15 pF 19 nS	CL = 15 pF 200 nS		150 nS	250 nS
tPLZ Output disable time from low level	RL = 110 Ω, See Figure 14		CL = 15 pF 28 nS	CL = 15 pF 32 nS		20 nS	30 nS

Switching characteristics -- Receiver	**VCC = 5 V, TA = 25°C, CL = 15 pF**	**DS75176B**			**SN75176B**		
Parameter	Test Conditions	Min	Typ	Max	Min	Typ	Max
tPLH Propagation delay time, low-to-highlevel output	VID = –1.5 V to 1.5 V, See Figure 13		30 nS	37 nS		21 nS	35 nS
tPHL Propagation delay time, high-to-lowlevel output			32 nS	37 nS		23 nS	35 nS
tPZH Output enable time to high level	See Figure 16		11 nS	20 nS		10 nS	20 nS
tPZL Output enable time to low level			15 nS	20 nS		12 nS	20 nS
tPHZ Output disable time from high level			13 nS	35 nS		20 nS	35 nS
tPLZ Output disable time from low level			28 nS	32 nS		17 nS	25 nS

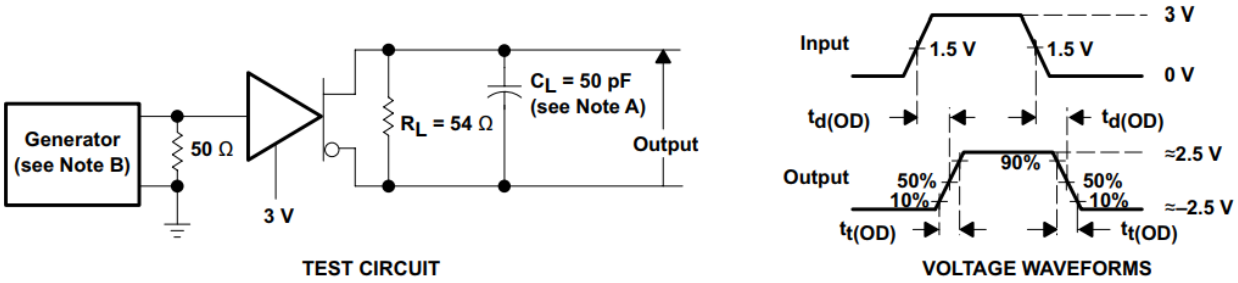
Figures and time diagrams



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 W.

B. C_L includes probe and jig capacitance.

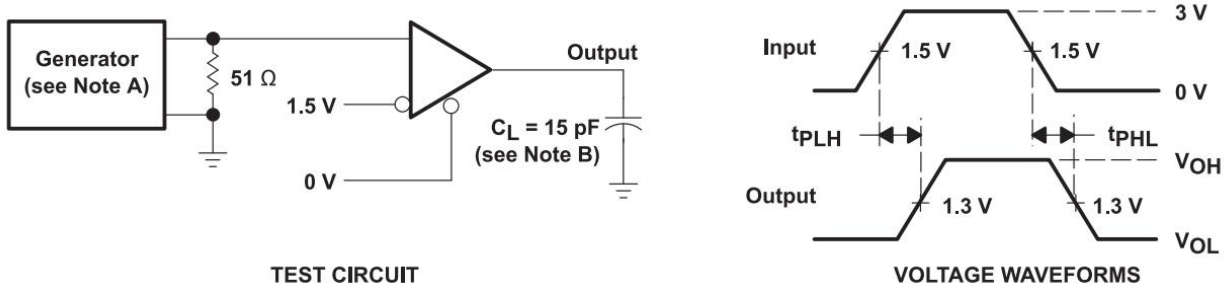
Figure 11. Driver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

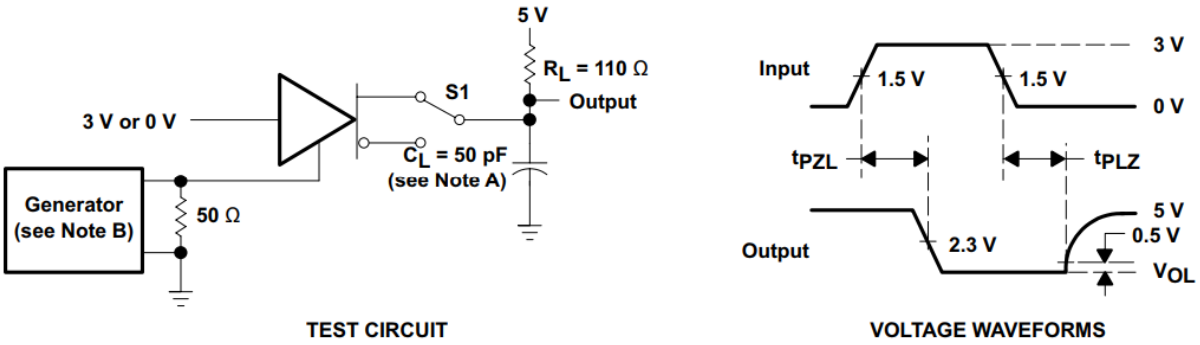
Figure 12. Driver Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 W.

B. C_L includes probe and jig capacitance.

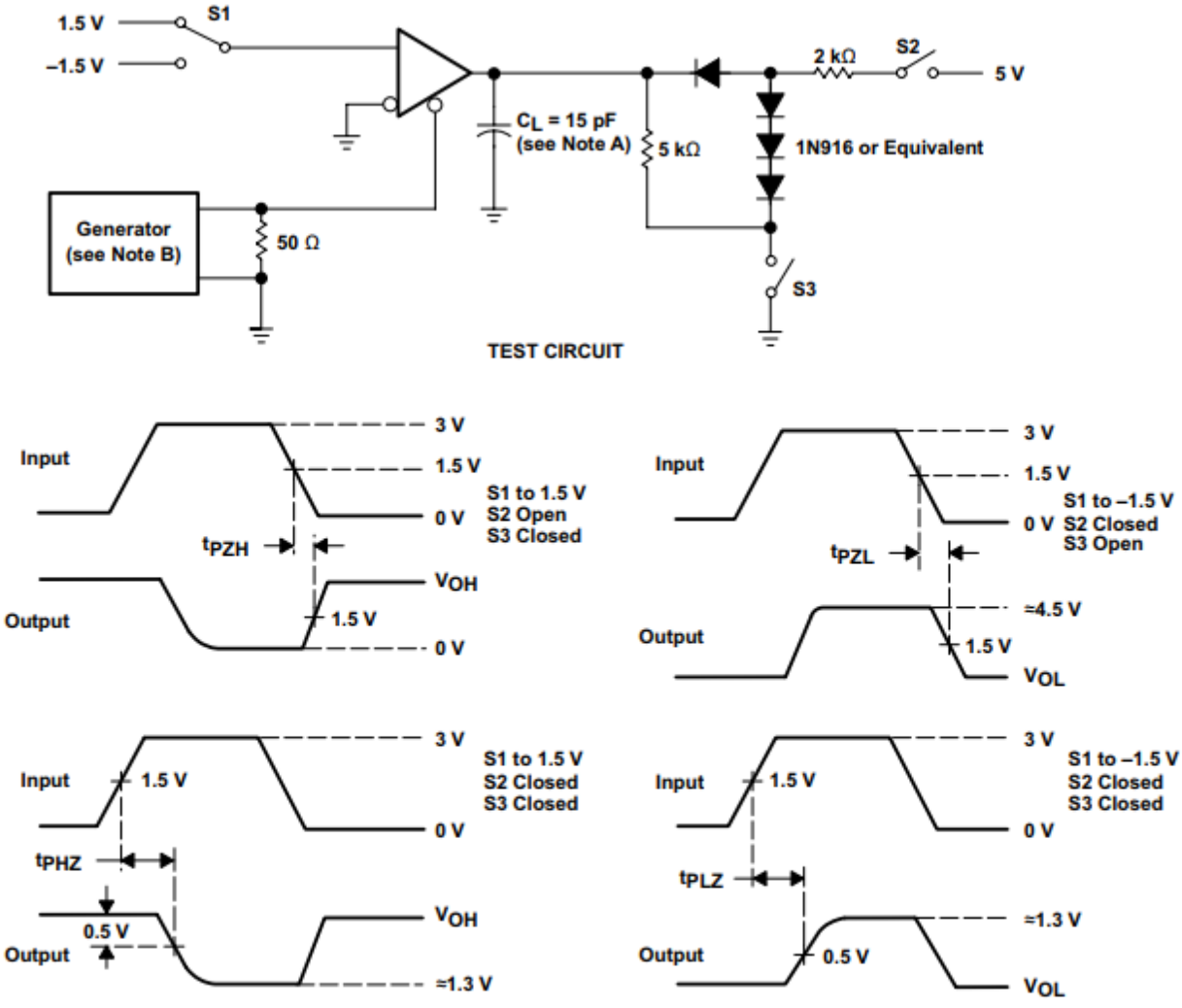
Figure 13. Receiver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 14. Driver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 16. Receiver Test Circuit and Voltage Waveforms