User's Guide
June 2009

SN75DP139 EVM

ABSTRACT

The SN75DP139 is a Dual-Mode DisplayPort input to TMDS output translator. The TMDS output has a built in level translator compliant with Digital Video Interface (DVI) 1.0 and High Definition Multimedia Interface (HDMI) 1.3. There are two separate EVM's to support the two physical interfaces. The SN75DP139 will support data rates of up to 2.5Gbps through each link in order to support resolutions greater then 1920x1200 or HDTV 12 bit color depth at 1080p.

An integrated Active I^2C buffer isolates the capacitive loading of the source system from that of the sink and interconnecting cable. This isolation improves overall signal integrity of the system and allows for considerable design margin within the source system for DVI / HDMI compliance testing.

A logic block has been designed into the SN75DP139 in order to assist with TMDS connector identification. Through the use of the I^2C_EN pin a logic block that will respond to I^2C read commands can be enabled to indicate that the translated port is a HDMI port thus legally supporting HDMI content.

The SN75DP139 is also equipped with output enable (OE_N) and DDC enable (DDC_EN) for low-power consumption during shut-down and DDC buffer enabling. Other additional features include edge-rate control (SRC) and DDC offset (OVS).

This evaluation module is a reference design for using the device as an integrated part of a digital television on a four layer board. The design principles of this design incorporating the SN75DP139 could potentially be used in other similar applications.

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Introduction

The SN75DP139 is a high-speed Display Port to HDMI/DVI (TMDS) signal translator. This guide describes the construction and usage of the EVM for the SN75DP139. The EVM is meant to serve as an evaluation tool for the SN75DP139.

SN75DP139 Evaluation Module Configuration

SN75DP139 EVM Kit Contents

This EVM kit should contain the following items:

- SN75DP139 EVM board
- This user's manual

Description of EVM Board

The SN75DP139 EVM is designed to provide easy evaluation of the SN75DP139 device.

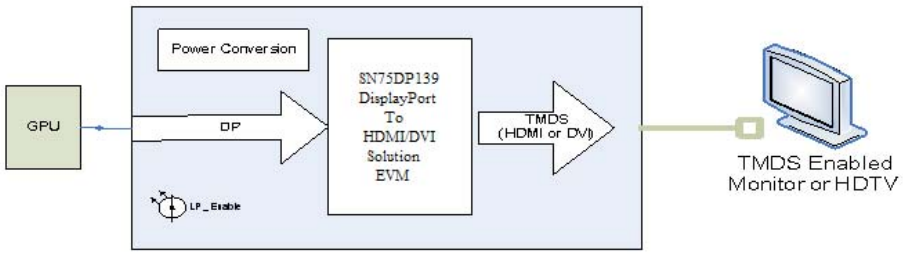

Figure 1. SN75DP139 EVM Block Diagram

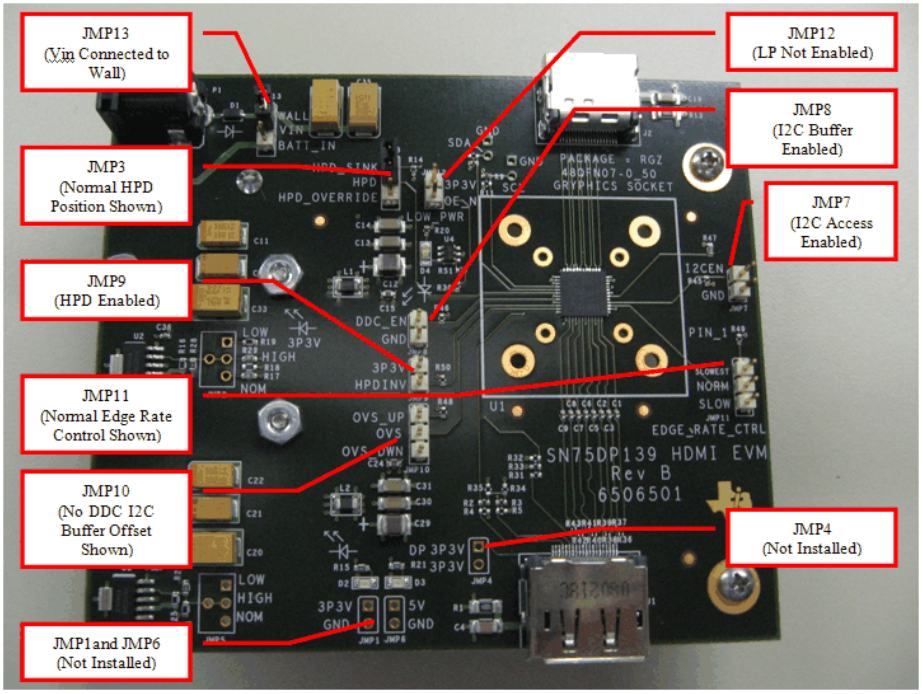

Figure 2. SN75DP139 EVM for HMDI Switch and Jumper Location

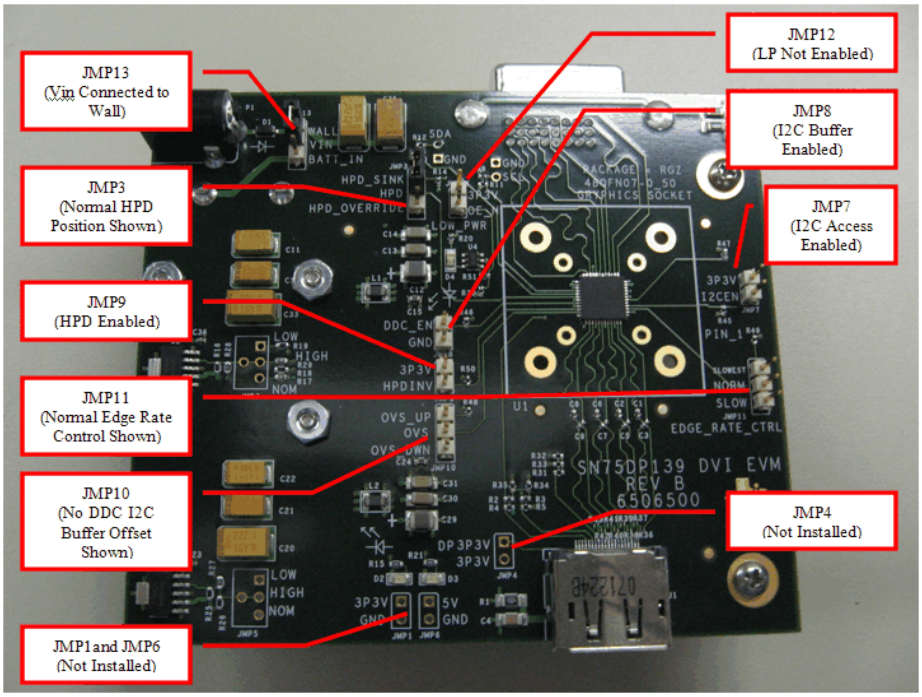

Figure 3. SN75DP139 EVM for DVI Switch and Jumper Location

Jumper Number/ Switch	Functionality
JMP12	Allows for LP mode to be manually controlled (installed = LP mode is enabled with LED indication)
JMP3	HPD Override/HPD_SINK (Only used to override or create an HPD)
JMP6 (not installed)	Allows for easy connect to the 5V rail for monitoring
JMP1 (not installed)	Allows for easy connect to the 3.3V rail for monitoring
JMP13	Allows for selection of EVM power from the wall or 9V battery Normal position would be "Wall" to "VIN"
JMP4 (not installed)	Allows for the DP 3.3V power to be connected to the board 3.3V
JMP7	I2C Enable (Installed = disabling access for internal I2C registers)
JMP8	DDC I2C buffer be enable/disable (Installed = I2C buffer disabled)
JMP9	Allows HPD_INV to be connected to 3.3V (Installed = disabling HPD)
JMP11	Edge Rate Control (Adjust TMDS output rise/fall time)
JMP10	DDC I2C buffer offset adjustment

Table 1. Jumper and Switch Functionality

The power supply provided with this EVM is a +9V AC power supply. The output voltage of the power supply should be within the range of +5V to +10V (JMP13 = VIN_WALL).

For portability, a battery holder is also provided for use with a 9V battery (JMP13 = BATT_IN).

PCB Construction

This section discusses the construction of the EVM boards. It includes the board schematics and Gerber files to show how the board was built.

SN75DP139 EVM Board Schematics

This section shows the board schematic sheets for the EVM.

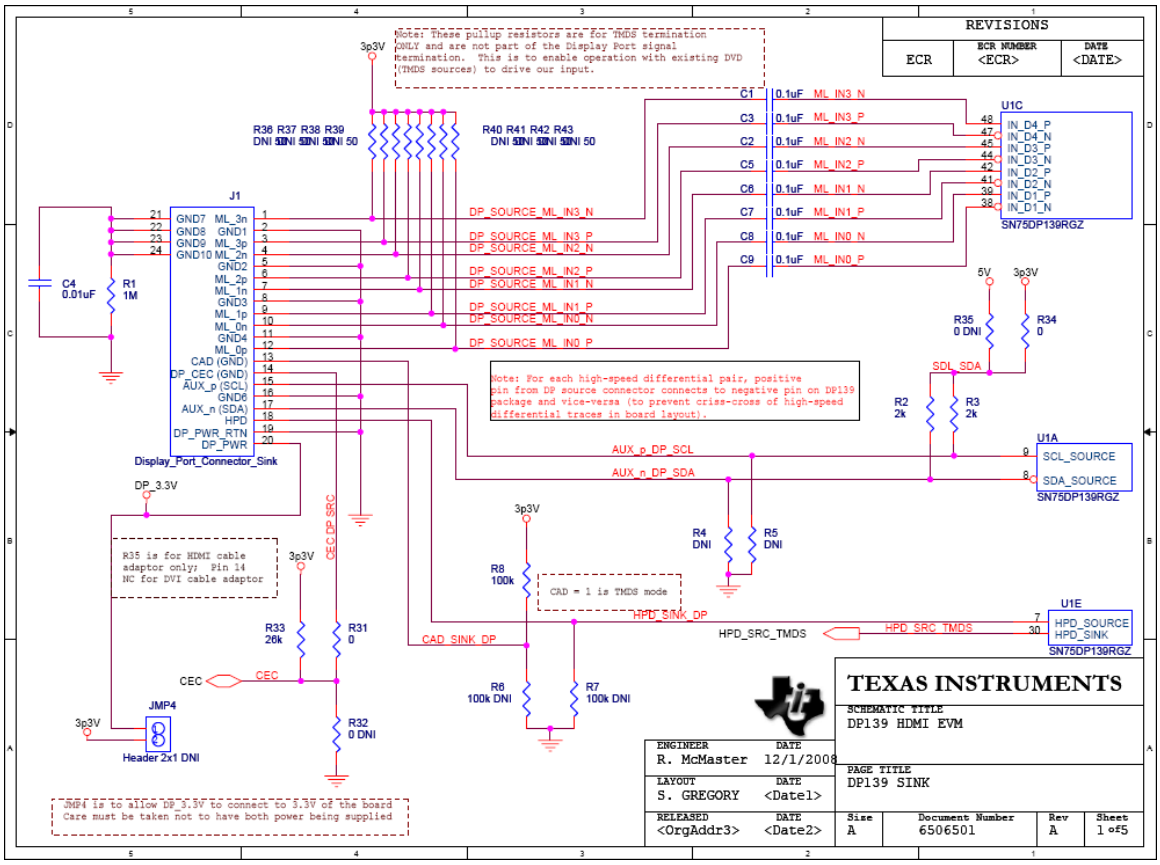

Figure 4. SN75DP139 EVM for HDMI Schematic Page 1

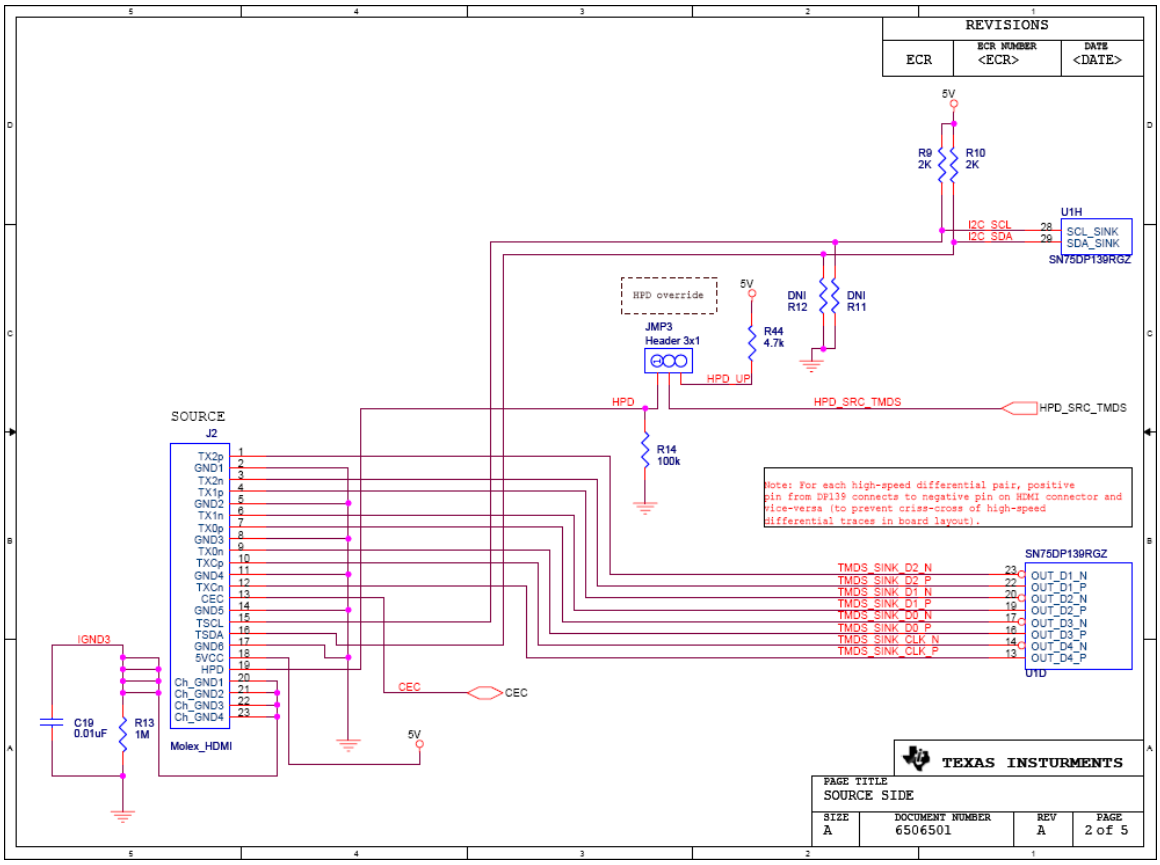

Figure 5. SN75DP139 EVM for HDMI Schematic Page 2

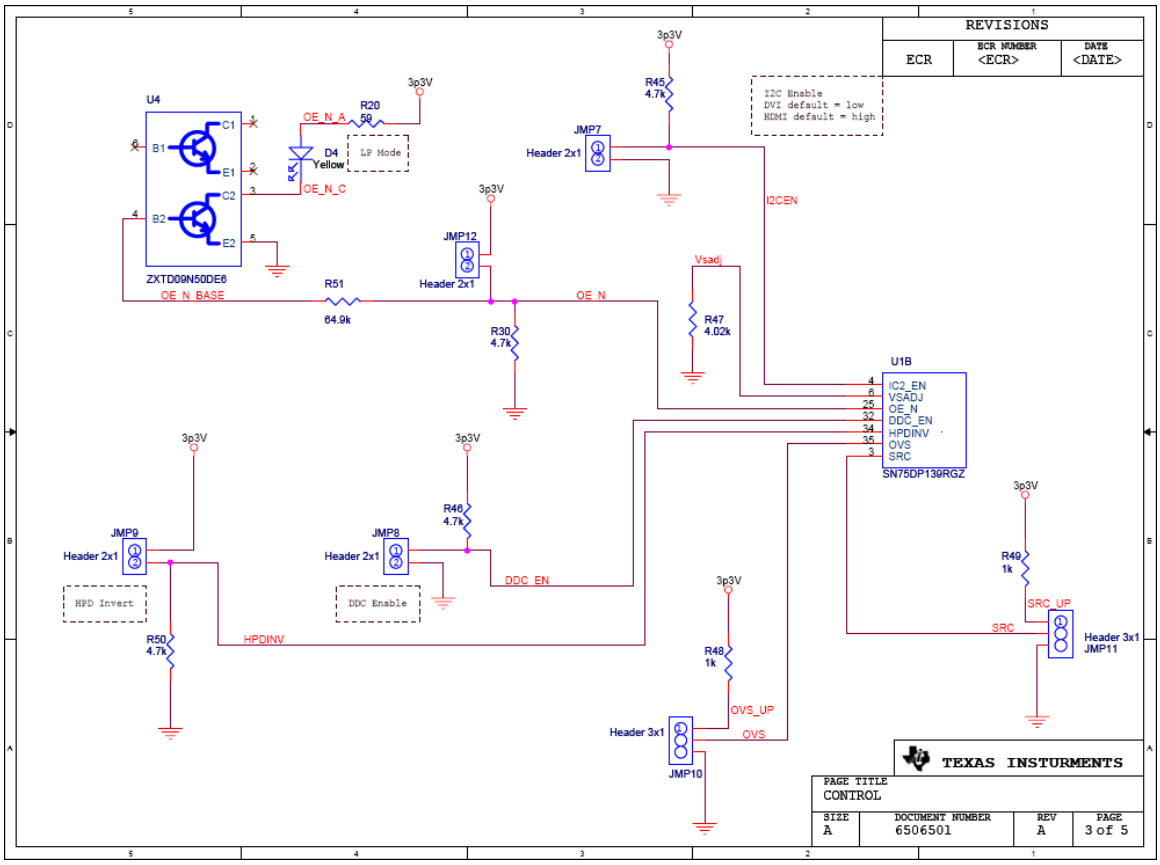

Figure 6. SN75DP139 EVM for HDMI Schematic Page 3

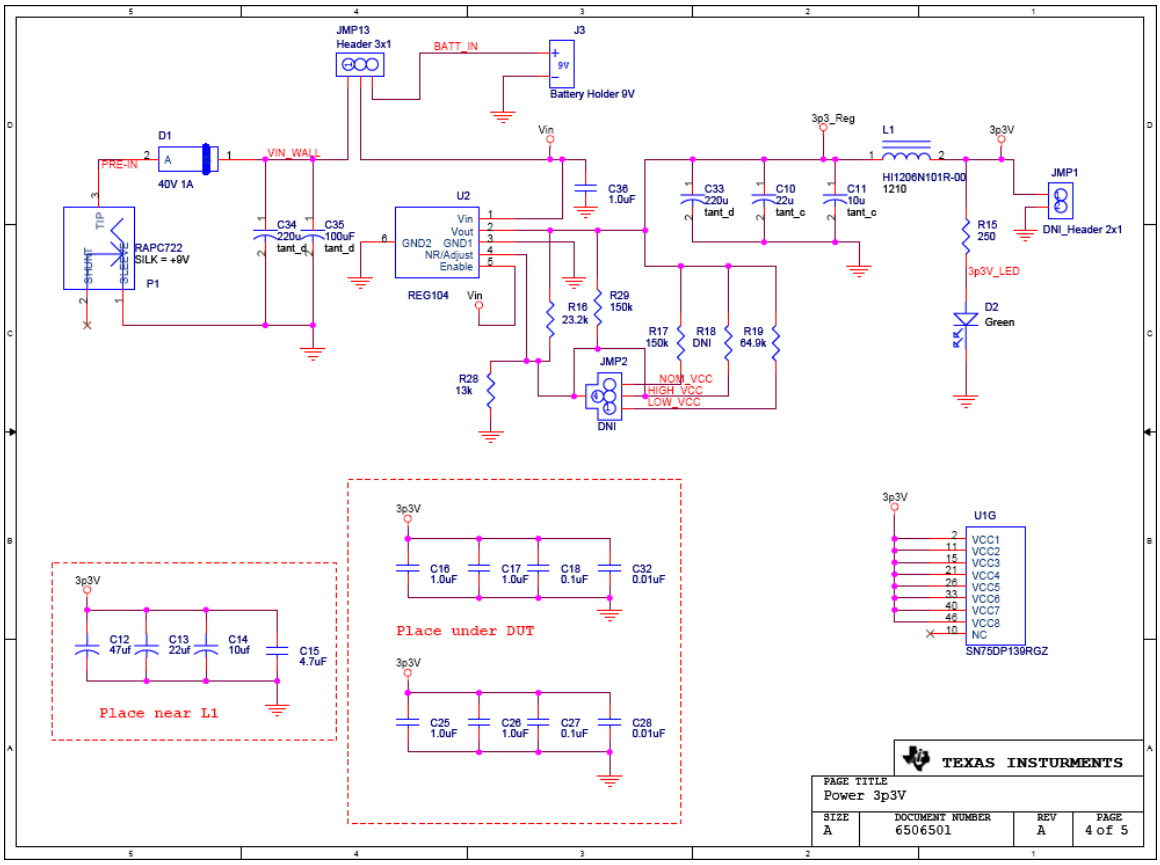

Figure 7. SN75DP139 EVM for HDMI Schematic Page 4

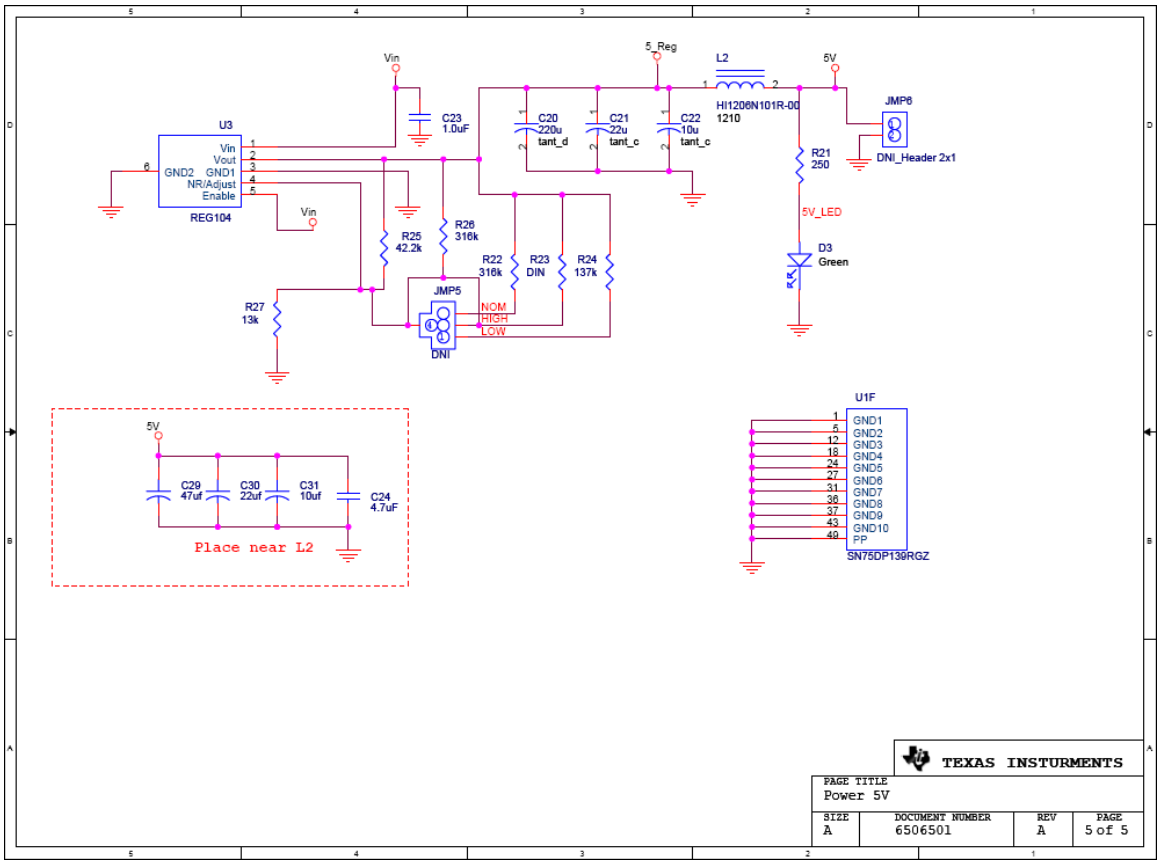

Figure 8. SN75DP139 EVM for HDMI Schematic Page 5

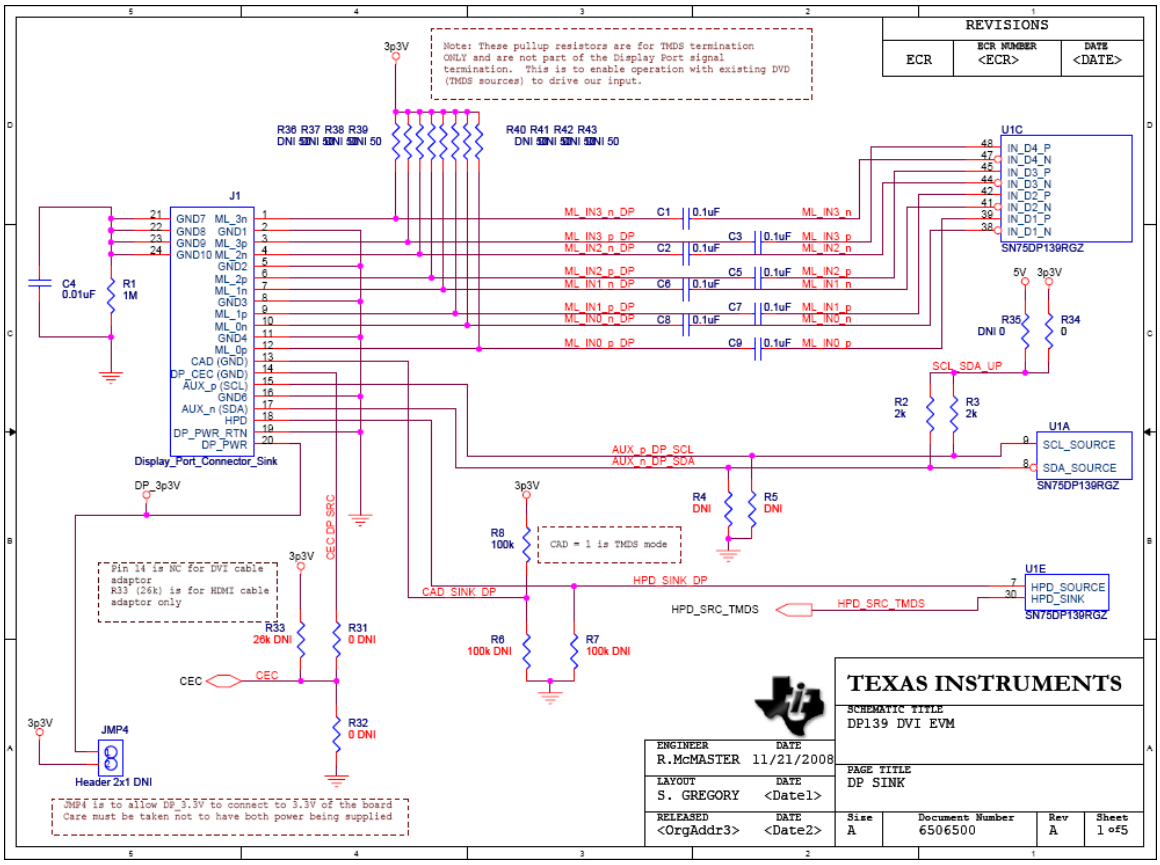

Figure 9. SN75DP139 EVM for DVI Schematic Page 1

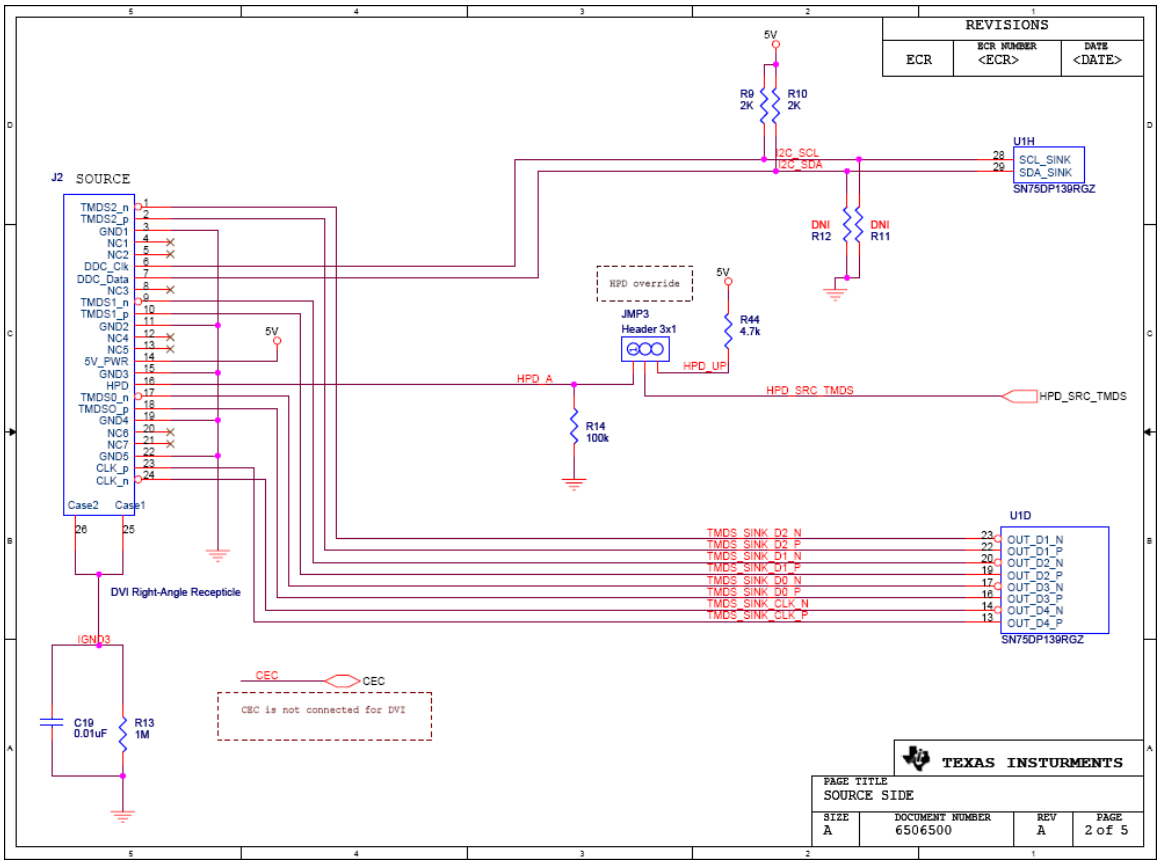

Figure 10. SN75DP139 EVM for DVI Schematic Page 2

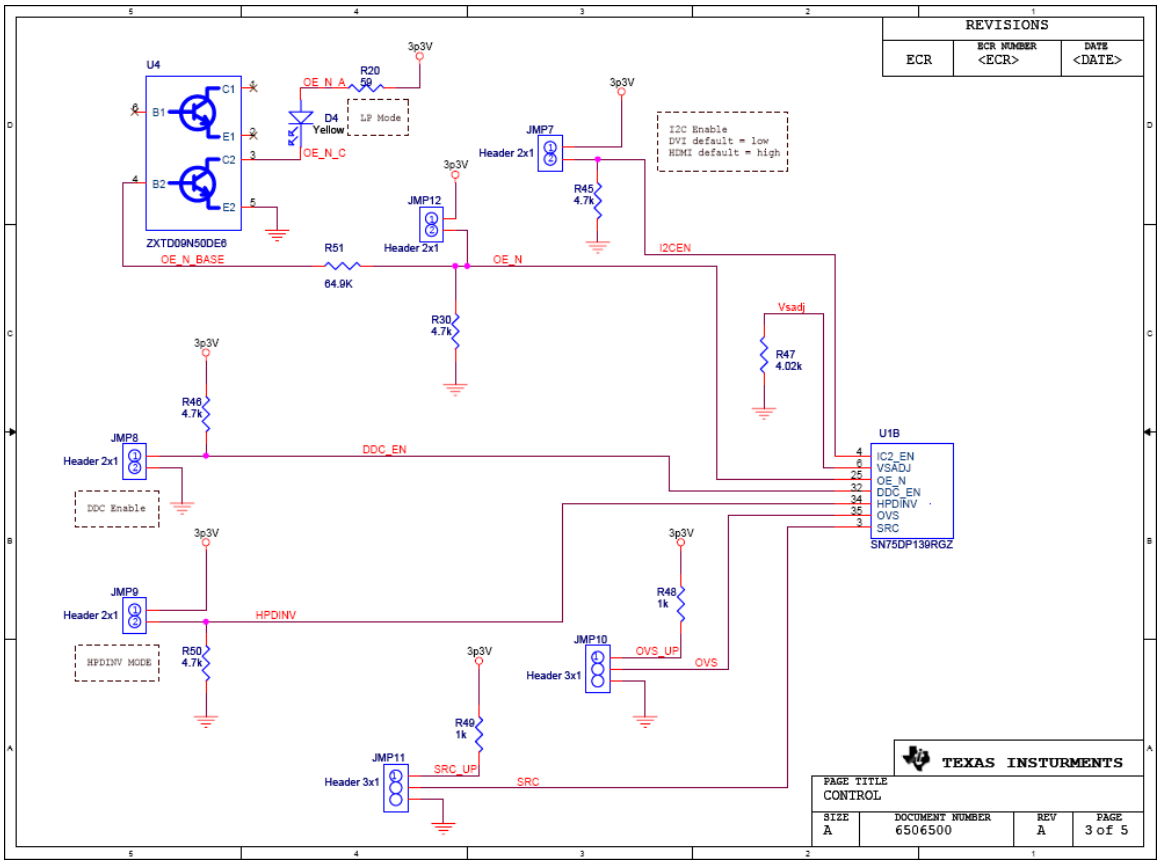

Figure 11. SN75DP139 EVM for DVI Schematic Page 3

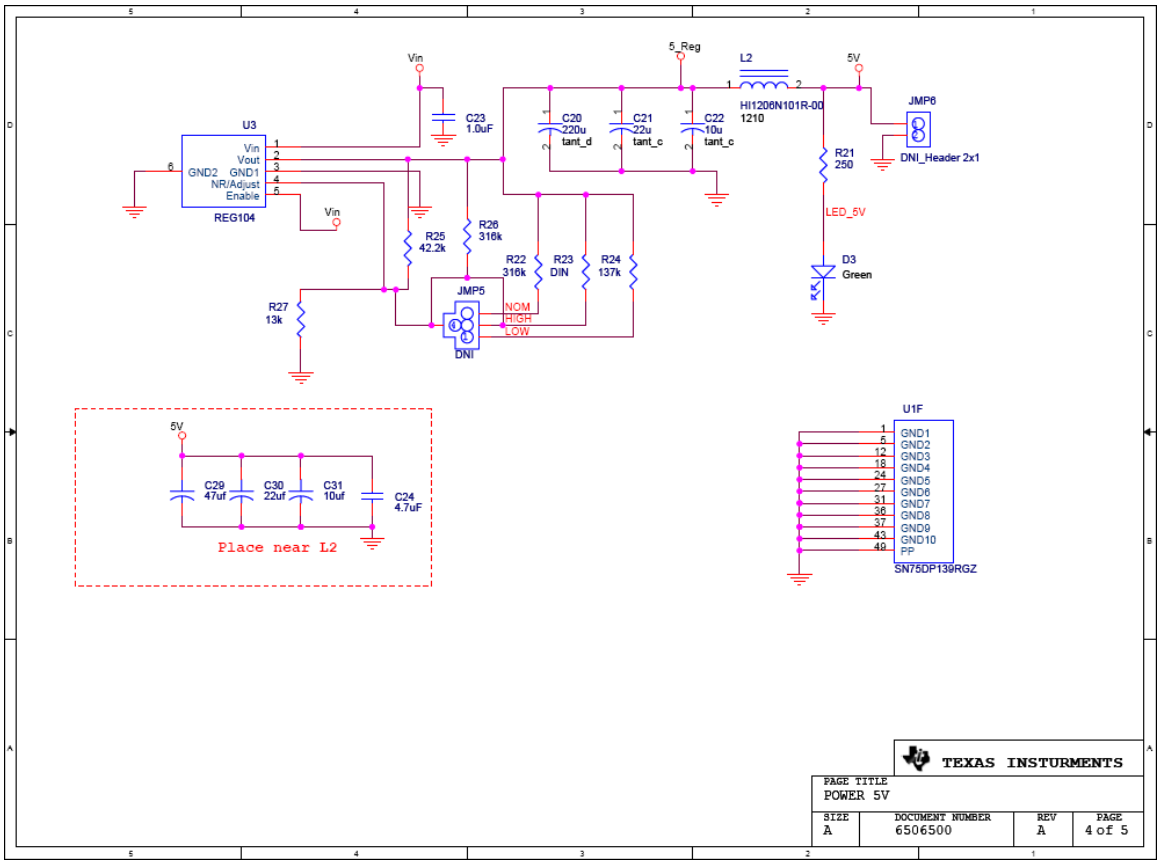

Figure 12. SN75DP139 EVM for DVI Schematic Page 4

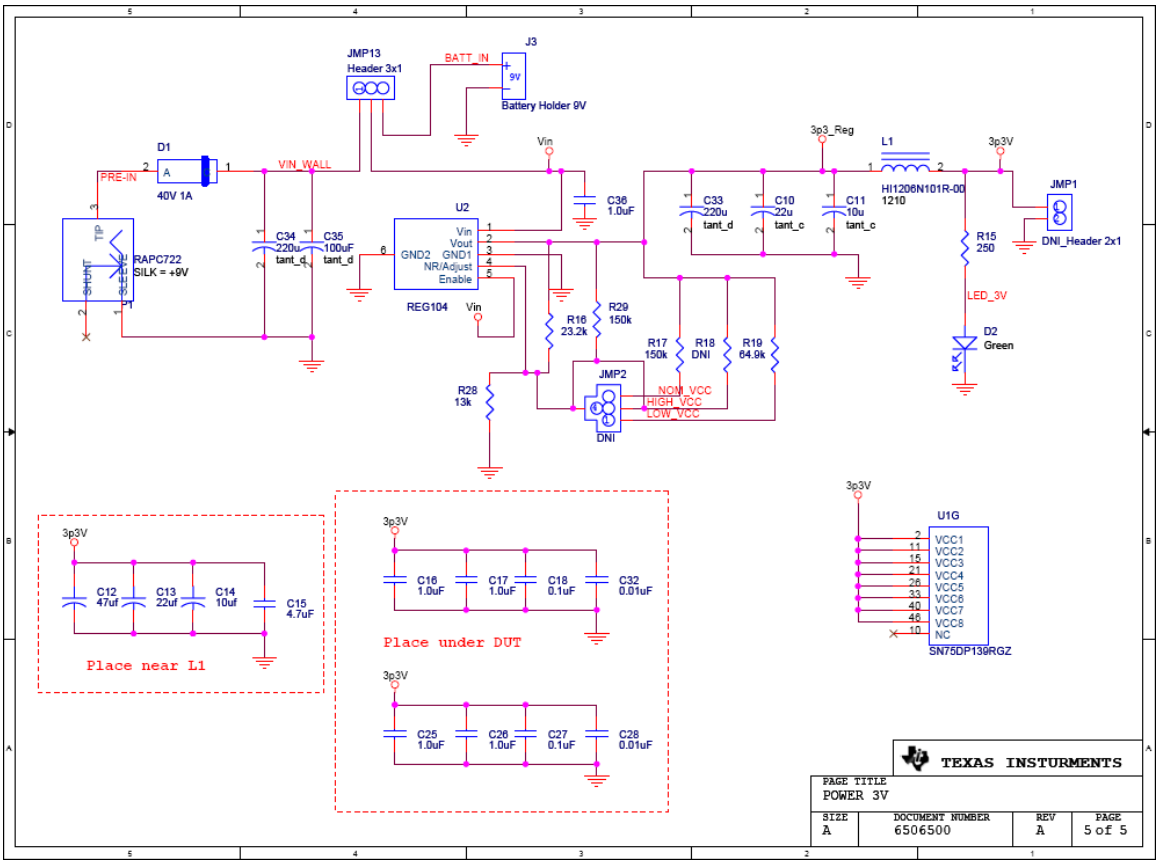

Figure 13. SN75DP139 EVM for DVI Schematic Page 5

SN75DP139 EVM Board Layout

This EVM was designed to show the implementation of this device on a 4-layer board.

The pin assignments of the input ports of the SN75DP139 device are optimized for the PCB mount DP connector. This allows easy routing of the input traces without the need for vias. The output port of the SN75DP139 device is optimized for a direct connection to a TMDS receiver. On this EVM the output port is routed to an HDMI or a DVI connector.

The board was designed to maintain 100 ohm differential impedance between each of the TMDS differential traces. For the material used in this design (FR4 – TurboClad 370), and with the stackup (shown below) this required the differential traces to be 12mil wide with an 11mil air gap between differential pairs. A minimum spacing of 3 times the trace width was maintained to all other components to prevent coupling.

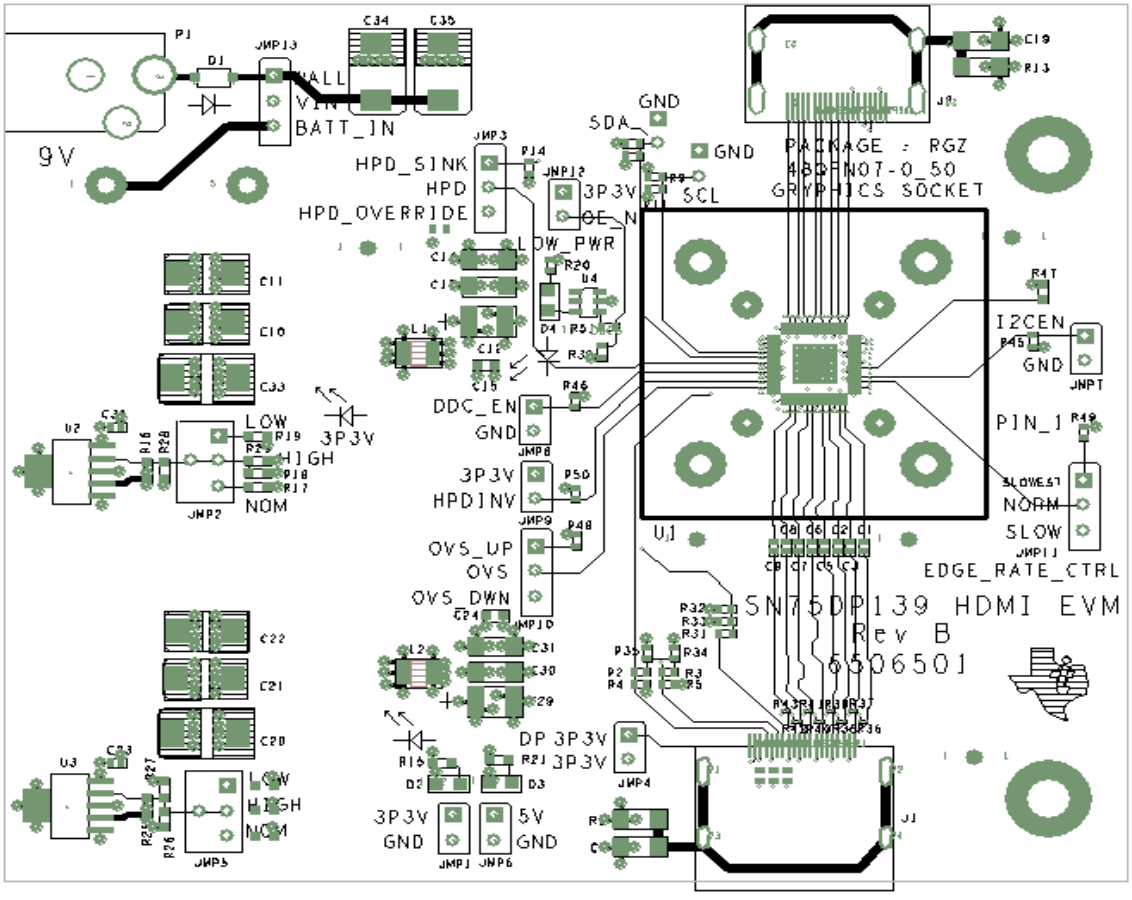

Figure 14. SN75DP139 EVM HDMI Top Layer 1

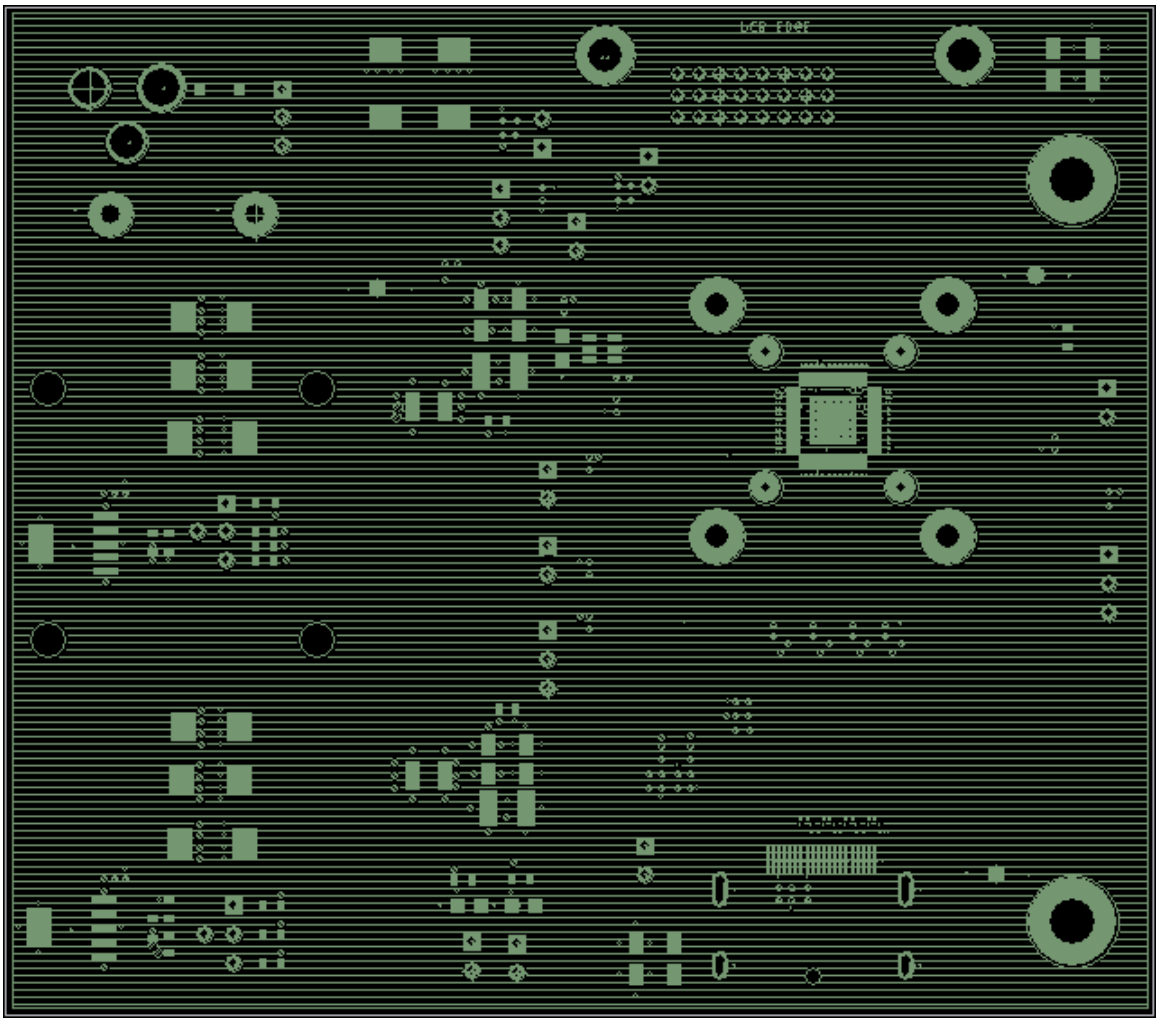

Figure 15. SN75DP139 EVM HDMI Ground Layer 2

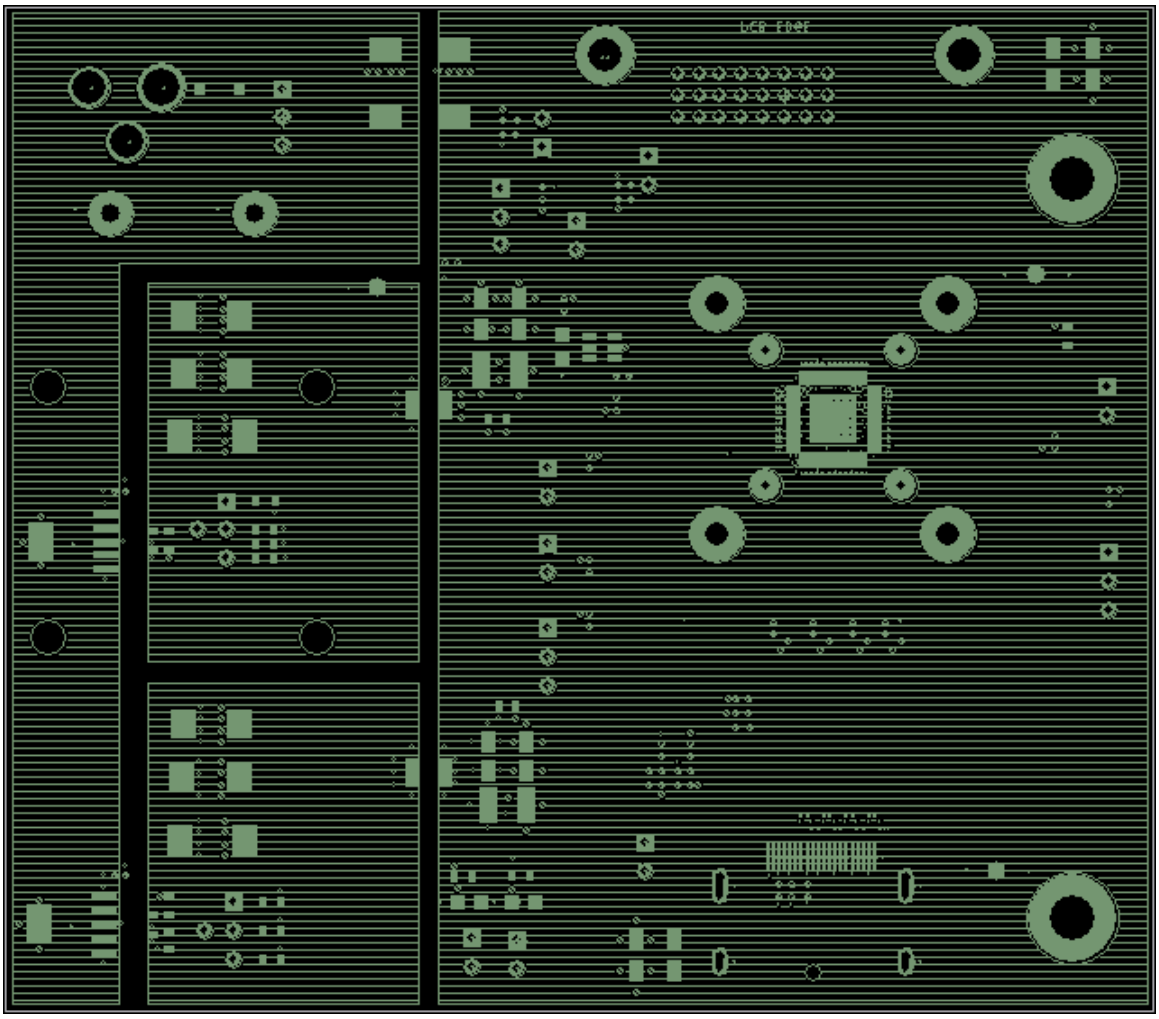

Figure 16. SN75DP139 EVM HDMI Power Layer 3

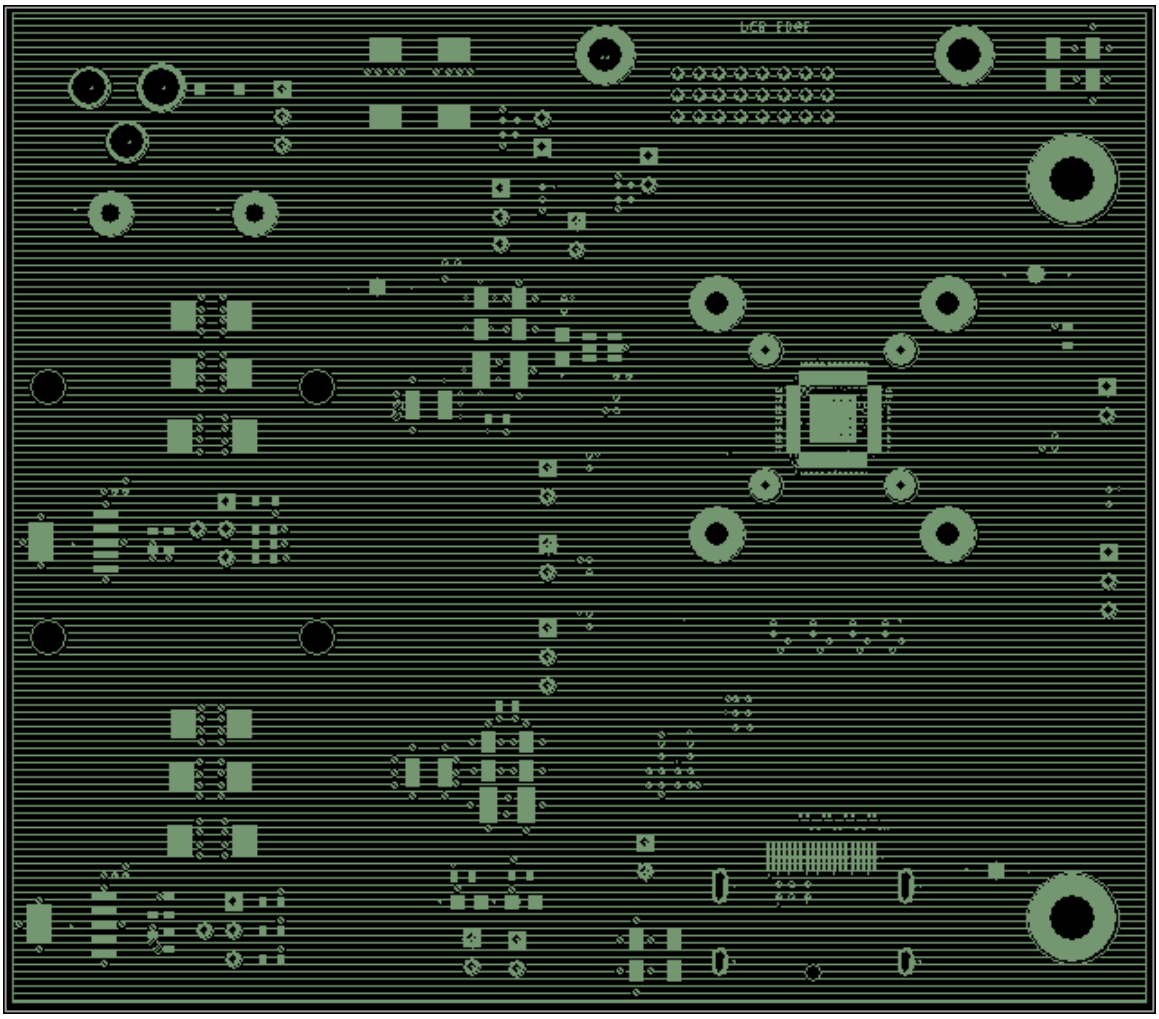

Figure 17. SN75DP139 EVM HDMI 3.3V Power Layer 4

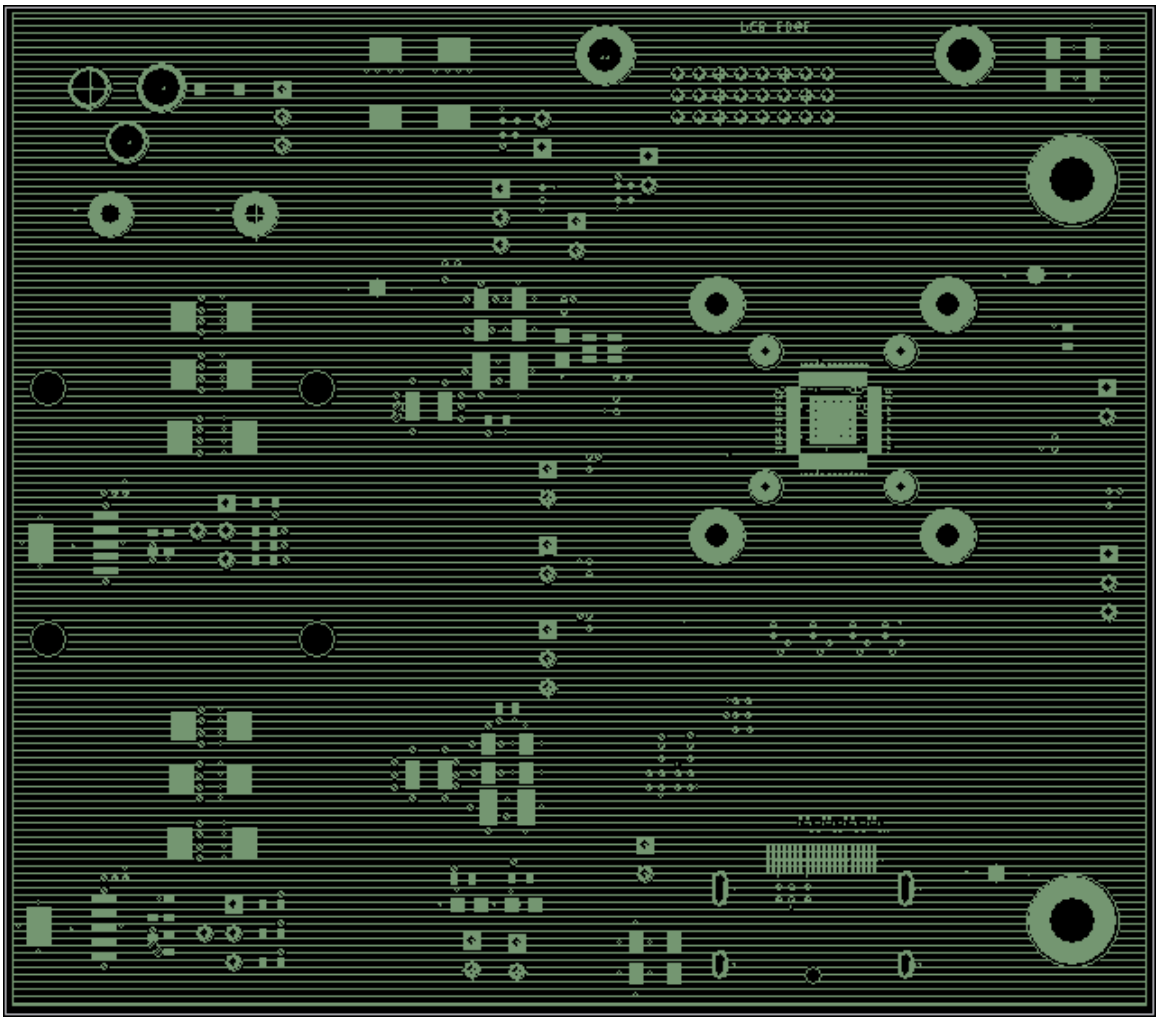

Figure 18. SN75DP139 EVM HDMI Ground Layer 5

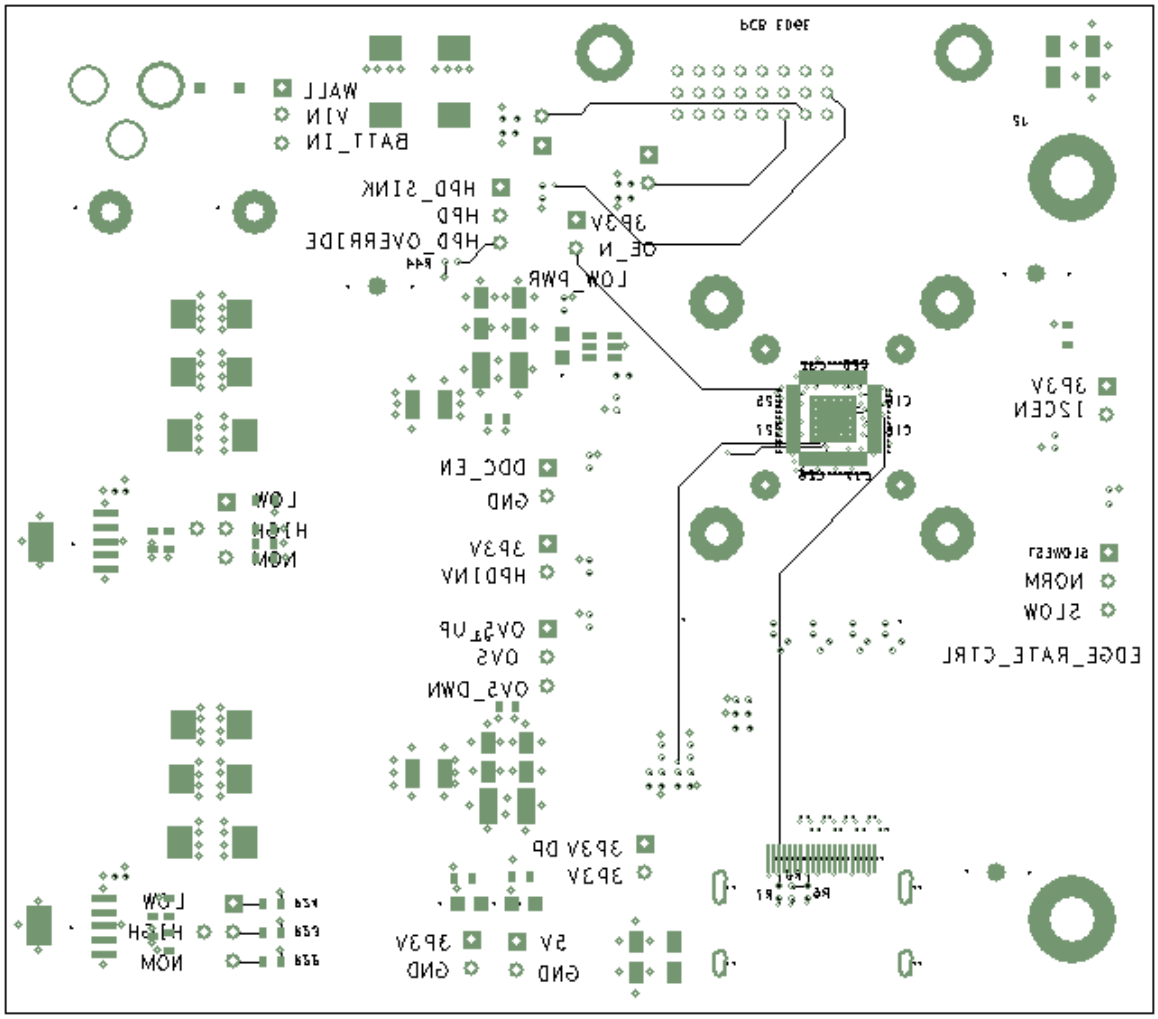

Figure 19. SN75DP139 EVM HDMI Bottom Layer 6

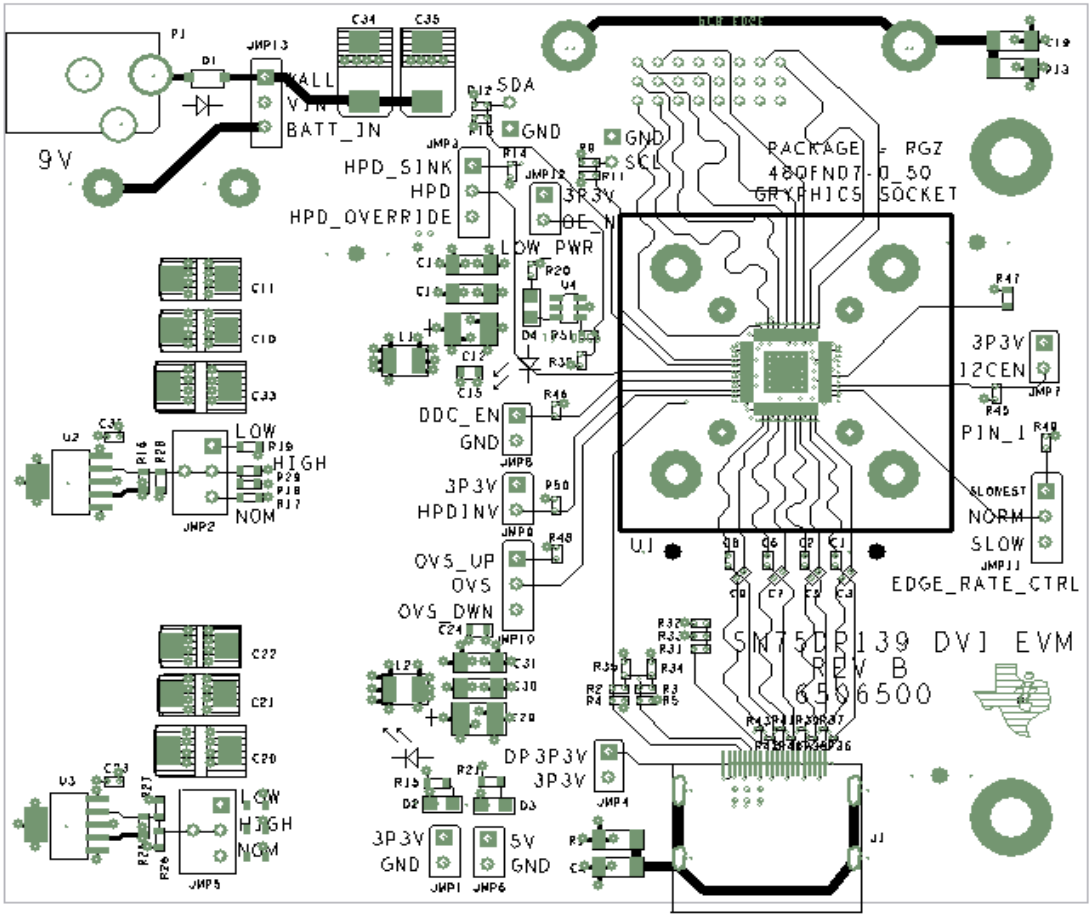

Figure 20. SN75DP139 EVM DVI Top Layer

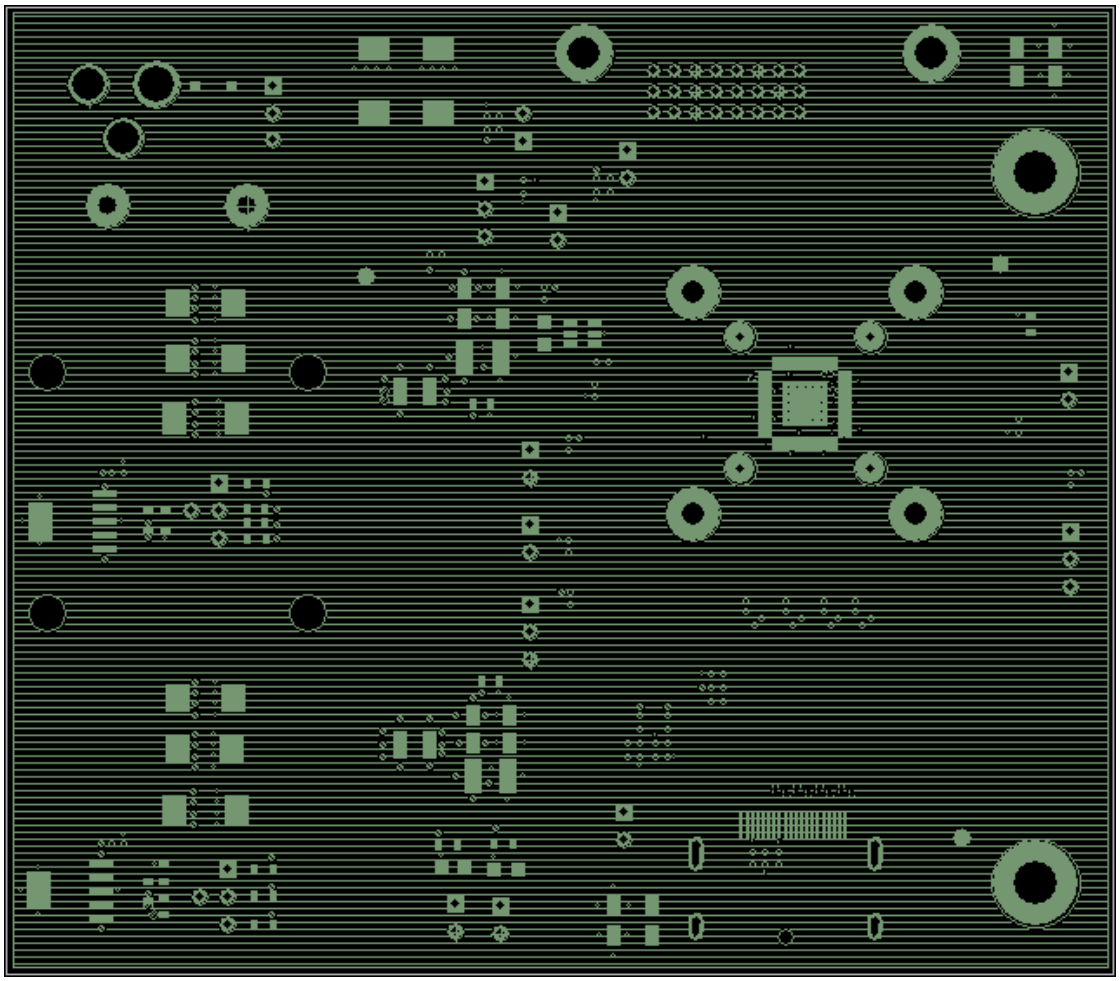

Figure 21. SN75DP139 EVM DVI Ground Layer 2

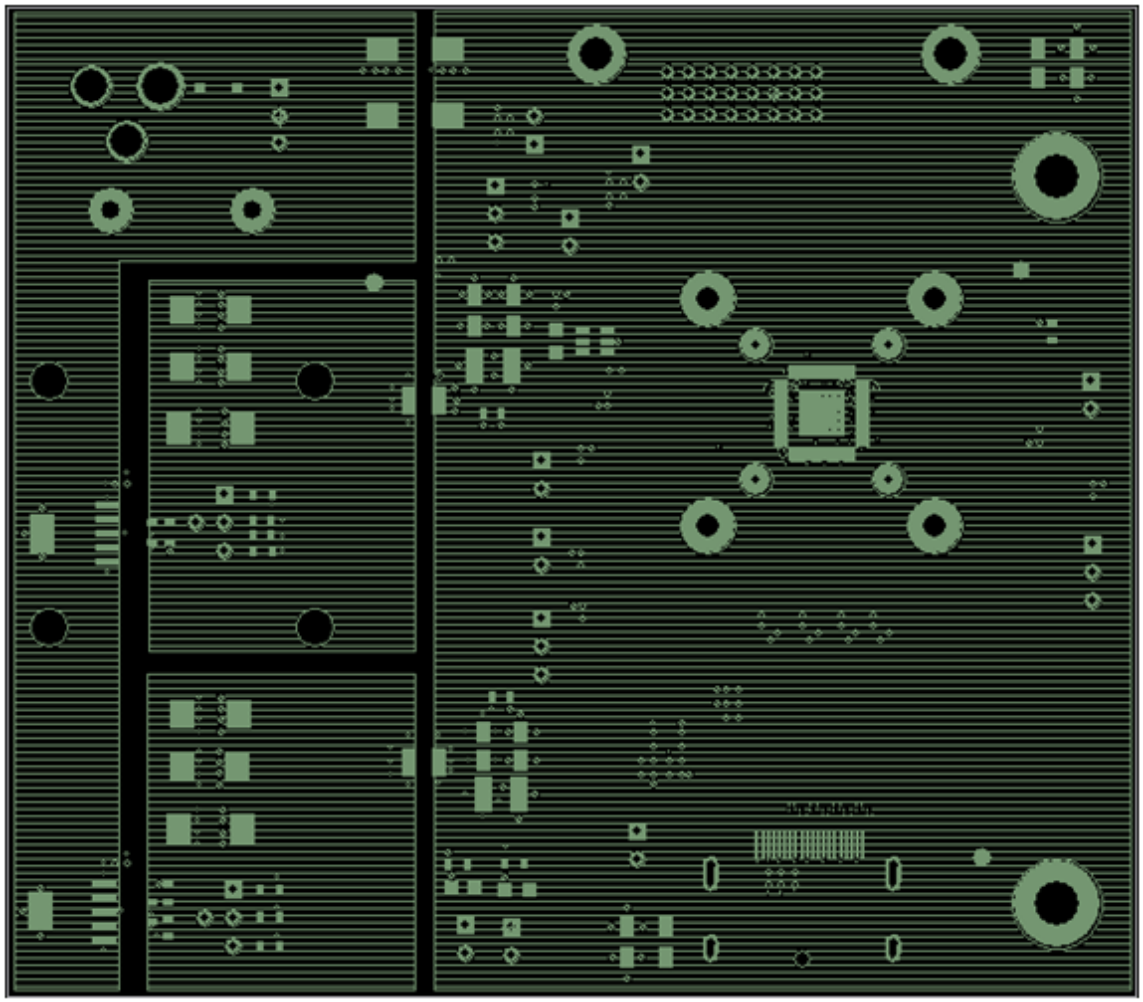

Figure 22. SN75DP139 EVM DVI Power Layer 3

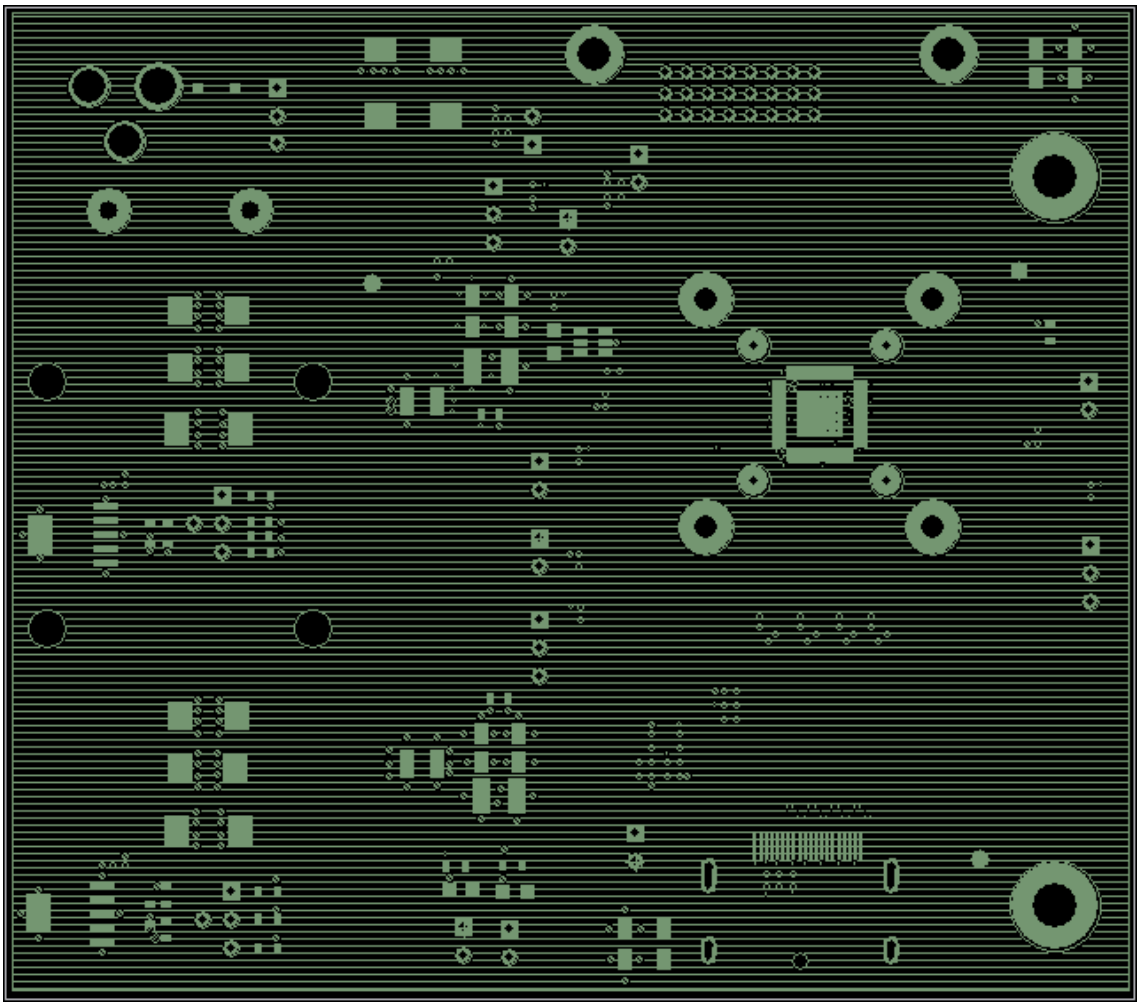

Figure 23. SN75DP139 EVM DVI 3.3V Power Layer 4

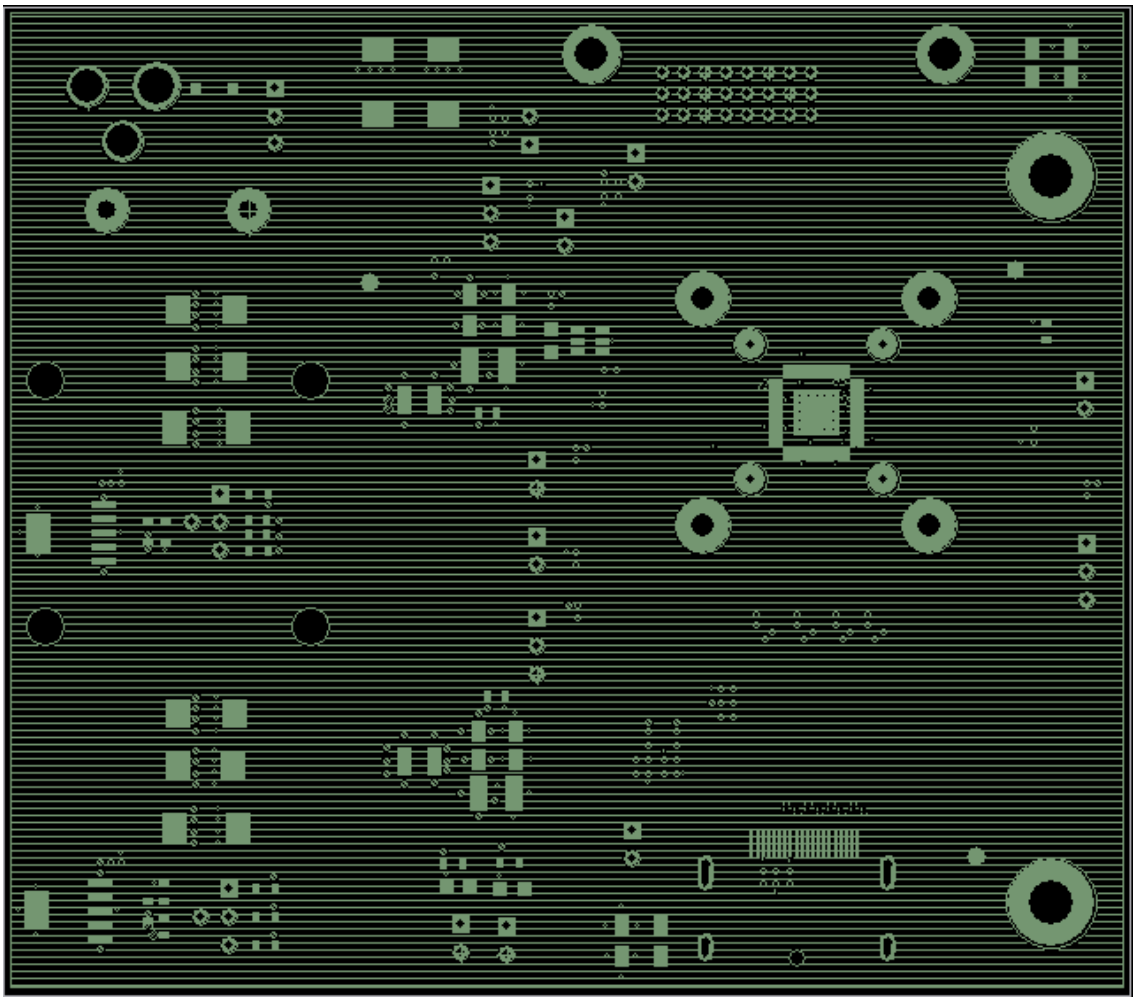

Figure 24. SN75DP139 EVM DVI Ground Layer 5

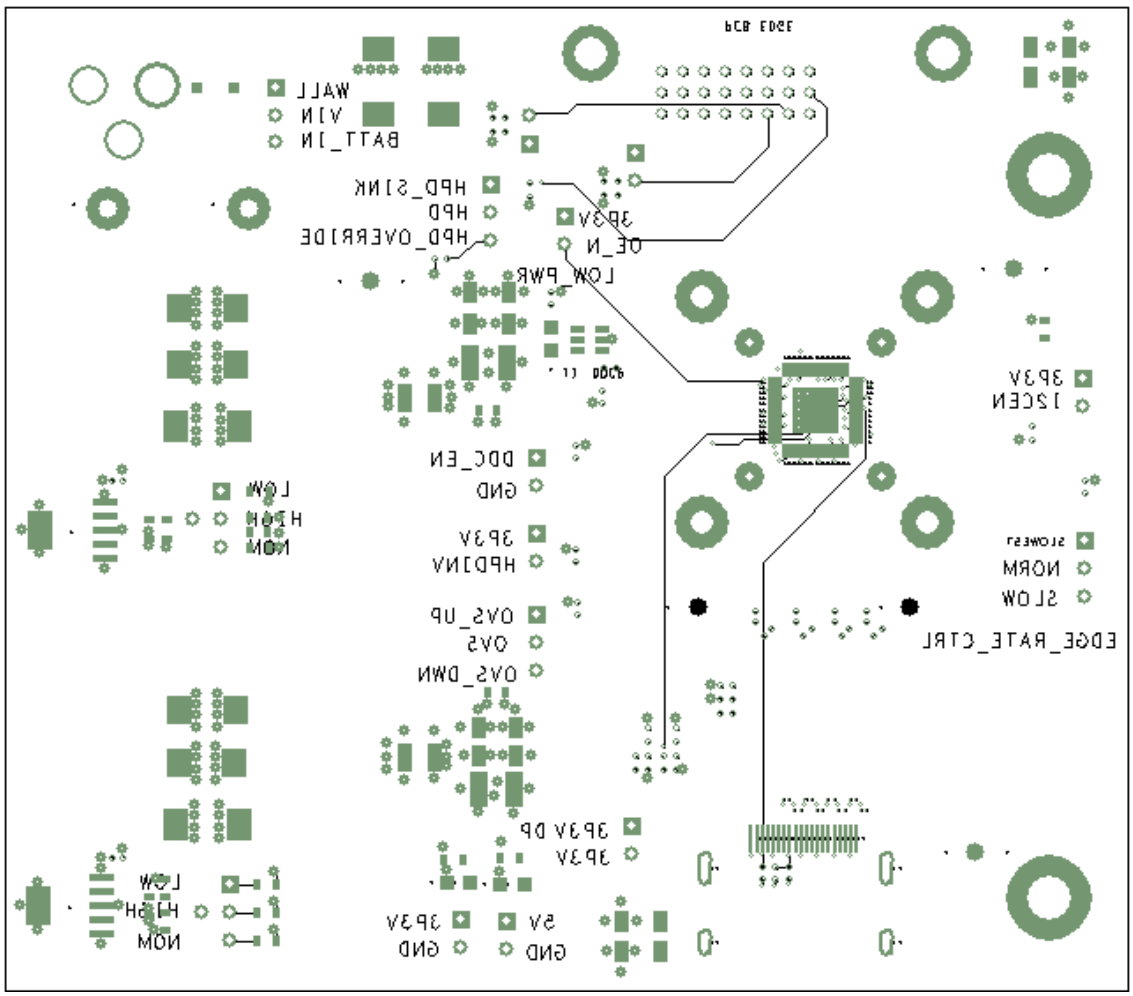

Figure 25. SN75DP139 EVM DVI Bottom Layer 6

SN75DP139 EVM Material Listing

The complete Bill of Material for the EVM is listed in Appendix A.

SN75DP139 EVM Board Construction

The EVM board is a 6-layer board constructed of FR4 – TurboClad 370 material. The board stackup consists of a signal layer on top, a ground layer, a power layer, power, ground, and a Signal layer on bottom.

Figure 26. EVM Layer Stack-up

Appendix A – Bill of Materials

Below is a table of the complete BOM for the EVM.

Item	Quantity	Reference	Value
1	10	C1,C2,C3,C5,C6,C7,C8,C9,C18,C27	0.1uF
2	2	C4,C19	0.01uF
3	2	C10,C21	22u
4	2	C11,C22	10u
5	2	C12,C29	47uf
6	2	C13,C30	22uf
7	2	C14,C31	10uf
8	2	C15,C24	4.7uF
9	6	C16,C17,C23,C25,C26,C36	1.0uF
10	3	C20,C33,C34	220u

11	2	C28,C32	0.01uF
12	1	C35	100uF
13	1	D1	40V 1A
14	2	D2,D3	HSMG-C170
15	1	D4	HSMY-C170
16	2	JMP1,JMP6	DNI_Header 2x1
17	2	JMP2,JMP5	DNI
18	4	JMP3,JMP10,JMP11,JMP13	Header 3x1
19	1	JMP4	Header 2x1 DNI
20	4	JMP7,JMP8,JMP9,JMP12	Header 2x1
21	1	J1	Display_Port_Connector_Sink
22	1	J2	Molex_HDMI
23	1	J3	Battery Holder 9V
24	2	L1,L2	HI1206N101R-00
25	1	P1	RAPC722
26	2	R1,R13	1M
27	4	R2,R3,R9,R10	2K
28	4	R4,R5,R11,R12	DNI
29	2	R6,R7	100k DNI
30	2	R8,R14	100k
31	2	R15,R21	250
32	1	R16	23.2k
33	2	R17,R29	150k
34	1	R18	DNI
35	1	R19	64.9k
36	1	R20	59
37	2	R22,R26	316k
38	1	R23	DIN
39	1	R24	137k
40	1	R25	42.2k
41	2	R27,R28	13k
42	5	R30,R44,R45,R46,R50	4.7k
43	2	R31,R34	0
44	2	R32,R35	0 DNI
45	1	R33	26k
46	8	R36,R37,R38,R39,R40,R41,R42,R43	DNI 50
47	1	R47	4.64k
48	2	R48,R49	1k
49	1	R51	64.9k
50	1	U1	SN75DP139RGZ
51	2	U2,U3	REG104
52	1	U4	ZXTD09N50DE6

Table 2. DP139 EVM HDMI Bill of Materials

Item	Quantity	Reference	Value
1	10	C1,C2,C3,C5,C6,C7,C8,C9,C18,C27	0.1uF
2	2	C4,C19	0.01uF
3	2	C10,C21	22u
4	2	C11,C22	10u
5	2	C12,C29	47uf
6	2	C13,C30	22uf
7	2	C14,C31	10uf
8	2	C15,C24	4.7uF
9	6	C16,C17,C23,C25,C26,C36	1.0uF
10	3	C20,C33,C34	220u
11	2	C28,C32	0.01uF
12	1	C35	100uF
13	1	D1	40V 1A
14	2	D2,D3	HSMG-C170
15	1	D4	HSMY-C170
16	2	JMP1,JMP6	DNI_Header 2x1
17	2	JMP2,JMP5	DNI
18	4	JMP3,JMP10,JMP11,JMP13	Header 3x1
19	1	JMP4	Header 2x1 DNI
20	4	JMP7,JMP8,JMP9,JMP12	Header 2x1
21	1	J1	Display_Port_Connector_Sink
22	1	J2	DVI Right-Angle Recepticle
23	1	J3	Battery Holder 9V
24	2	L1,L2	HI1206N101R-00
25	1	P1	RAPC722
26	2	R1,R13	1M
27	4	R2,R3,R9,R10	2K
28	4	R4,R5,R11,R12	DNI
29	2	R6,R7	100k DNI
30	2	R8,R14	100k
31	2	R15,R21	250
32	1	R16	23.2k
33	2	R17,R29	150k
34	1	R18	DNI
35	1	R19	64.9k
36	1	R20	59
37	2	R22,R26	316k
38	1	R23	DIN
39	1	R24	137k
40	1	R25	42.2k
41	2	R27,R28	13k
42	5	R30,R44,R45,R46,R50	4.7k

43	2	R31,R32	0 DNI	
44	1	R33	26k DNI	
45	1	R34		0
46	1	R35	DNI 0	
47	8	R36,R37,R38,R39,R40,R41,R42,R43	DNI 50	
48	1	R47	4.64k	
49	2	R48,R49	1k	
50	1	R51	64.9K	
51	1	U1	SN75DP139RGZ	
52	2	U2,U3	REG104	
53	1	U4	ZXTD09N50DE6	

Table 3. DP139 EVM DVI Bill of Materials