Schematic Review Form

SN75DP159

Pin #	Name	Info	Violations	*Description*
2[RGZ] 1[RSB]	IN_D2p	ok		Channel 2 differential input
3[RGZ] 3[RSB]	IN_D2n	typo -> 2[RSB] ok		Channel 2 differential input
5[RGZ] 4[RSB]	IN_D1p	ok		Channel 1 differential input
6[RGZ] 5[RSB]	IN_D1n	ok		Channel 1 differential input
8[RGZ] 6[RSB]	IN_D0p	ok		Channel 0 differential input
9[RGZ] 7[RSB]	IN_D0n	ok		Channel 0 differential input
11[RGZ] 9[RSB]	IN_CLKp	ok		Clock differential input
12[RGZ] 10[RSB]	IN_CLKn	ok		Clock differential input

34[RGZ] 29[RSB]	OUT_D2n	ok		TMDS data 2 differential output
35[RGZ] 30[RSB]	OUT_D2p	ok		TMDS data 2 differential output
31[RGZ] 26[RSB]	OUT_D1n	ok		TMDS data 1 differential output
32[RGZ] 27[RSB]	OUT_D1p	ok		TMDS data 1 differential output
28[RGZ] 24[RSB]	OUT_D0n	ok		TMDS data 0 differential output
29[RGZ] 25[RSB]	OUT_D0p	ok		TMDS data 0 differential output
25[RGZ] 21[RSB]	OUT_CLKn	ok		TMDS data clock differential output
26[RGZ] 22[RSB]	OUT_CLKp	ok		TMDS data clock differential output
4[RGZ] 3[RSB]	HPD_SRC	ok		Hot plug detect output
33[RGZ] 28[RSB]	HPD_SNK	ok		Hot plug detect input

45[RGZ]	AUX_SRCp	no DisplayPort so should be ok		Source side bidirectional DisplayPort auxiliary for I2C-over-AUX (DP159RGZ only)
44[RGZ]	AUX_SRCn	no DisplayPort so should be ok		Source side bidirectional DisplayPort auxiliary for I2C-over-AUX (DP159RGZ only)
47[RGZ] 39[RSB]	SDA_SRC	ok		Source side TMDS port bidirectional DDC data line
46[RGZ] 38[RSB]	SCL_SRC	ok		Source side TMDS port bidirectional DDC data line
39[RGZ] 33[RSB]	SDA_SNK	ok		Sink side TMDS port bidirectional DDC data lines
38[RGZ] 32[RSB]	SCL_SNK	ok		Sink side TMDS port bidirectional DDC data lines
42[RGZ] 36[RSB]	OE	ok		Operation enable/reset pin OE = L: Power-down mode OE = H: Normal operation Internal weak pullup: Resets device when transitions from H to L
17[RGZ]	NC	ok		NC
18[RGZ]	CEC_EN	ok		CEC control pin for Dongle applications

40[RGZ] 34[RSB]	SLEW_CTL	ok		Slew rate control when I2C_EN/PIN = Low. SLEW_CTL = H, fastest data rate SLEW_CTL = L, 5 ps slow SLEW_CTL = No Connect, 10 ps slow When I2C_EN/PIN = High Slew rate is controlled through I2C[4]
20[RGZ] 16[RSB]	PRE_SEL	ok		De-emphasis pin strap when I2C_EN/PIN = Low. PRE_SEL = L: - 2 dB de-emphasis PRE_SEL = No Connect: 0 dB PRE_SEL = H: Reserved
21[RGZ] 17[RSB]	EQ_SEL/A0	ok		Input Receive Equalization pin strap when I2C_EN/PIN = Low EQ_SEL = L: Fixed EQ at 7.5 dB EQ_SEL = No Connect: Adaptive EQ EQ_SEL = H: Fixed at 14 dB When I2C_EN/PIN = High Address bit 1 Note: (3 level for pin strap programming but 2 level when I2C[4] address)
10[RGZ] 8[RSB]	I2C_EN/PIN	ignore		I2C_EN/PIN = High; puts device into I 2C control mode I2C_EN/PIN = Low; puts device into pin strap mode
15[RGZ] 13[RSB]	I2C_EN/PIN	ignore		I2C_EN/PIN = High; puts device into I 2C control mode I2C_EN/PIN = Low; puts device into pin strap mode
10[RGZ] 8[RSB]	I2C_EN/PIN	ok		I2C_EN/PIN = High; puts device into I 2C control mode I2C_EN/PIN = Low; puts device into pin strap mode

15[RGZ] 13[RSB]	SCL_CTL		are these pins in use?	I2C clock signal Note: When I2C_EN/PIN = Low Pin strapping take priority and those functions cannot be changed by I2C
16[RGZ] 14[RSB]	SDA_CTL		are these pins in use?	I2C data signal Note: When I2C_EN/PIN = Low Pin strapping take priority and those functions cannot be changed by I2C
27[RGZ] 23[RSB]	~HDMI_SEL/A1	ok		HDMI_SEL when I2C_EN/PIN = Low HDMI_SEL = High: Device configured for DVI HDMI_SEL = Low: Device configured for HDMI (Adaptor ID block is readable through I2C[4] or I2C-over-AUX. When I2C_EN/PIN = High Address bit 2 Note: Weak internal pull down
36[RGZ]	TX_TERM_CTL	ok		Transmit Termination Control when I2C_EN/PIN = Low TX_TERM_CTL = H, No transmit termination TX_TERM_CTL = L, Transmit termination impedance in 75 to about 150 Ω TX_TERM_CTL = No Connect, automatically selects the termination impedance Data rate (DR) > 3.4 Gbps – 75- to 150-Ω differential near end termination 2 Gbps < DR < 3.4 Gbps – 150- to 300-Ω differential near end termination DR < 2 Gbps – no termination

				Note: If left floating will be in automatic select mode.
1[RGZ]	SWAP/POL	ok		Input lane SWAP and polarity control pin when I2C_EN/PIN = Low SWAP/POL = H receive lane polarity swap (retimer mode only) SWAP/POL = L receive lanes swap (retimer and redriver mode) SWAP/POL = No Connect normal working
13,43[RGZ] 11,37[RSB]	VCC	may need small cap to filter high frequency noise		3.3-V power supply
14,23,24,37,48[RGZ] 12,19,20,31,40[RSB]	VDD	ok		1.1-V power supply
7,19,41,30[RGZ] 15,35[RSB]	GND	ok		Ground
Pad	Pad	ok		Connected to ground

Comments

ESD should be ok but please double check the CMC circuitry