Schematic Review Form

SN75LVPE5412/21 U36, U37, U38, U39

Pin #	Name	Info	Violations	*Description*
41	MODE	1k to GND. Pin mode selected.		*Type: Input, 5-level* Sets device control configuration modes. 5-level IO pin as provided in SN75LVPE5412 data sheet Table 6-1. The pin can be exercised at device power up or in normal operation mode. L0: **Pin mode** - device control configuration is done solely by strap pins. L1 or L2: **SMBus/I^{2}C mode** - device control configuration is done by an external controller with SMBus/I^{2}C primary. This pin along with ADDR pin sets device's secondary address. L3 and L4 (Float): RESERVED - TI internal test modes.
40	EQ0 / ADDR	1k to GND.		*Type: Input, 5-level* In **Pin Mode**: The EQ0 and EQ1 pins set receiver linear equalization CTLE (AC gain) for all channels according to data sheet Table 6-2. These pins are sampled at device power-up only. In **SMBus/I^{2}C Mode**: The ADDR pin in conjunction with MODE pin sets SMBus/I^{2}C secondary address according to data sheet Table 6-5. The pin is sampled at device power-up only.
20	EQ1	1k to GND. EQ index 0 selected. EQ setting can be modified with different resistor values.		*Type: Input, 5-level* In **Pin Mode**: The EQ0 and EQ1 pins set receiver linear equalization CTLE (AC gain) for all channels according to data sheet Table 6-2. These pins are sampled at device power-up only. In **SMBus/I^{2}C Mode**: This pin has no effect.
1	GAIN / SDA	1k to GND. -6dB gain selected. Gain setting can be modified with different resistor values.	TI recommends using 0dB gain setting for most applications. 0dB gain can be selected by leaving the GAIN pin floating.	*Type: Input, 5-level or Input/Output* In **Pin Mode**: Flat gain (broadband gain – DC and AC) from the input to the output of the device for all channels. **Note**: The device also provides AC (high frequency) gain in the form of equalization controlled by EQx pins or SMBus/I^{2}C registers. The pin is sampled at device power-up only.

				In **SMBus/I^{2}C Mode**: 3.3V SMBus/I^{2}C data. External pullup resistor such as 4.7 kΩ required for operation.
18	PD	PD pins of all 4 devices shorted together. Diode logic implemented with PEG slot and PCIE slot RST_N signals.	Please review the logic on the PD pin as it doesn't quite make sense to me. Typically we recommend using the PERST# and PRSNT# signals to control the PD pin logic. Please refer to the "PD pin controls cases" slide.	*Type: Input, 3.3V LVCMOS* 2-level logic controlling the operating state of the redriver. Active in **both Pin Mode and SMBus/I^{2}C Mode**. The pin is used part of PCIe RX_DET state machine as outlined in data sheet Table 6-4. High: power down for all channels. Low: power up, normal operation for all channels.
42	RX_DET / SCL	1k to GND. Impedance is always 50-ohm. RX-Detect setting can be modified with different resistor values.	TI recommends using option L4 (leave the RX_DET pin floating) for most applications.	*Type: Input, 5-level or Input/Output* In **Pin Mode**: Sets receiver detect state machine options according to data sheet Table 6-4. The pin is sampled at device power-up only. In **SMBus/I^{2}C Mode**: 3.3V SMBus/I^{2}C clock. External pullup resistor such as 4.7 kΩ required for operation.
17	SEL	SEL pins of all 4 devices shorted together. Logic implemented with PEG slot RST_N signal.	Please review the logic on the SEL pin as it doesn't quite make sense to me.	*Type: Input, 3.3V LVCMOS* Selects the mux path. Active in both Pin Mode and SMBus/I^{2}C Mode. The pin has a weak internal pull-down resistor. **Note**: the SEL pin must be exercised in system implementations for mux selection between Port A vs Port B. The pin is used for PCIe RX_DET state machine as outlined in data sheet Table 6-4. Low: Port A selected. High: Port B selected.
3, 4, 7, 8, 10, 11, 14, 15	5412: RXnP, RXnN 5421: TXnP, TXnN	5412: Signals transmitted from motherboard. 5421: Signals route to motherboard connector with 224pF AC coupling caps.	5412: Please confirm high-speed signals are AC coupled on the motherboard before passing through the connector and reaching the redriver. 5421: 220nF AC coupling capacitors are recommended for PCIe 3.0, 4.0, 5.0.	**5412:** *Type: Differential Input* Non-inverting and inverting differential RX input, Channels 0-3. Please refer to data sheet section 7.2.1.1 for further design requirements. **5421:** *Type: Differential Output* Non-inverting and inverting differential TX output, Channels 0-3. 220nF AC coupling capacitors of maximum size 0402 are recommended at each device TXN and TXP output. Please refer to data sheet section 7.2.1.1 for further design requirements.
24, 25, 28, 29, 33, 34,	5412: TXAnP,	5412: Signals route to PCIE slot with 224pF AC	5412: 220nF AC coupling capacitors are	**5412:** *Type: Differential Output*

37, 38	TXAnN 5421: RXAnP, RXAnN	coupling caps. 5421: Signals transmitted from PCIE slot.	recommended for PCIe 3.0, 4.0, 5.0. 5421: Please confirm high-speed signals are AC coupled on the endpoint before passing through the connector and reaching the redriver.	Non-inverting and inverting differential TX output, Port A, Channels 0-3. 220nF AC coupling capacitors of maximum size 0402 are recommended at each device TXN and TXP output. Please refer to data sheet section 7.2.1.1 for further design requirements. **5421:** *Type: Differential Input* Non-inverting and inverting differential RX input, Port A, Channels 0-3. Please refer to data sheet section 7.2.1.1 for further design requirements.
22, 23, 26, 27, 31, 32, 35, 36	5412: TXBnP, TXBnN 5421: RXBnP, RXBnN	5412: Signals route to PEG slot with 224pF AC coupling caps. 5421: Signals transmitted from PEG slot.	5412: 220nF AC coupling capacitors are recommended for PCIe 3.0, 4.0, 5.0. 5421: Please confirm high-speed signals are AC coupled on the endpoint before passing through the connector and reaching the redriver.	**5412:** *Type: Differential Output* Non-inverting and inverting differential TX output, Port B, Channels 0-3. 220nF AC coupling capacitors of maximum size 0402 are recommended at each device TXN and TXP output. Please refer to data sheet section 7.2.1.1 for further design requirements. **5421:** *Type: Differential Input* Non-inverting and inverting differential RX input, Port B, Channels 0-3. Please refer to data sheet section 7.2.1.1 for further design requirements.
5, 13	VCC	4 pcs 106pF, 6 pcs 105pF decoupling caps used for all 4 devices.	TI recommends following the decoupling scheme provided in the datasheet: a 0.1uF capacitor per VCC pin, a 1.0uF bulk capacitor per device, and a 10uF bulk capacitor per power bus.	*Type: Power* Power supply, VCC = 3.3V ± 10%. The VCC pins on this device should be connected through a low-resistance path to the board VCC plane. Refer to data sheet Section 7.3 for power supply recommendations.
EP, 6, 9, 16, 21, 30, 39	GND	looks good		*Type: Ground* Ground reference for the device. EP: the Exposed Pad at the bottom of the QFN package. It is used as the GND return for the device. The EP should be connected to one or more ground planes through the low resistance path. A via array provides a low impedance path to GND. The EP also improves thermal dissipation.
19	TEST	Labeled RSVD1 on schematic. Left floating.		TI internal test pin. Leave unconnected.
2, 12	RSVD1, 2	Labeled RSVD2, RSVD3 on schematic. Connected to	TI recommends either directly connecting these	Reserved pins. For best signal integrity performance connect the pins to GND. Alternate option would be 0Ω

		104pF capacitor to GND.	pins to GND or shorting through 0 ohm resistors to GND for best signal integrity performance.	resistors from pins to GND.

Comments