SNxxLVDS82-83-93-94 FlatLink™ Transmitter and Receiver Evaluation Module (EVM) User's Guide

ABOUT THIS MANUAL

The Texas Instruments SNxxLVDS82-83-93-94 FlatLink™ Evaluation Module (EVM) board is used to evaluate a pair of LVDS83 and LVDS82 or LVDS93 and LVDS94 receiver and transmitter devices (56 pin TSSOP) for point-to-point data transmission application. The transmitter and receiver pair serializes 28 LVTTL bits into 4 LVDS channel and vice versa. The board enables the system designer to connect 50Ω parallel buses to both transmitter and receiver connectors. Using the internal 7x clock PLL, the transmitter (LVDS83 or LVDS93) portion of the board serializes and transmits data along the four differential pair lines. The receiver (LVDS82 or LVDS94) portion of the board de-serializes and presents data on the parallel bus. The high speed serial data lines (up to 476Mbps per line or 1.904Gbps total throughput) interface to four 50Ω controlled impedance SMA connectors.

WARNING

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at own expense will be required to take whatever measures may be required to correct this interference.

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Introduction

The Texas Instruments (TI™) SNxxLVDS82-83-93-94 FlatLink™ Evaluation Module (EVM) board is used to evaluate a pair of LVDS83 and LVDS82 or LVDS93 and LVDS94 transmitter and receiver devices (56 pin TSSOP). The transmitter and receiver pair serializes 28 LVTTL bits into 4 LVDS channel and vice versa. The board enables the designer to connect 50Ω parallel buses to both the transmitter and receiver parallel connectors. Using the internal 7x clock PLL, the transmitter (LVDS83 or LVDS93) portion of the board serializes and transmits data along the four differential pair lines. The receiver (LVDS82 or LVDS94) portion of the board de-serializes and presents data on the parallel bus. The high speed serial data lines (up to 476Mbps per line or 1.904Gbps total throughput) interface to four 50Ω controlled impedance SMA connectors.

Flexibility has been designed into the EVM so the receiver and transmitter ICs on the EVM can be replaced by similar pin-to-pin compatible receiver and transmitter ICs of the same FlatLink family. The SNxxLVDS82-83-93-94 EVM supports 4 LVDS channels to 28 LVTTL bits transmitter and receivers. Specifically, it includes SN75LVDS83 and SN75LVDS82 as its default transmitter and receiver. Moreover, the default ICs on the EVM can be replaced by SN65LVDS93 and SN65LVDS94 transmitter and receiver (PLL input of 20MHz to 68MHz and temperature range of -40°C to 85°C), which operate at wider bandwidth and wider temperature range than the SN75LVDS83 and SN75LVDS82 transmitter and receiver (PLL input of 31MHz to 68MHz and temperature range of 0°C to 70°C).

As the frequency of operation increases, the board designer must take special care to ensure that the highest signal integrity is maintained. To achieve this, the board's impedance is controlled to 50Ω for both the high-speed differential serial and parallel data connections. In addition, board impedance mismatches are reduced by designing the component pad size to be as close as possible to the width of the connecting transmission lines. Vias are minimized and, when necessary, placed as close as possible to the device transmitters. Since the board contains both serial and parallel transmission lines, care was taken to control both impedance and trace-length mismatch (board skew) to less than +/- 1 MIL.

Overall, the board layout is designed and optimized to support high-speed operation. Thus, understanding impedance control and transmission-line effects is crucial when designing a high-speed board.

Some of the advanced features offered by this board include:

- PCB (printed-circuit board) is designed for high-speed signal integrity.
- SMA and parallel fixtures are easily connected to test equipment.
- All input/output signals are accessible for rapid prototyping.
- Device and signal power planes can be supplied through separate banana jacks for isolation, or can be combined by placing jumpers on the supplied header pins.

SNxxLVDS82-83-93-94 EVM Kit Contents

The SNxxLVDS82-83-93-94 EVM kit contains the following:

- SNxxLVDS82-83-93-94 EVM board
- SNxxLVDS82-83-93-94 EVM User's Guide (this document)

SNxxLVDS82-83-93-94 EVM Board Configuration

The SNxxLVDS82-83-93-94 EVM board gives the developer various options for operation, many of which are jumper-selectable. Other options can be either soldered into the EVM or connected through input connectors.

The EVM has been designed with the receiver section on the left side of the board and the transmitter section on the right side of the board. The installed LVDS receiver is designated U1, while the installed LVDS transmitter is designated U2. The EVM, as delivered, incorporate 100Ω termination resistors to the LVDS inputs and clock input of the receiver. The termination resistors are R5 through R9 for the SNxxLVDS82-83-93-94 EVM

Jumper 1 through Jumper 4 on the SNxxLVDS82-83-93-94 EVM (see **Figure 1**) are 4x7 headers that contains ground pins, receiver data output pins, transmitter data input pins, and ground pins, counted column-wise from left to right. They allow the user to do a loop-through test by placing jumpers on the “DATA” pins of the header. This connects the LVTTL outputs (both data and clock-out) of the receiver to the LVTTL inputs (both data and clock-in) of the transmitter. Jumper 5 is a 4x1 (see **Figure 1**) header that contains ground pin, receiver clock-out pin, transmitter clock-in pin, and ground pin. The header not only serves as individual test points for the LVTTL receiver outputs, but it also serves as individual input points for the LVTTL driver inputs.

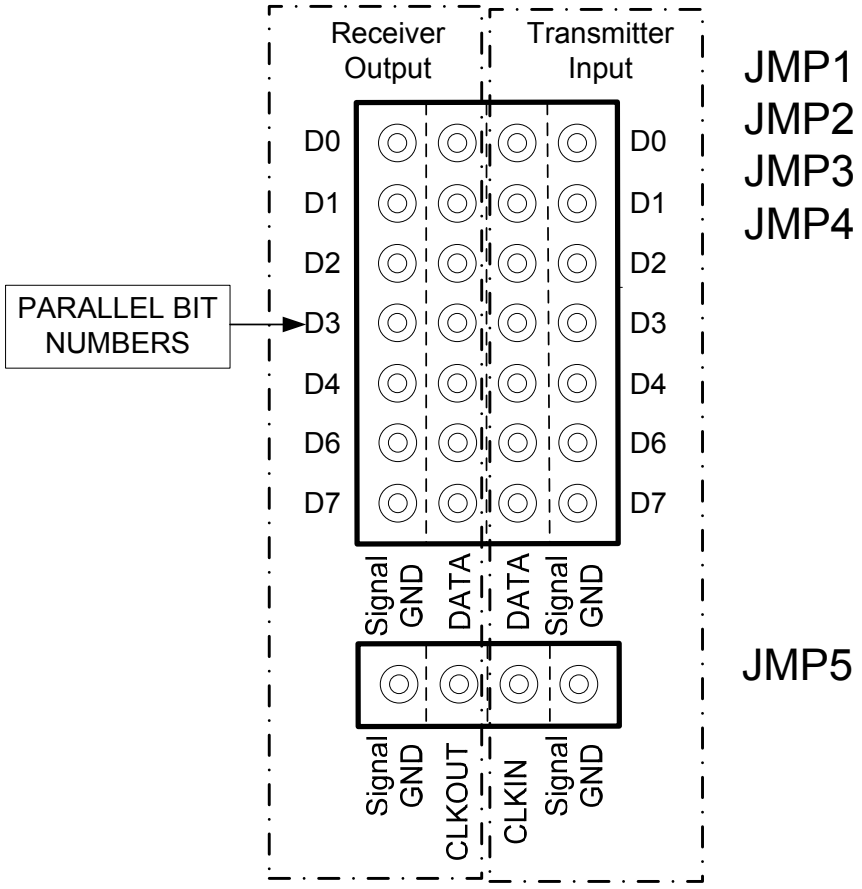

Figure 1. Parallel Signal Header Block

Parallel Loop-back, shown in **Figure 2**, can be easily implemented by placing jumper pins on the RD/TD pins of the header.

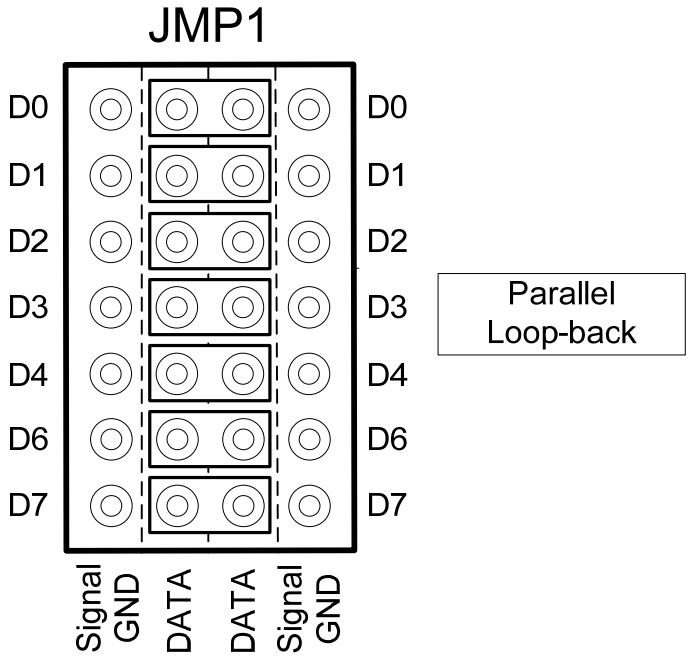

Figure 2. Parallel Loopback Configuration

Jumper 6 through Jumper 8 (see **Figure 3**) are 1x2 headers with one pin connected to the logic control (shutdown-not and edge select) of the IC and the other pin connected to ground. The logic control pin is normally pulled high to Vcc by a 4.7kΩ resistor. Placing a jumper pin across the jumpers would pull the pin to ground. Jumper 7 of the EVM allows the user to select the clock edge of the SN75LVDS83 and SN65LVDS93. A logic high sets the transmitter for rising edge latch, and a logic low sets the transmitter for falling edge latch. Jumper 6 and Jumper 8 control receiver and transmitter power, respectively. A logic high enables the device, and a logic low disables the device.

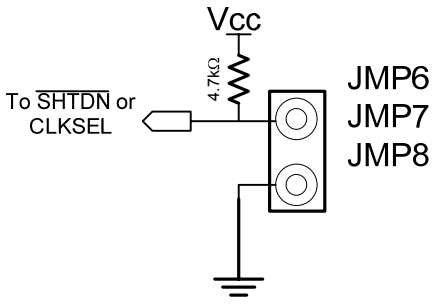

Figure 3. Logic Control Jumper

On the EVM, the signal ground and device-under-test (DUT) ground are separated to facilitate test equipment termination. When testing the EVM with a BERT with 100Ω differential termination, the user can short the two grounds together by shorting Header 9. For detail regarding signal ground and DUT ground, please refer to the respective section on this user's guide.

Table 1. Default EVM--Board Configuration as Shipped

Designator	Function	Condition
JMP1	Data Bridge	Joins the LVTTL data channels D0, D1, D2, D3, D4, D6, and D7 between the transmitter and receiver
JMP2	Data Bridge	Joins the LVTTL data channels D8, D9, D12, D13, D14, D15, and D18 between the transmitter and receiver
JMP3	Data Bridge	Joins the LVTTL data channels D19, D20, D21, D22, D24, D25, and D26 between the transmitter and receiver
JMP4	Data Bridge	Joins the LVTTL data channels D27, D5, D10, D11, D16, D17, and D23 between the transmitter and receiver
JMP5	Clock Bridge	Joins the LVTTL clock-out of the receiver to the LVTTL clock-in of the transmitter
JMP6	Receiver Enable	Logic High to enable the receiver and logic Low to disable the receiver
JMP7†	Transmitter Clock-Edge Select	Logic High to select rising edge and logic Low to select falling edge
JMP8	Transmitter Enable	Logic High to enable the transmitter and logic Low to disable the transmitter
JMP9	Signal Ground and DUT Ground Bridge	Place Jumper Pin to short Signal Ground to DUT Ground

† When performing parallel loop-back test, use logic Low for LVDS82-83 transmitter and receiver pair, and use logic High for LVDS93-94 transmitter and receiver pair

Signal Ground and Device-Under-Test (DUT) Ground

LVDS signal has a common mode voltage V_{CM} of about 1.2V. Therefore, in order for the device to function properly, the output differential voltage has to swing at 1.2V above the device ground (see **Figure 4** and **Figure 5**). To facilitate proper test equipment termination, the EVM has two separate ground planes, which are signal ground and DUT ground. In addition, the signal ground (used for probing the LVDS signal) and the DUT ground (used to bias the device) are to be configured to have a difference of 1.2V.

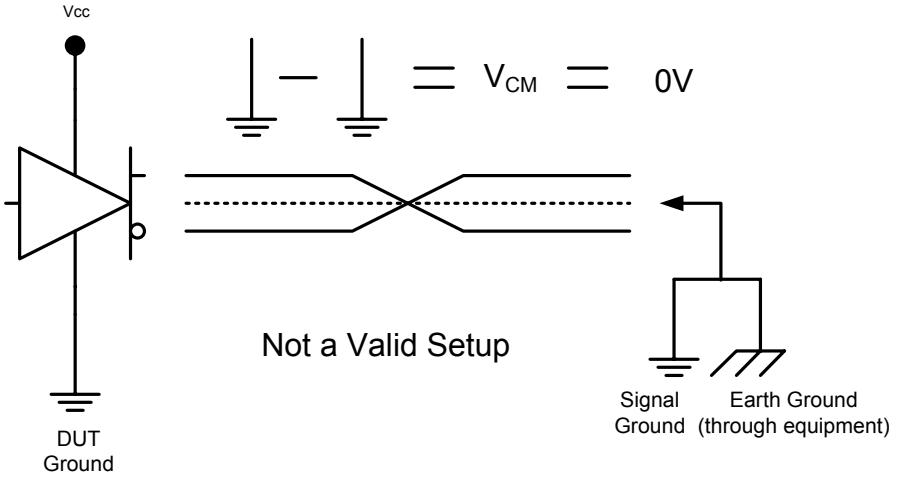

Figure 4. Signal Ground and DUT Ground without Offset

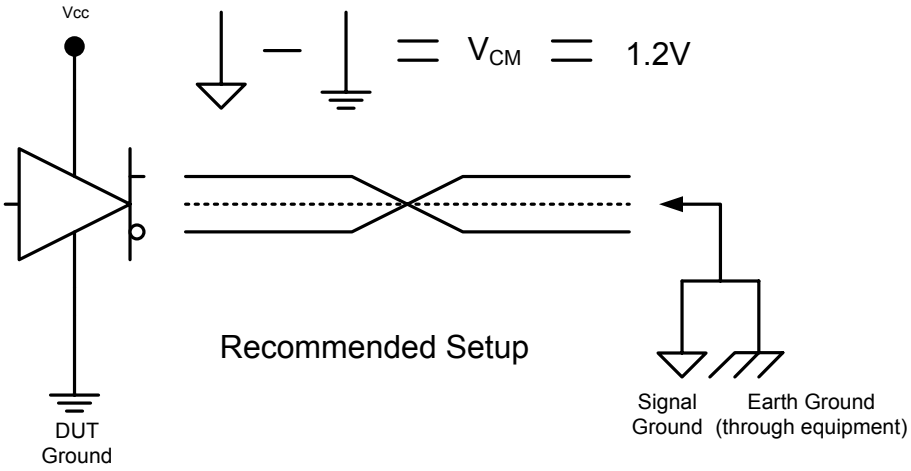

Figure 5. Signal Ground and DUT Ground with Offset

To avoid damaging the test equipment, the two power supplies needed must be isolated power supplies. That is, the power supply's negative terminal is not connected to earth ground. Also, since the generator is referenced to signal ground, which is 1.2V higher than the DUT ground, please offset the generator by -1.2V to avoid damage to the EVM. For instance, if the LVTTL signal swing is 3.3V to 0V, please offset the generator so that the output is 2.1V to -1.2V. Expect a signal on the oscilloscope to be offset by -1.2 V as well since the oscilloscope is also referenced to signal ground as well. An example test setup to evaluate the receiver side and transmitter side of the EVM is shown in **Figure 6**Error! Reference source not found. and **Figure 7**, respectively.

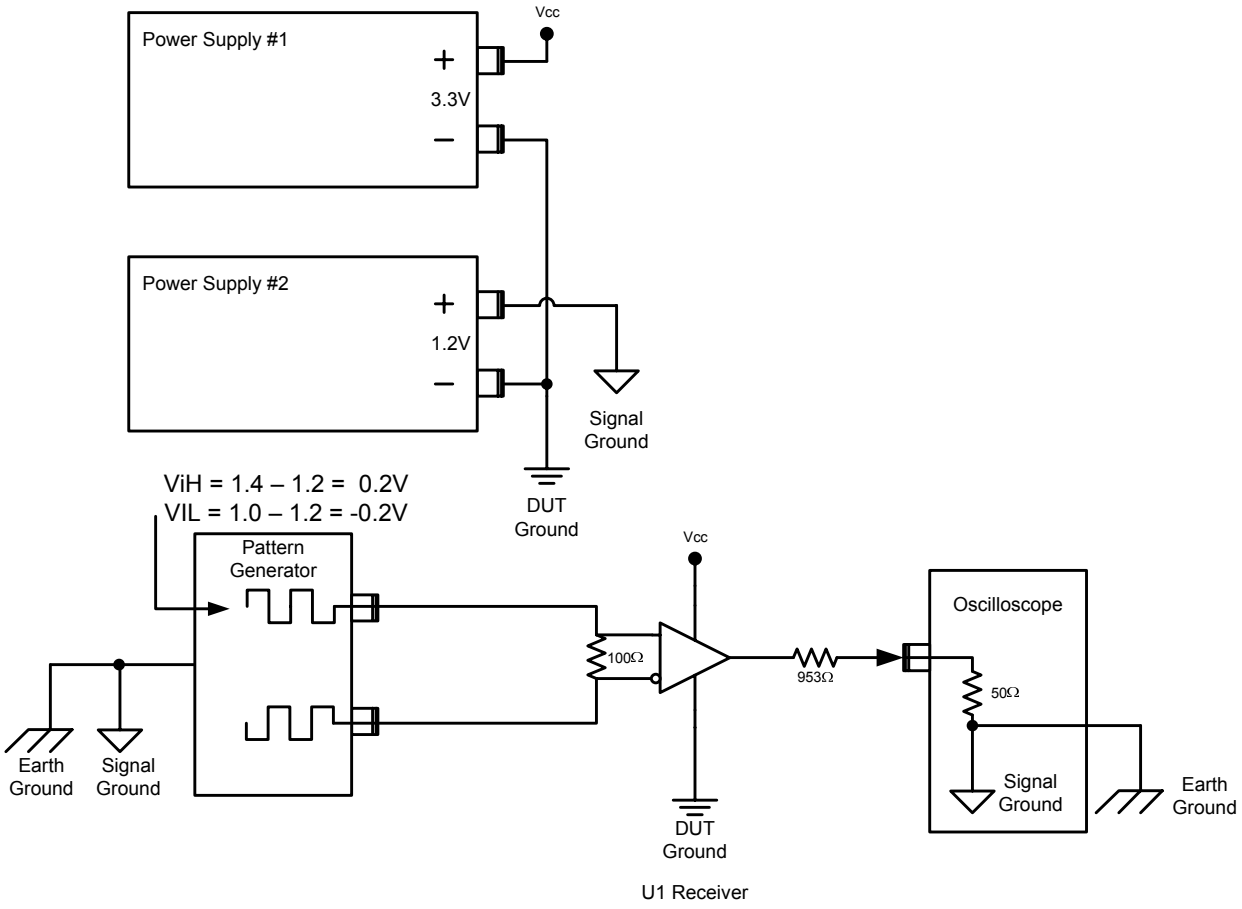

Figure 6. Test Setup to Evaluate Receiver

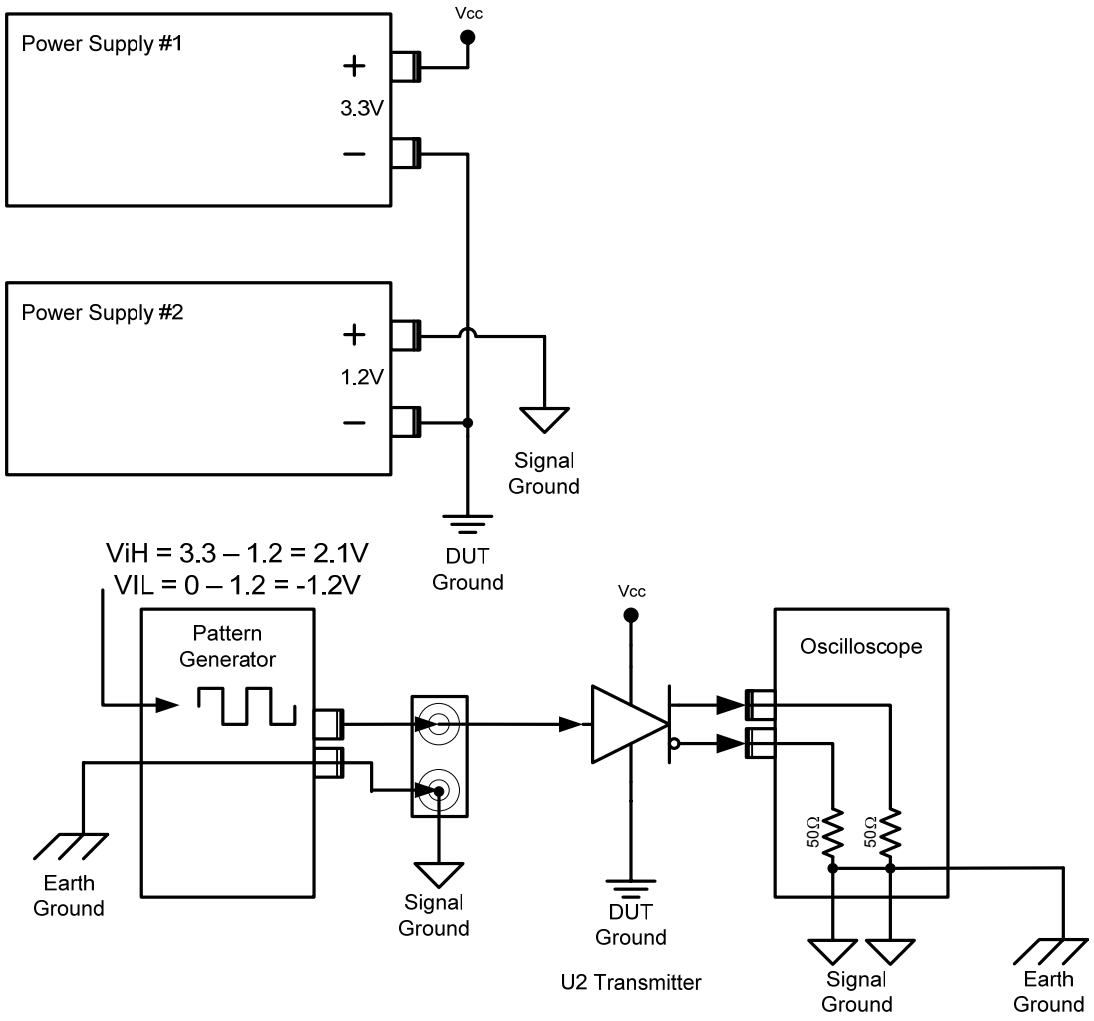

Figure 7. Test Setup to Evaluate Transmitter

Typical Test and Setup Configurations

This section presents the typical test and setup configuration used to evaluate and test the transceiver. The printed-circuit board construction and characteristics are included in the second section of this section.

The following configurations are used to evaluate and test the LVDS82-83-93-94 EVM. The first configuration is an external serial loopback of the high-speed signals shown in **Figure 8**. The serial loopback allows the system designer to evaluate most of the functions of the transmitter and receiver devices of the EVM. To test a system, a parallel Bit Error Rate Tester (BERT) generates a predefined parallel bit pattern. The pattern is connected to the transmitter (U2) through parallel connectors D0 through D27. The transmitter (U2) device serializes and presents the data on the high speed serial pair (YxM/YxP). The serial TX data is then looped back to the receiver side and the device (U1) de-serializes and presents the data on the receiver side D0 through D27. The data is received by the BERT and compared against the transmitted pattern and monitored for valid data and errors.

Moreover, if a serial BERT is available, the system designer can independently test both serial channels of the device with a PRBS 2^7-1 data pattern, see **Figure 9**. By connecting the jumper pins across Jumper 1 through Jumper 5, the receiver and transmitter have their parallel ports connected. This test only validates the high speed serial portion of the device and the system interconnects. The PRBS pattern is compatible with most serial BERT test equipment. This function allows the operator to isolate and test the transmitter and receiver independently.

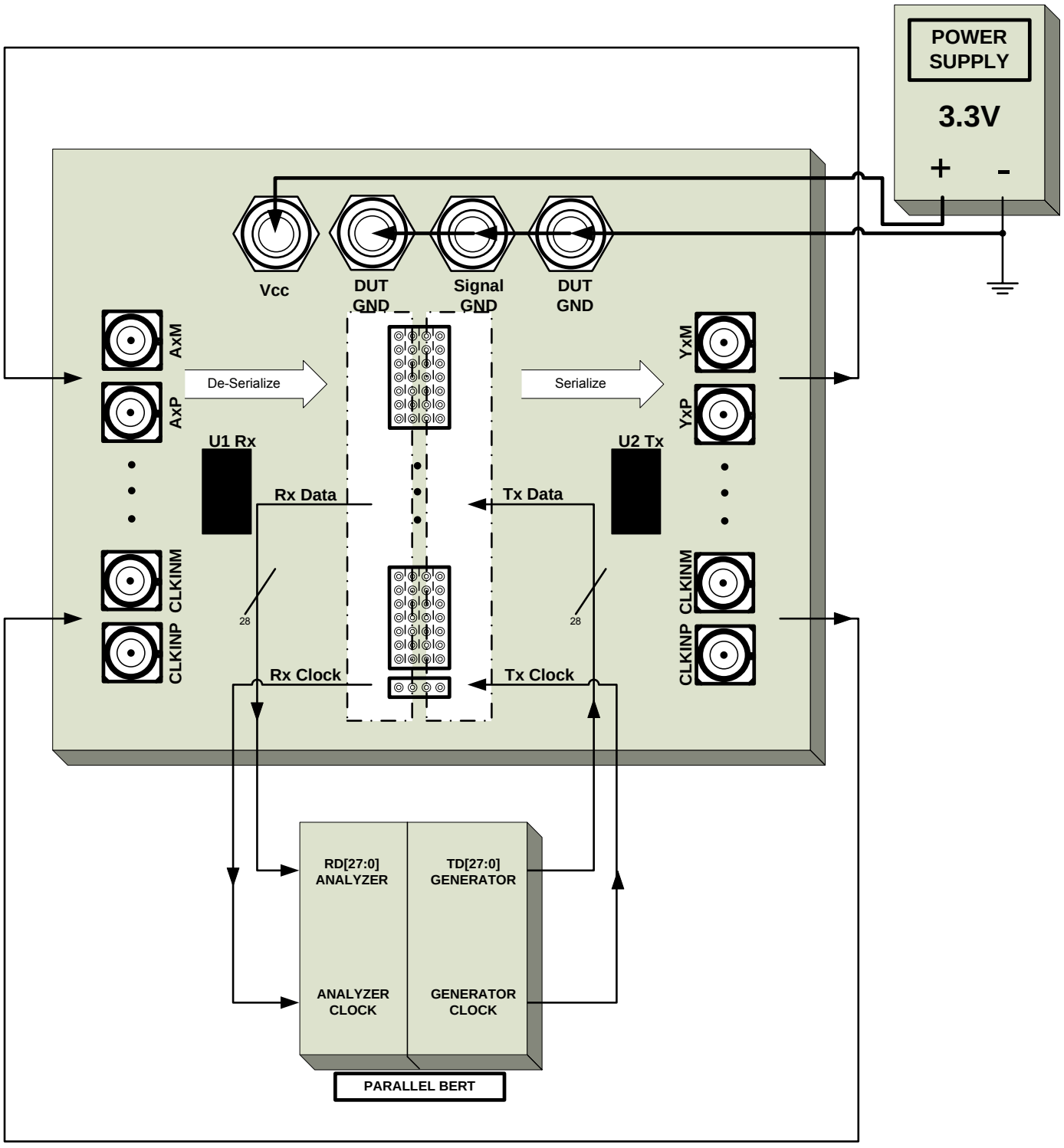

Figure 8. External Serial Loop-back using Parallel BERT

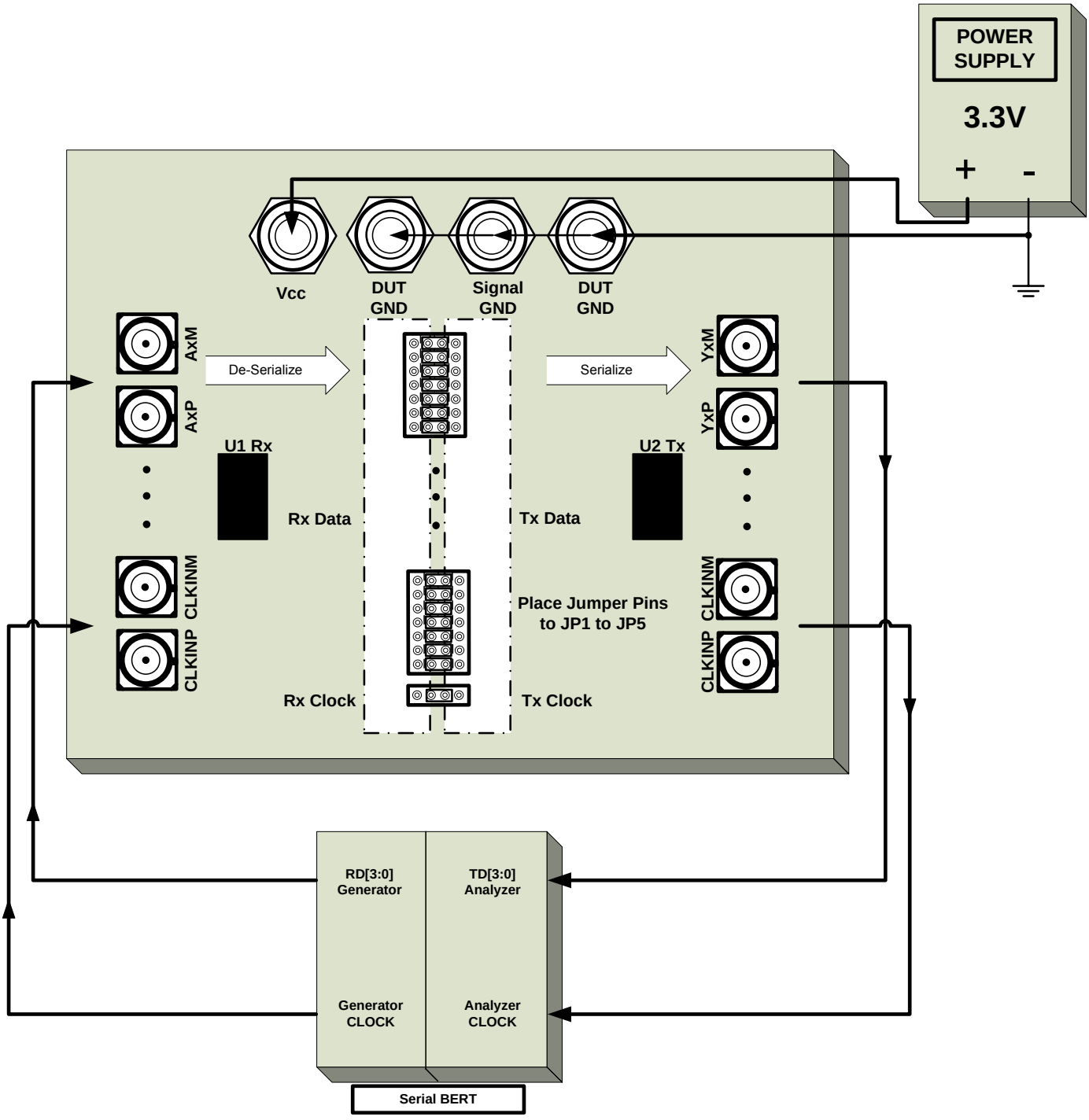

Figure 9. External Parallel Loop-back using Serial BERT

Schematic

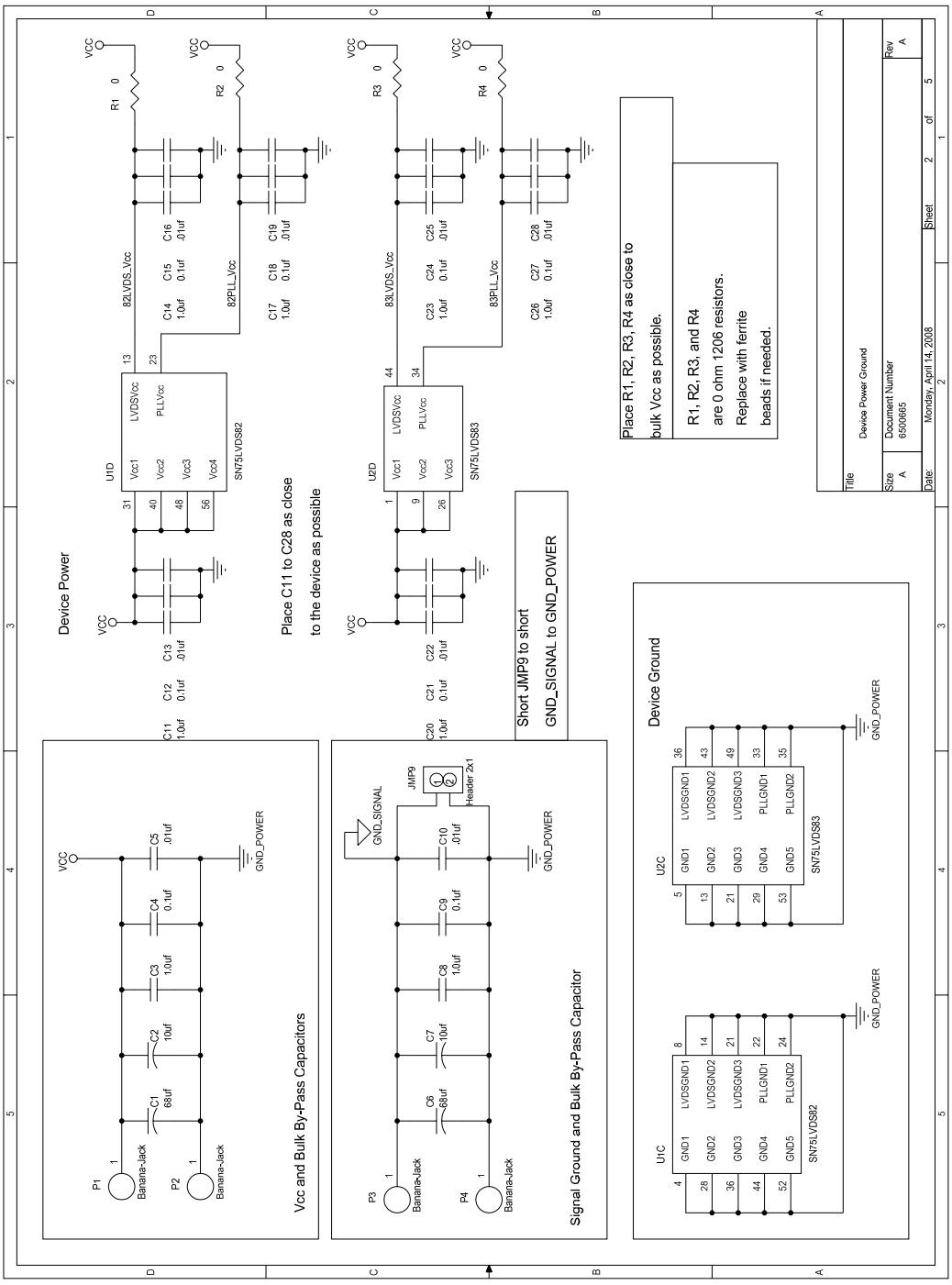

Figure 10. SNxxLVDS82-83-93-94 EVM Device Power Ground

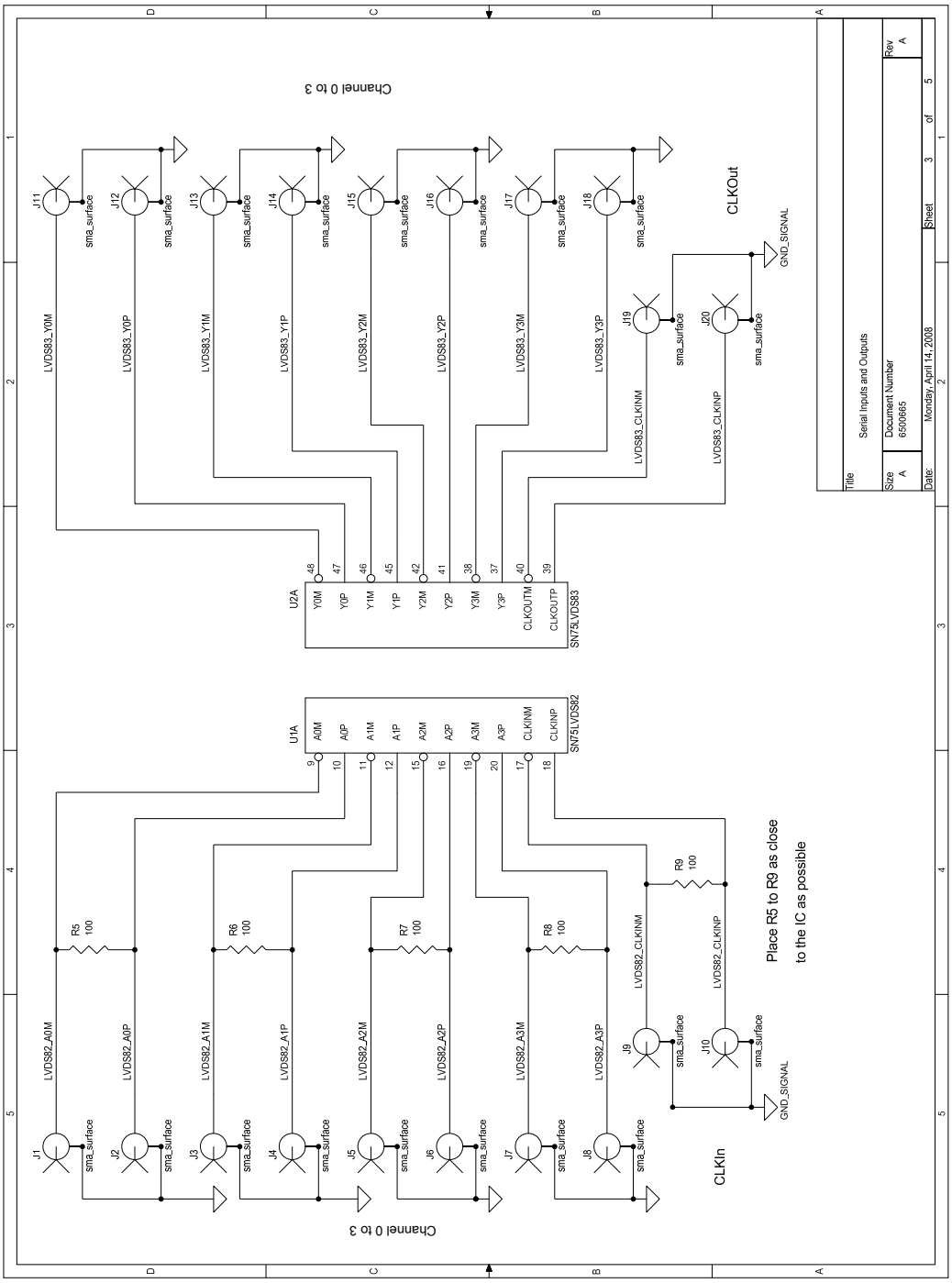

Figure 11. SNxxLVDS82-83-93-94 EVM Serial Inputs and Outputs

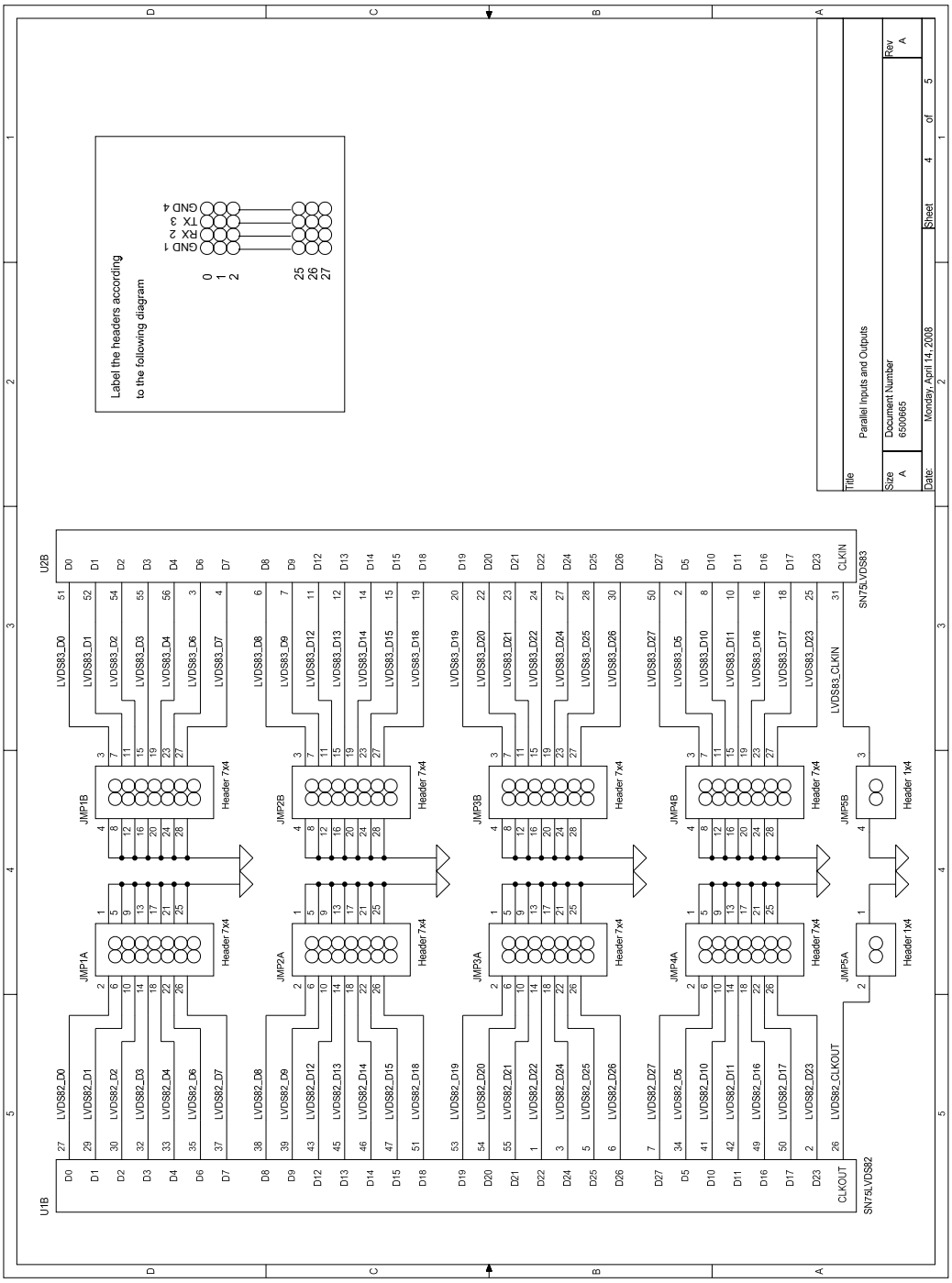

Figure 12. SNxxLVDS82-83-93-94 EVM Parallel Inputs and Outputs

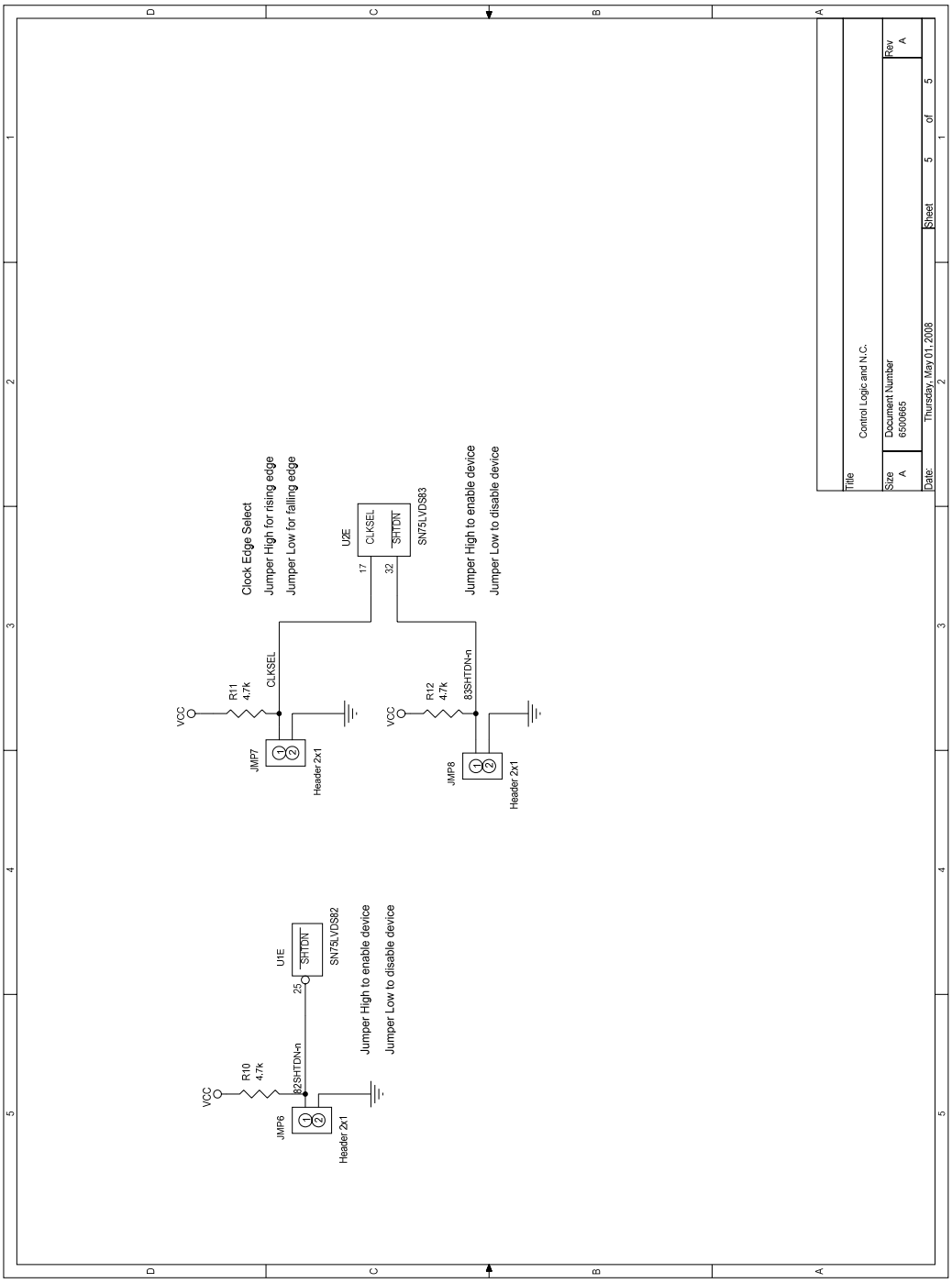

Figure 13. SNxxLVDS82-83-93-94 EVM Control Logic

Table 2. SNxxLVDS82-83-93-94 EVM Bill of Materials

Item No.	Quantity	Ref. Des.	Description	Part Number	Mfg.
1	2	C1, C6	Capacitor, 68uF, tantalum	TAJE686K025R	AVX
2	2	C2, C7	Capacitor, 10uF, tantalum	293D106X0035D2W	Sprague
3	2	C3, C8	Capacitor, 1.0uF, ceramic	12063G105ZAT2A	AVX
4	2	C4, C9	Capacitor, 0.1uF, ceramic	1206C104JATMA	AVX
5	2	C5, C10	Capacitor, 0.01uF, ceramic	08051C103JATMA	AVX
6	6	C11, C14, C17, C20, C23, C26	Capacitor, 1.0uF, ceramic	12063G105ZAT2A	AVX
7	6	C12, C15, C18, C21, C24, C27	Capacitor, 0.1uF, ceramic	1206C104JATMA	AVX
8	6	C13, C16, C19, C22, C25, C28	Capacitor, 0.01uF, ceramic	08051C103JATMA	AVX
9	4	JMP1, JMP2, JMP3, JMP4	Header 7x4		
10	1	JMP5	Header 1x4		
11	4	JMP6, JMP7, JMP8, JMP9	Header 2x1		
12	20	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20	SMA Surface Mount	32k141-40m-fr4wvia	
13	4	P1, P2, P3, P4	Banana Jack		Pomona
14	4	R1, R2, R3, R4	Resistor, 0 Ω, 1210‡		
15	5	R5, R6, R7, R8, R9	Resistor, 100Ω, 0402		
16	3	R10, R11, R12	Resistor, 4.7kΩ 0603		
17	1	U1	SN75LVDS82 Receiver (may be replaced with SN65LVDS93)		TI
18	1	U2	SN75LVDS83 Driver (may be replaced with SN65LVDS94)		TI

‡ R1, R2, R3, and R4 1210 size 0Ω resistors may be replaced with 1210 ferrite beads if necessary.

Board Layouts

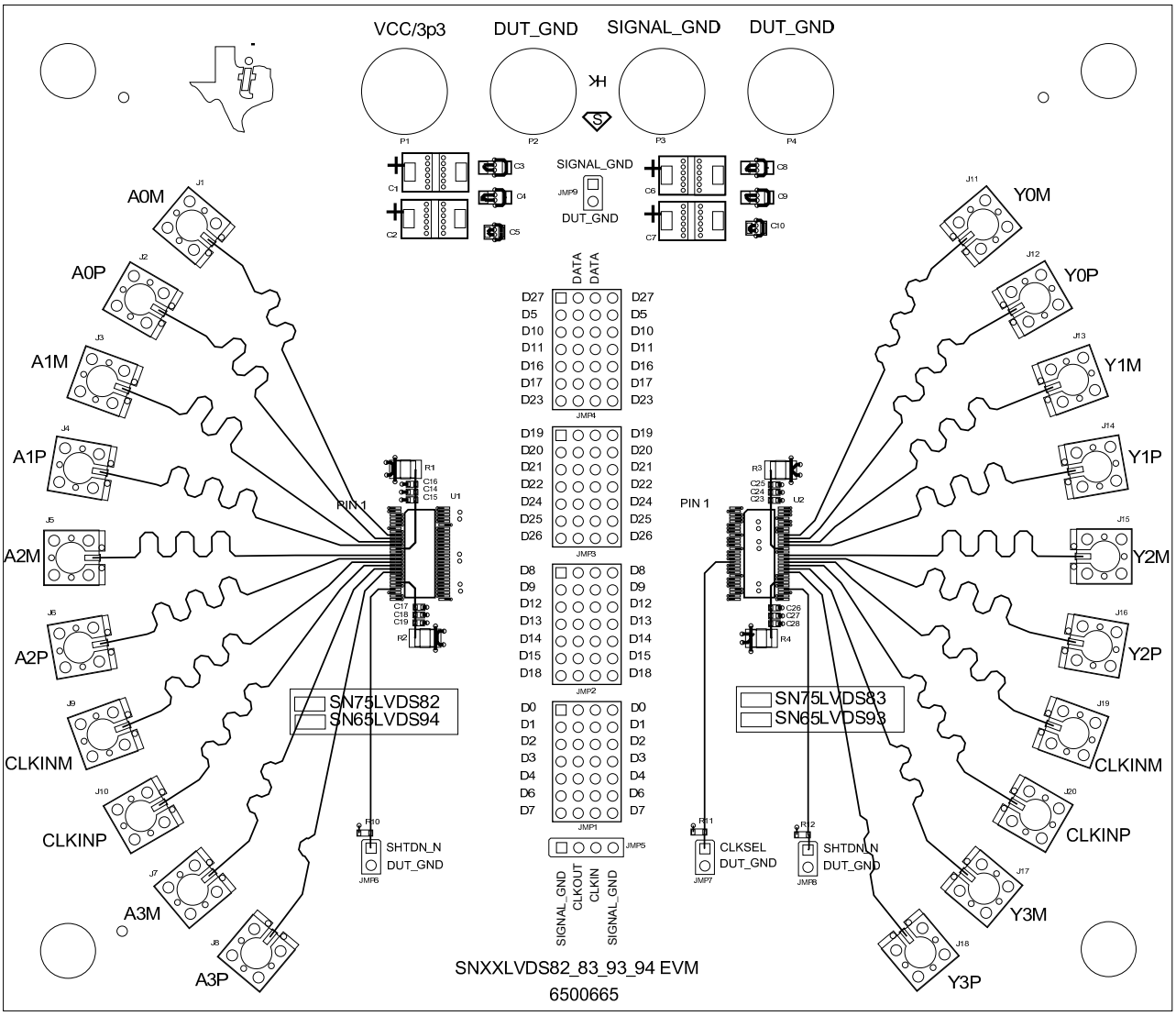

Figure 14. SNxxLVDS82-83-93-94 Board Layout: Top (Layer 1)

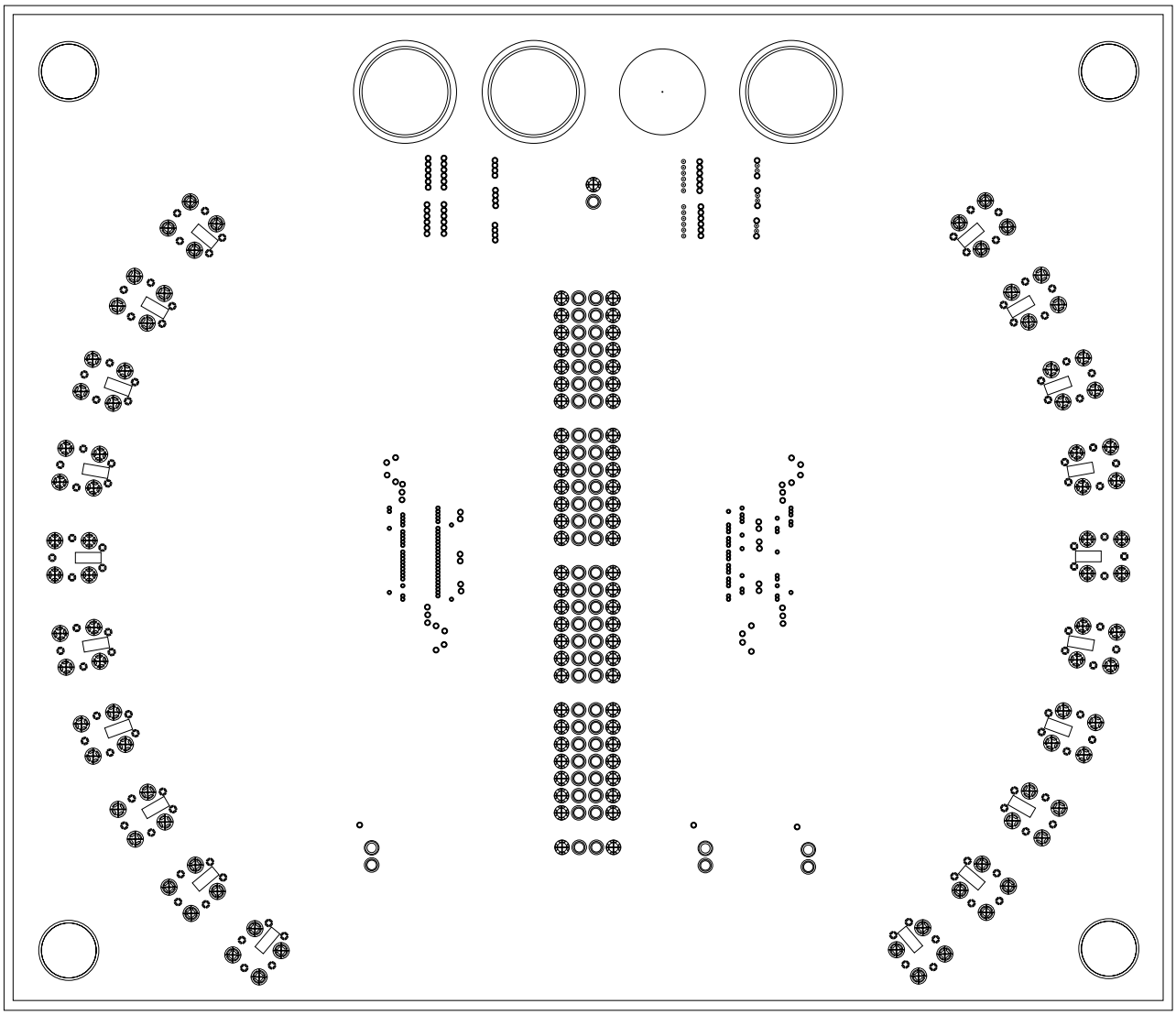

Figure 15. SNxxLVDS82-83-93-94 Board Layout: GND (Layer 2)

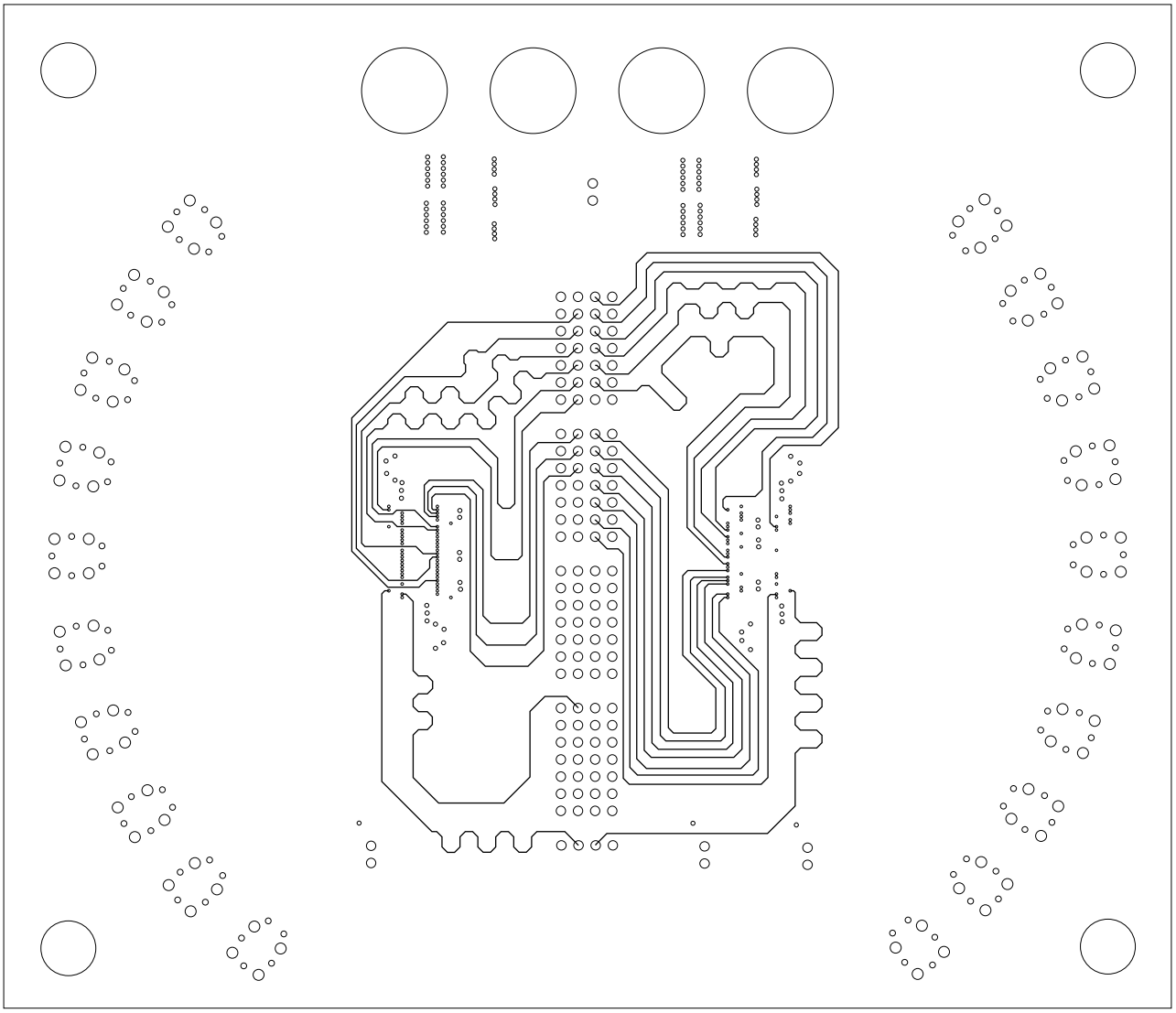

Figure 16. SNxxLVDS82-83-93-94 Board Layout: Signal (Layer 3)

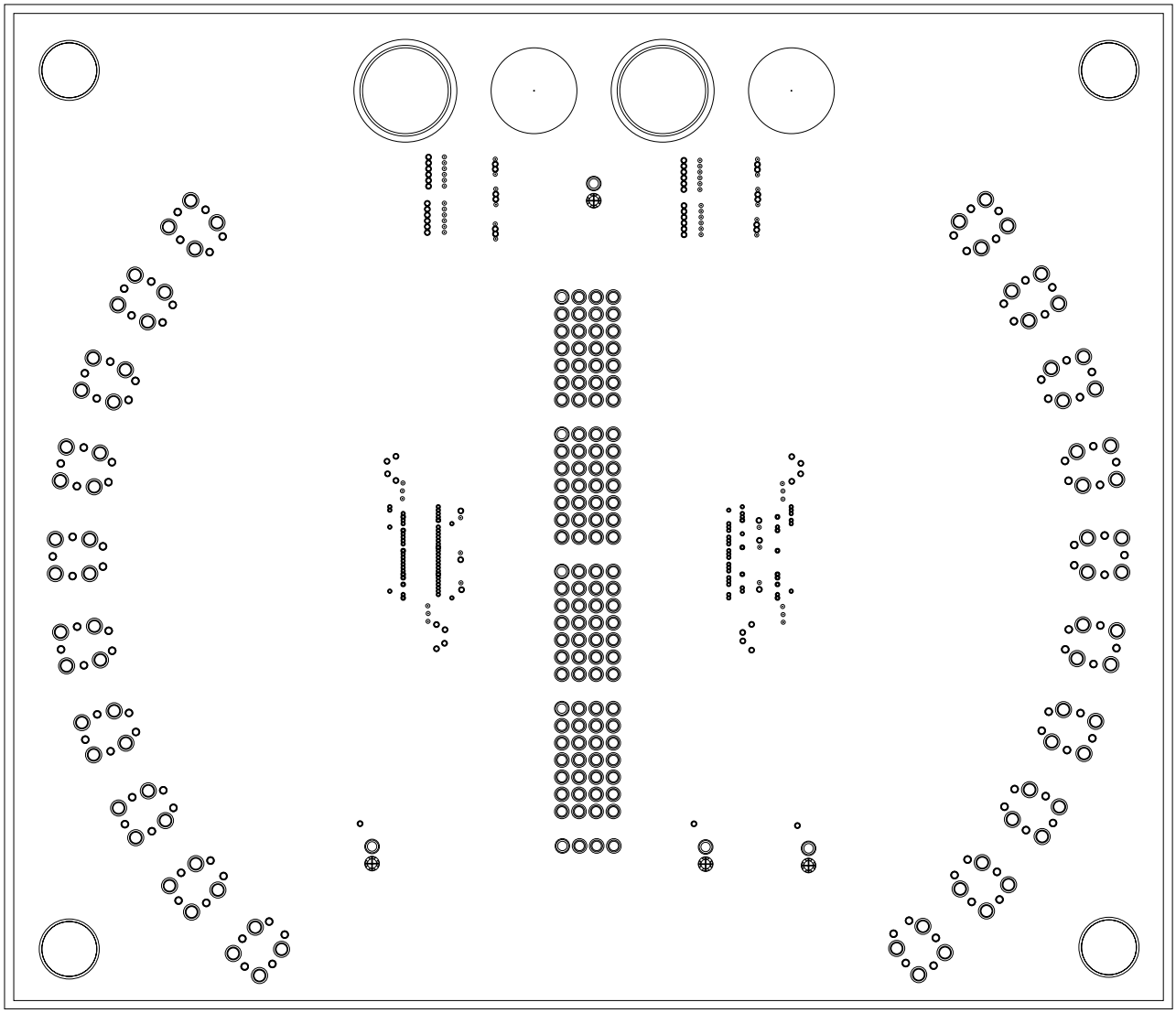

Figure 17. SNxxLVDS82-83-93-94 Board Layout: GND (Layer 4)

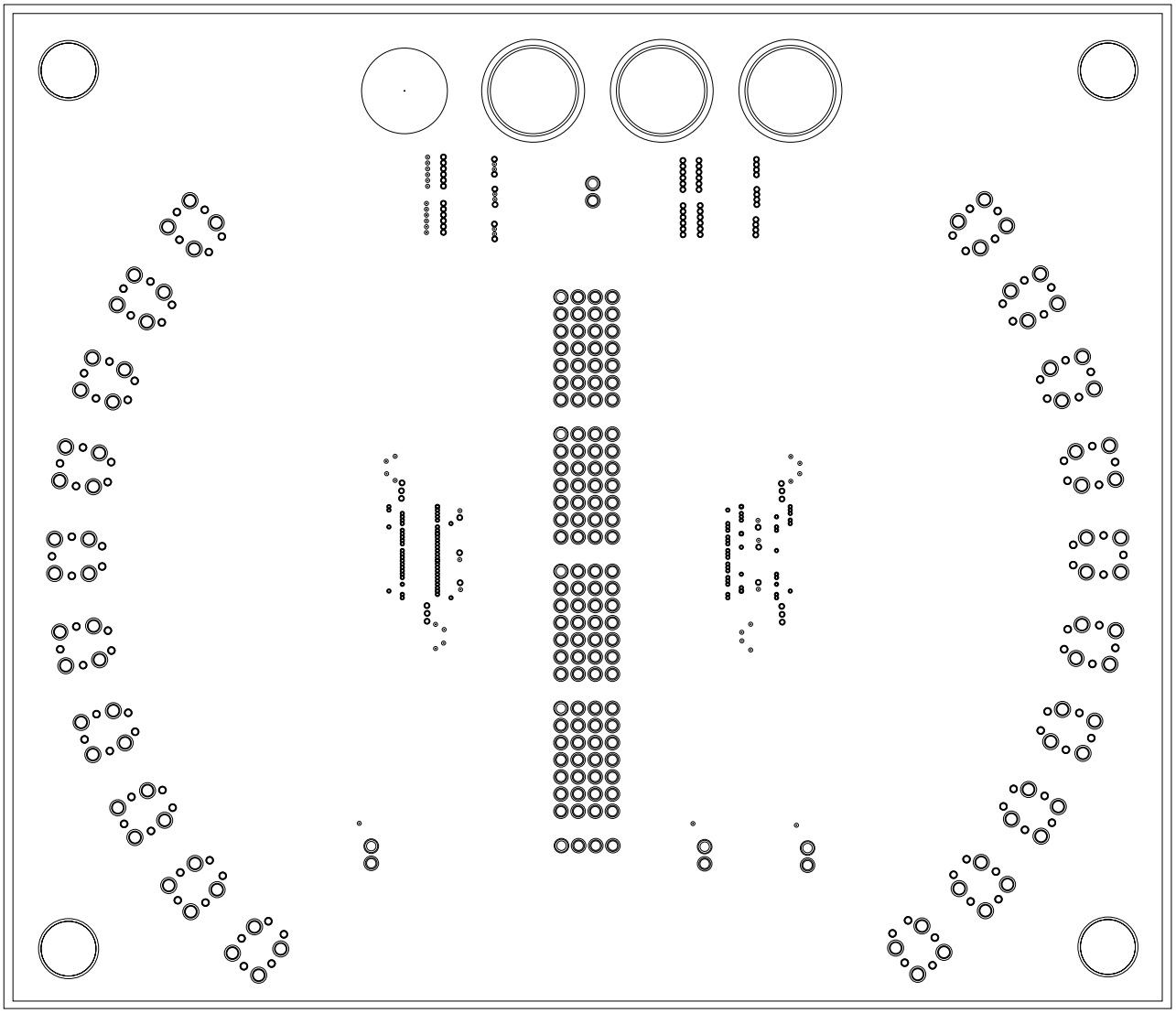

Figure 18. SNxxLVDS82-83-93-94 Board Layout: Vcc (Layer 5)

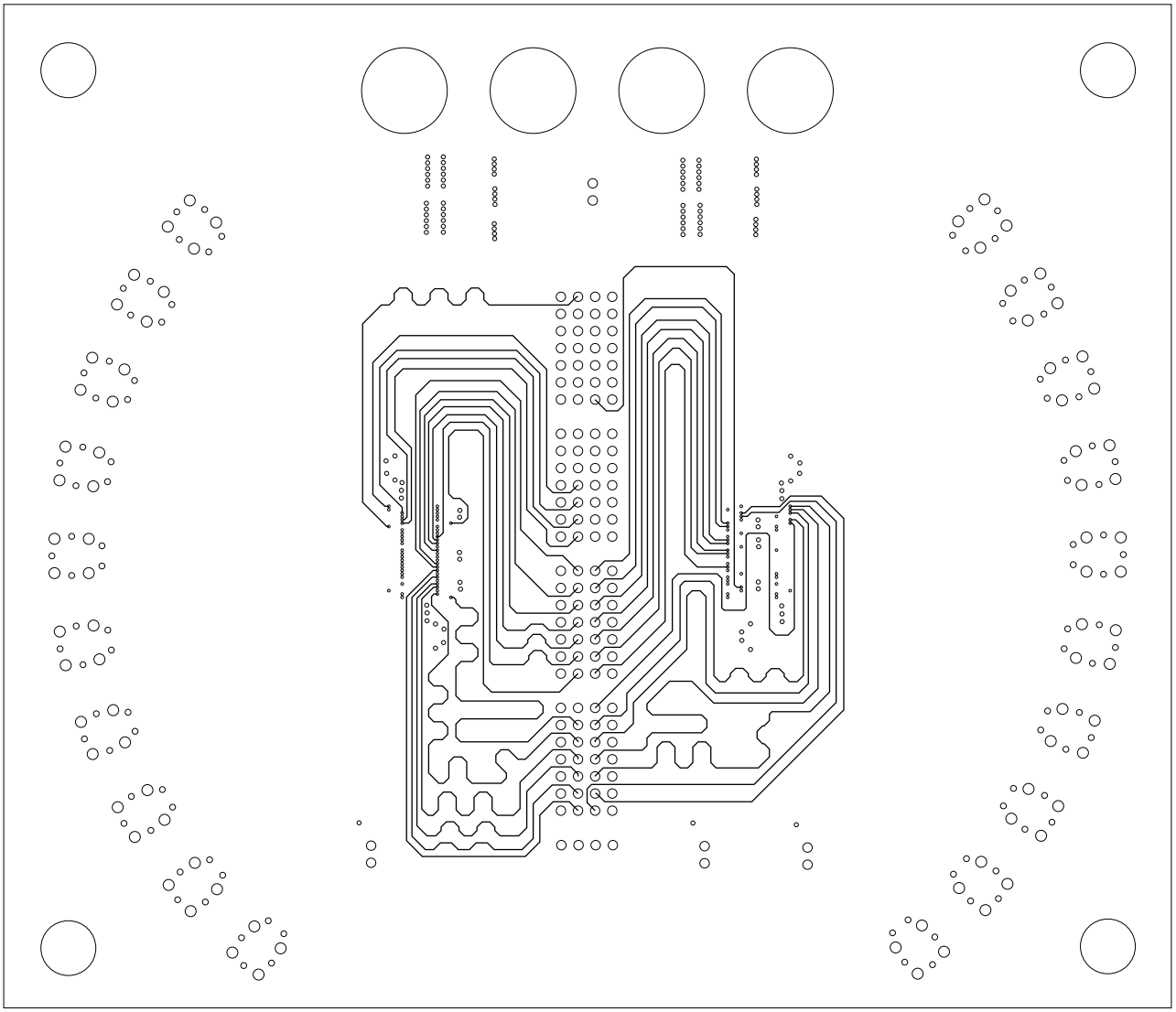

Figure 19. SNxxLVDS82-83-93-94 Board Layout: Signal (Layer 6)

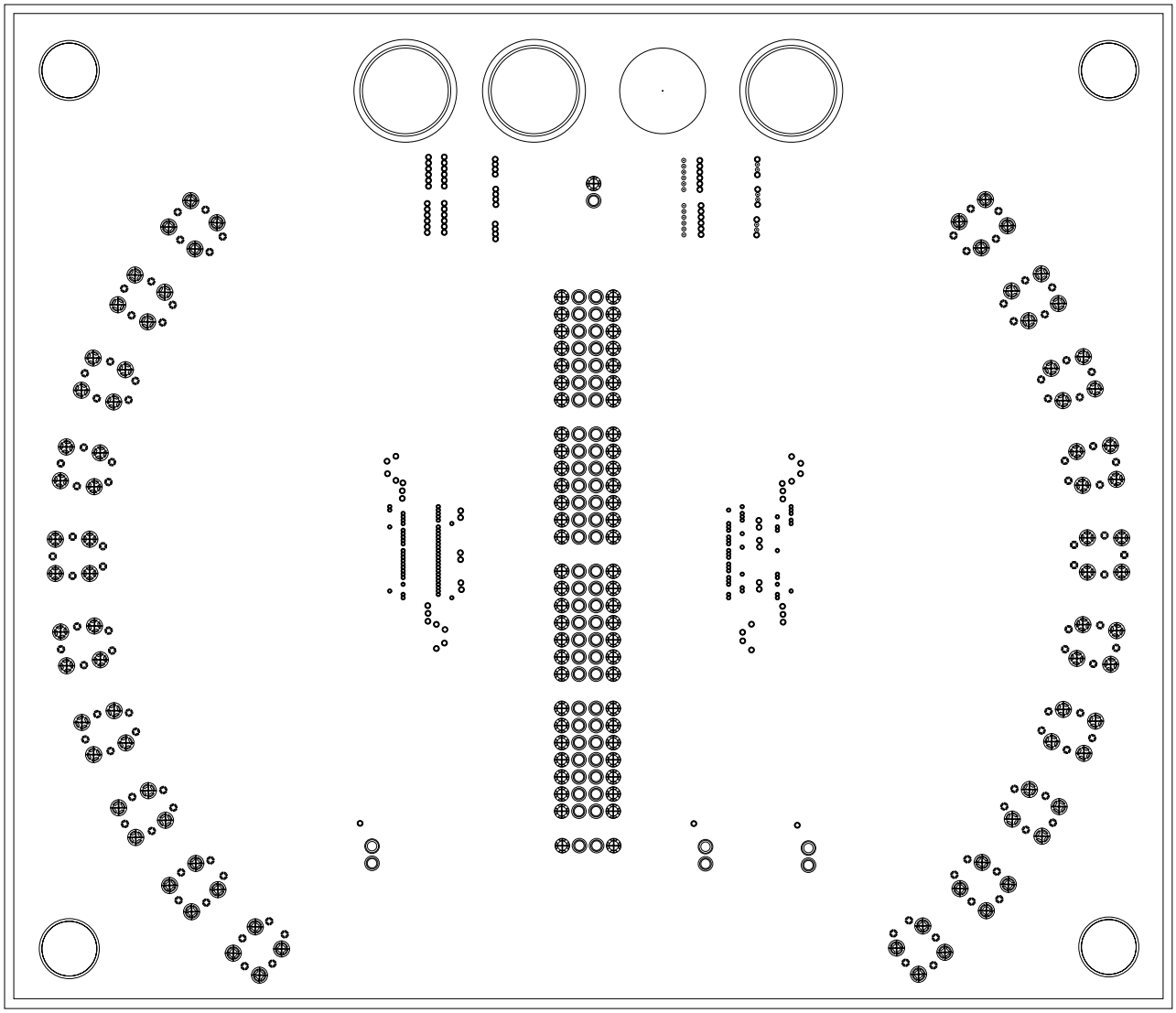

Figure 20. SNxxLVDS82-83-93-94 Board Layout: GND (Layer 7)

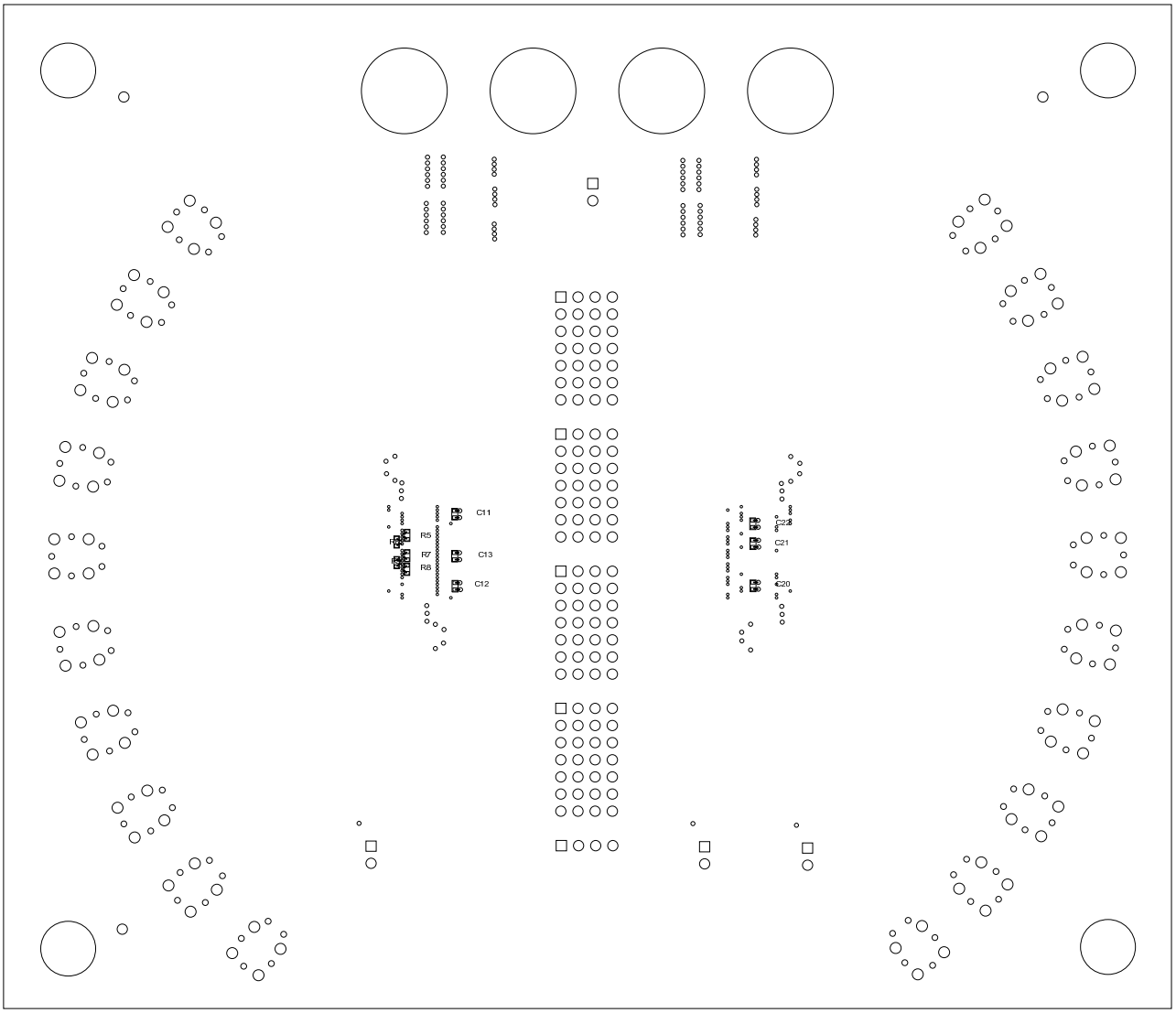

Figure 21. SNxxLVDS82-83-93-94 Board Layout: Bottom (Layer 8)

Table 3. SNxxLVDS82-83-93-94 EVM PCB Layer Construction

Subclass Name	Type	Material	Thickness (MIL)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Negative Artwork	SHIELD	Width (MIL)	Impedance (ohm)
	SURFACE	AIR								
TOP	CONDCUTOR	COPPER	2.4	595900	1	0	No		9.50	47.917
	DIELECTRIC	FR-4	5	0	4.1	0.035				
L2_GND	PLANE	COPPER	1.2	595900	1	0	No	YES		
	DIELECTRIC	FR-4	5	0	4.1	0.035				
L3_SIG	CONDCUTOR	COPPER	1.2	595900	1	0	No		7.00	49.196
	DIELECTRIC	FR-4	20	0	4.1	0.035				
L4_GND	PLANE	COPPER	1.2	595900	1	0	No	YES		
	DIELECTRIC	FR-4	5	0	4.1	0.035				
L5_VCC	PLANE	COPPER	1.2	595900	1	0	No	YES		
	DIELECTRIC	FR-4	20	0	4.1	0.035				
L6_SIG	CONDCUTOR	COPPER	1.2	595900	1	0	No		7.00	48.778
	DIELECTRIC	FR-4	5	0	4.1	0.035				
L7_GND	PLANE	COPPER	1.2	595900	1	0	No	YES		
	DIELECTRIC	FR-4	5	0	4.1	0.035				
BOTTOM	CONDCUTOR	COPPER	2.4	595900	1	0	No		9.50	47.917
	SURFACE	AIR								

****NOTE: Always consult with your board manufacturer for their process/design requirements to ensure the desired impedance is achieved.**

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Customers are responsible for their applications using TI components.

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