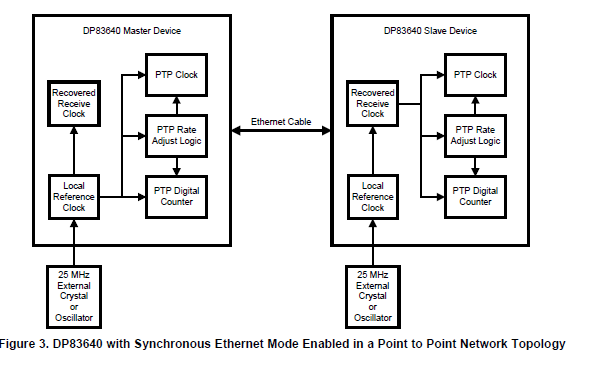
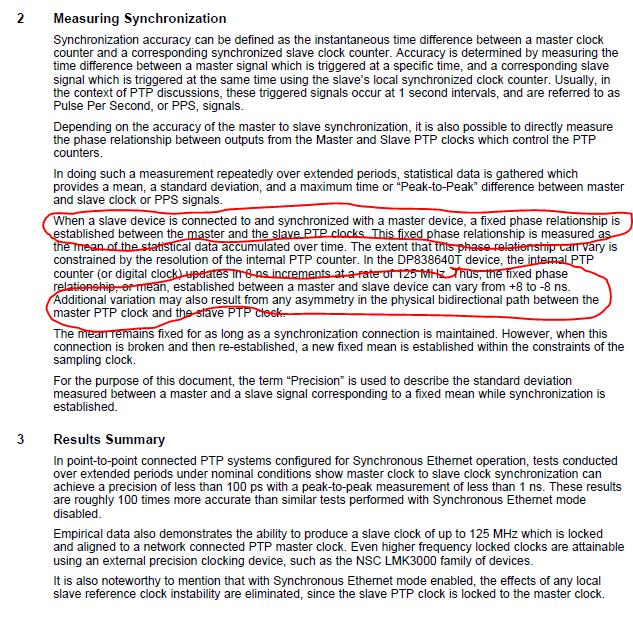
We will have the same SYNCe point-to-point system configuration as shown in the following figure derived from the SNLA100A (AN-1730) app-note:



Also lifted from the SNLA100A (AN-1730) app-note:



As an example of our system; we will be creating a periodic ping event at the master (master event shown in figure) at a fixed 6Hz rate. The slave device will acquire ADC samples to capture the response to the ping event. It is important that the slave know when the master ping occurred so the slave ADC data can be tagged to the corresponding pin event. The ping tag location must be repeatable within a 2.5us window. The slave device will be in SYNCe mode and synchronized to the master PTP clock.



Is this a good application for SYNCe?

Is there a way for the slave and/or master to determine the actual phase offset between the two devices via a register access to the corresponding PHY devices? Can we access the PTP counters somehow?