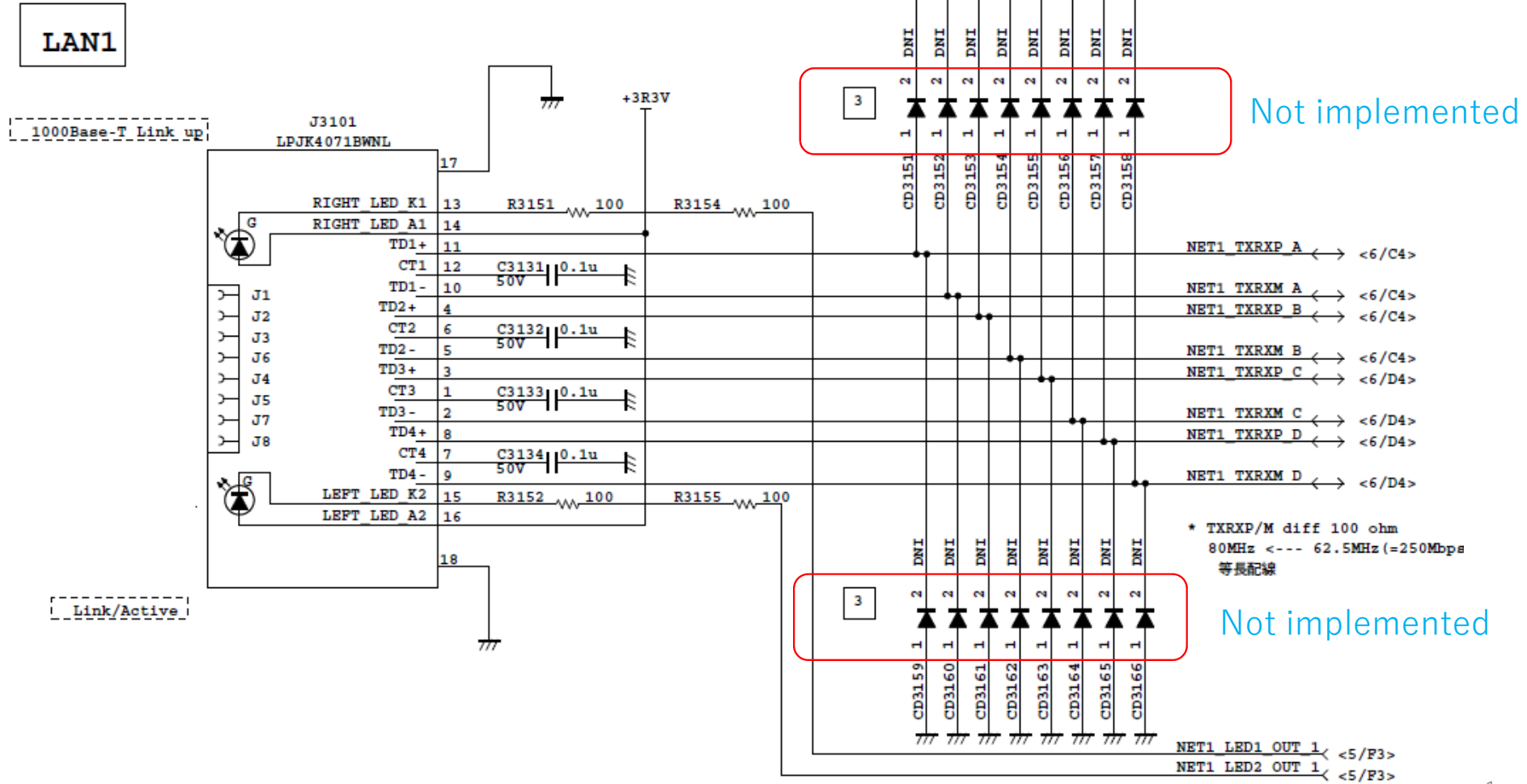
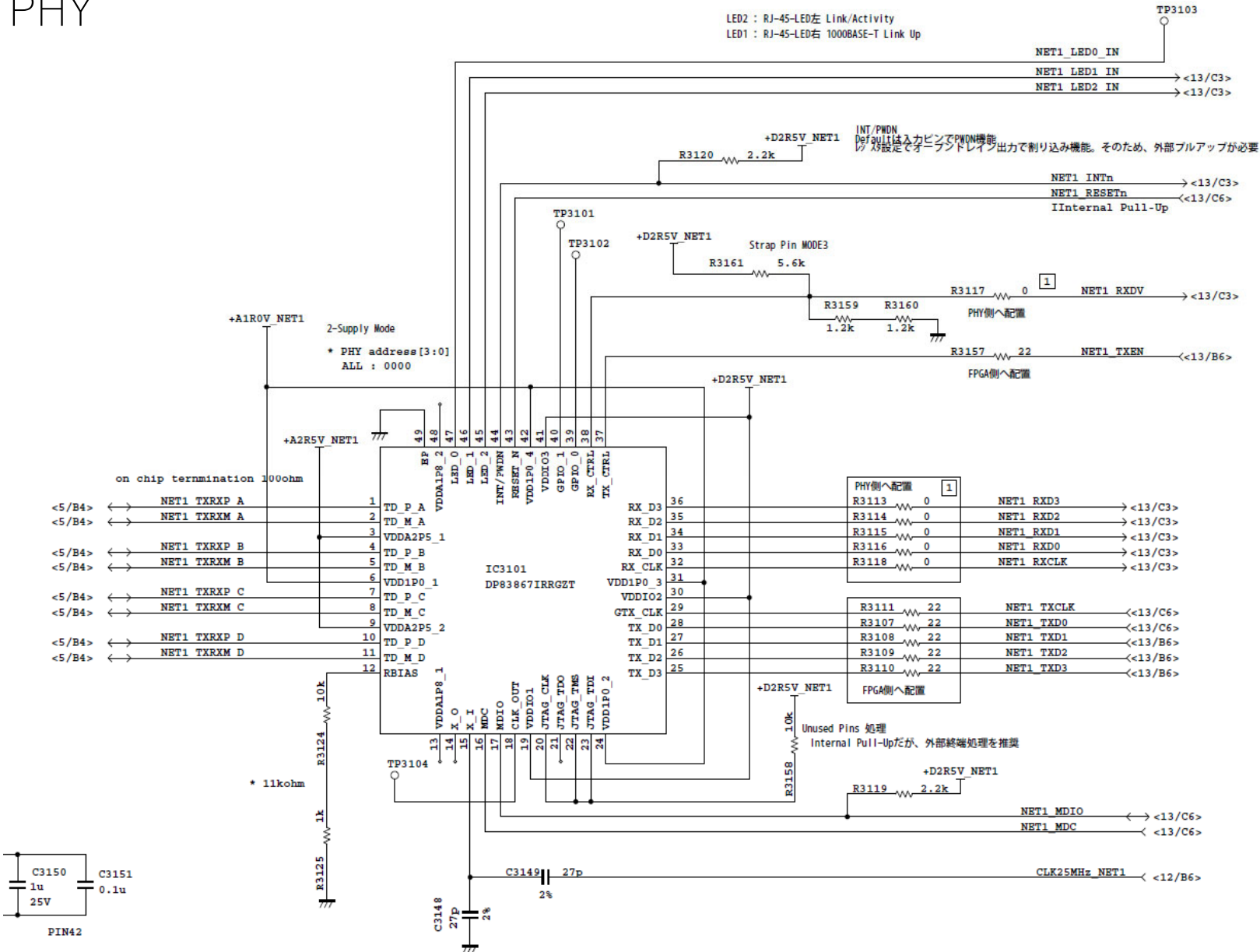


Schematic , Connector

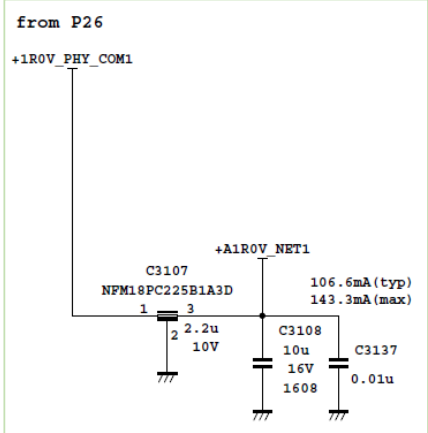
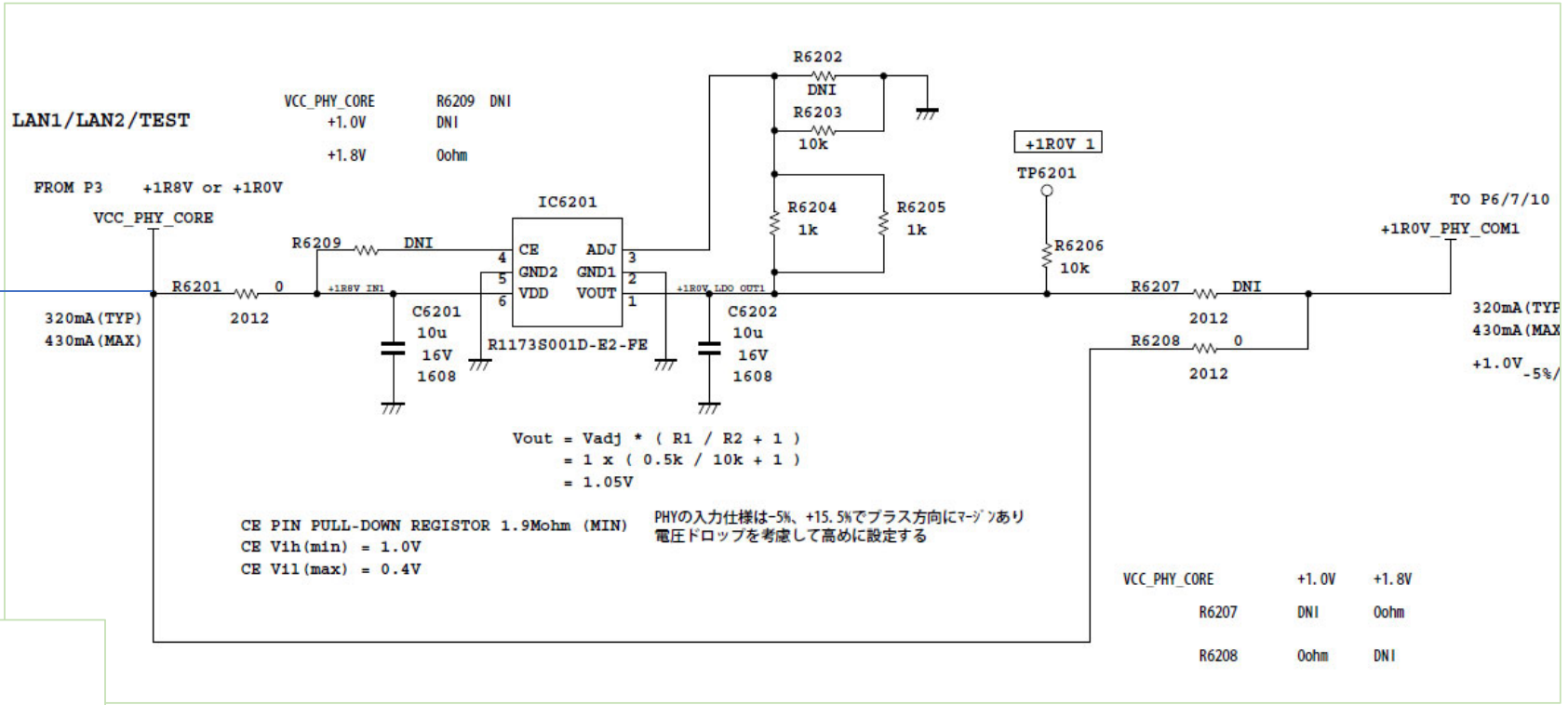


Schematic , PHY

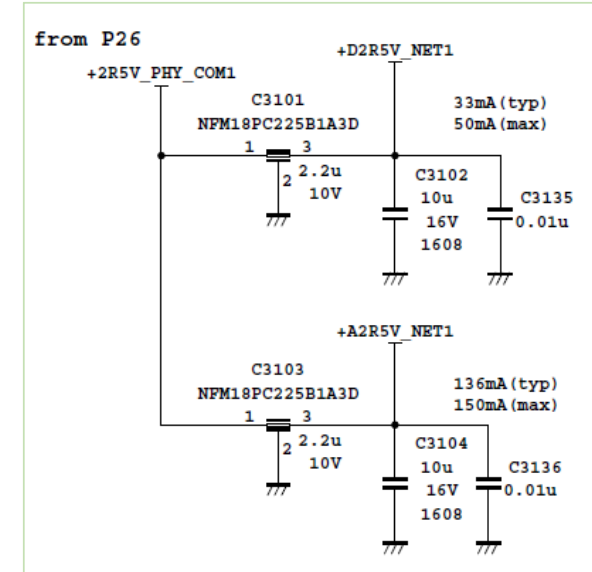
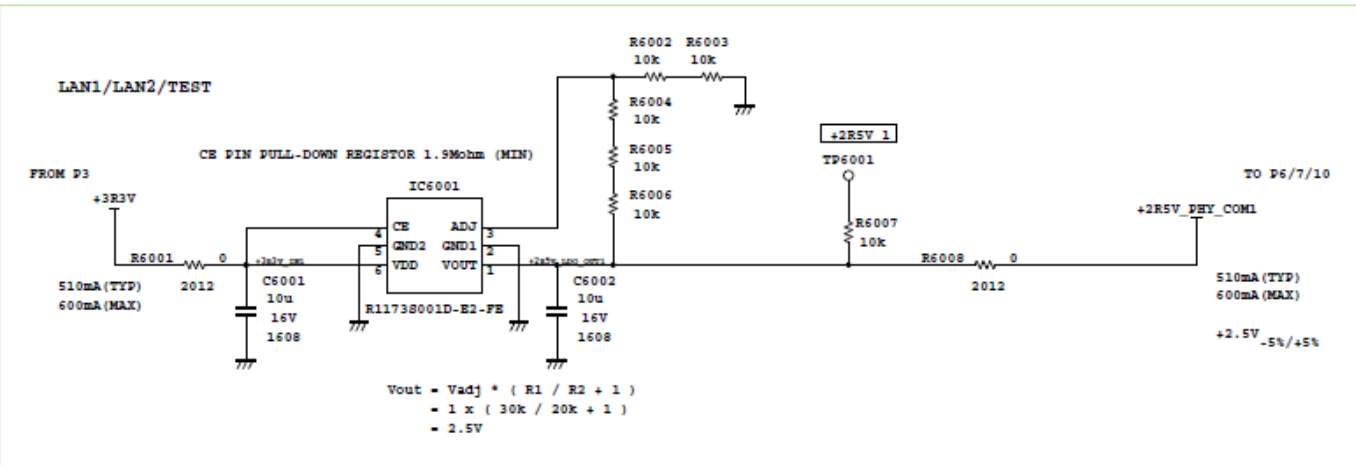


Schematic , Power Supply +1.0V

TPS62130



Schematic , Power Supply +2.5V



PCB Layout (Layer1)

Difference A,B Peak Output Voltage(w/ Disturbing Signal)																				
No3																				
ポート	TEST				P1				P2				P3				P4			
チャンネル(Pair)	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
Peak A [mV] 670~820 mV	726.5	720.1	721.7	724.3	725.4	723.7	717.8	721.6	727.3	720.1	722.6	726.5	734.6	722.7	733.4	736.9	738.8	711.3	721.7	738.4
Peak B [mV] 670~820 mV	-733.3	-716.9	-723.1	-730.5	-739.3	-723.4	-722	-731.5	-741	-727.7	-722.9	-732.8	-742.4	-731.7	-739.2	-743.8	-746.9	-716.3	-729.8	-747.6
difference <1%	0.93%	0.45%	0.20%	0.85%	1.90%	0.03%	0.59%	1.37%	1.86%	1.04%	0.05%	0.87%	1.05%	1.25%	0.78%	0.93%	1.10%	0.70%	1.11%	1.23%

No4																				
ポート	TEST				P1				P2				P3				P4			
チャンネル(Pair)	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
Peak A [mV] 670~820 mV	727.7	713.7	742.7	729.4	735.3	722.9	724.6	733.7	703.2	719	719.3	729.3	725.7	727.3	711.2	734.5	722	724.8	725.7	740.7
Peak B [mV] 670~820 mV	-732.5	-722.2	-752.6	-741.4	-739.1	-723.6	-728.8	-742.5	-713.3	-722.8	-723.2	-738.9	-729.3	-733	-715.3	-742	-731.7	-734.5	-733.9	-754.5
difference <1%	0.66%	1.18%	1.33%	1.63%	0.52%	0.10%	0.57%	1.19%	1.43%	0.53%	0.17%	1.31%	0.49%	0.79%	0.14%	1.01%	1.34%	1.33%	1.13%	1.84%

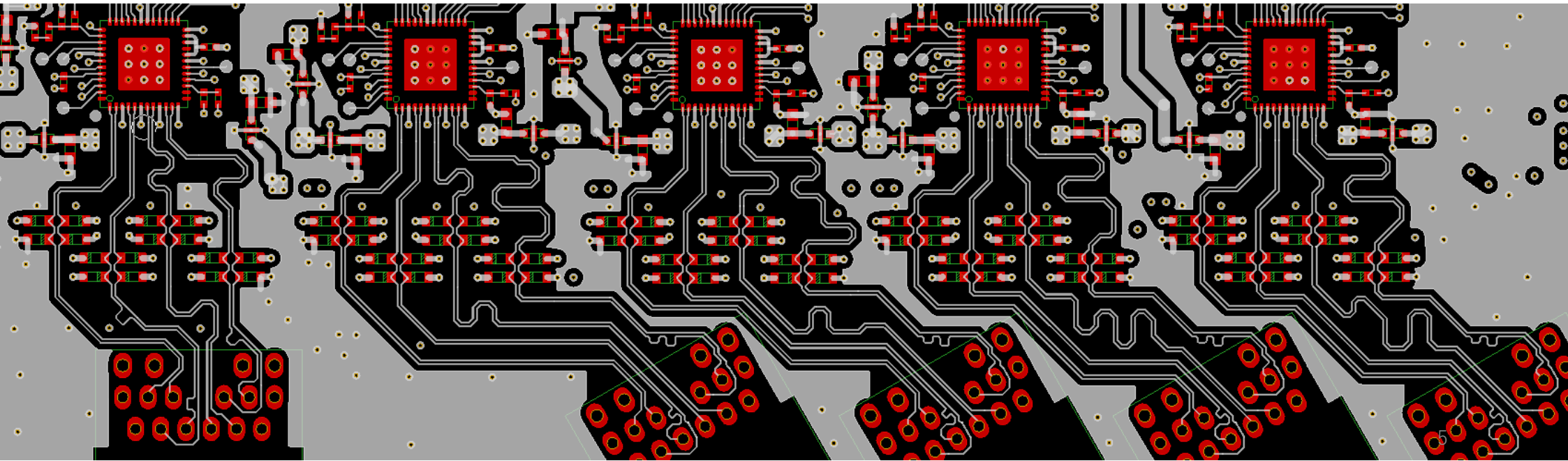
TEST

P1 (LAN1)

P2 (LAN2)

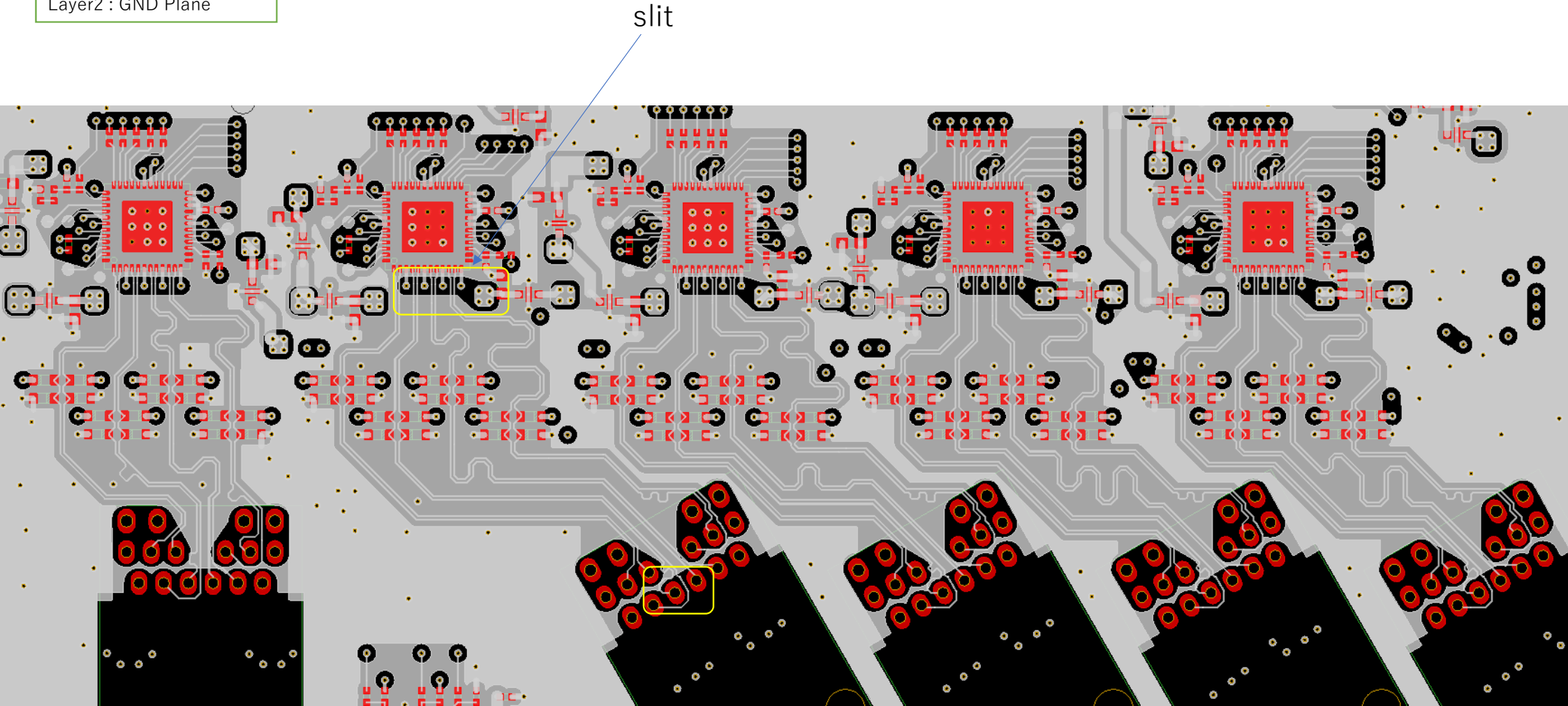
P3 (LAN4)

P1 (LAN4)

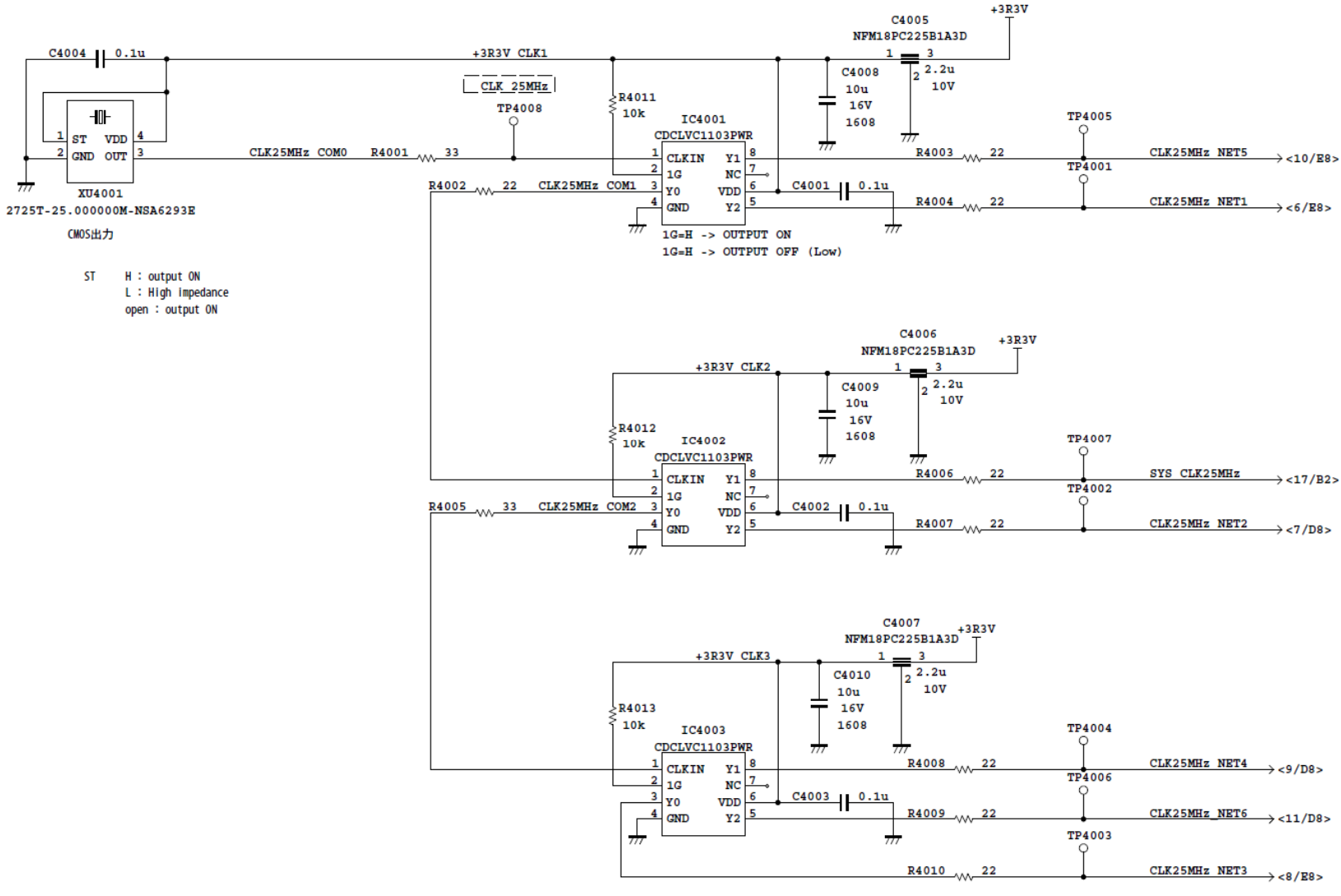


PCB Layout (Layer1 & Layer2)

Layer1 : Trace
Layer2 : GND Plane



Clock Distribution



to TEST
to P1

to FPGA
to P2

to P4
to P3

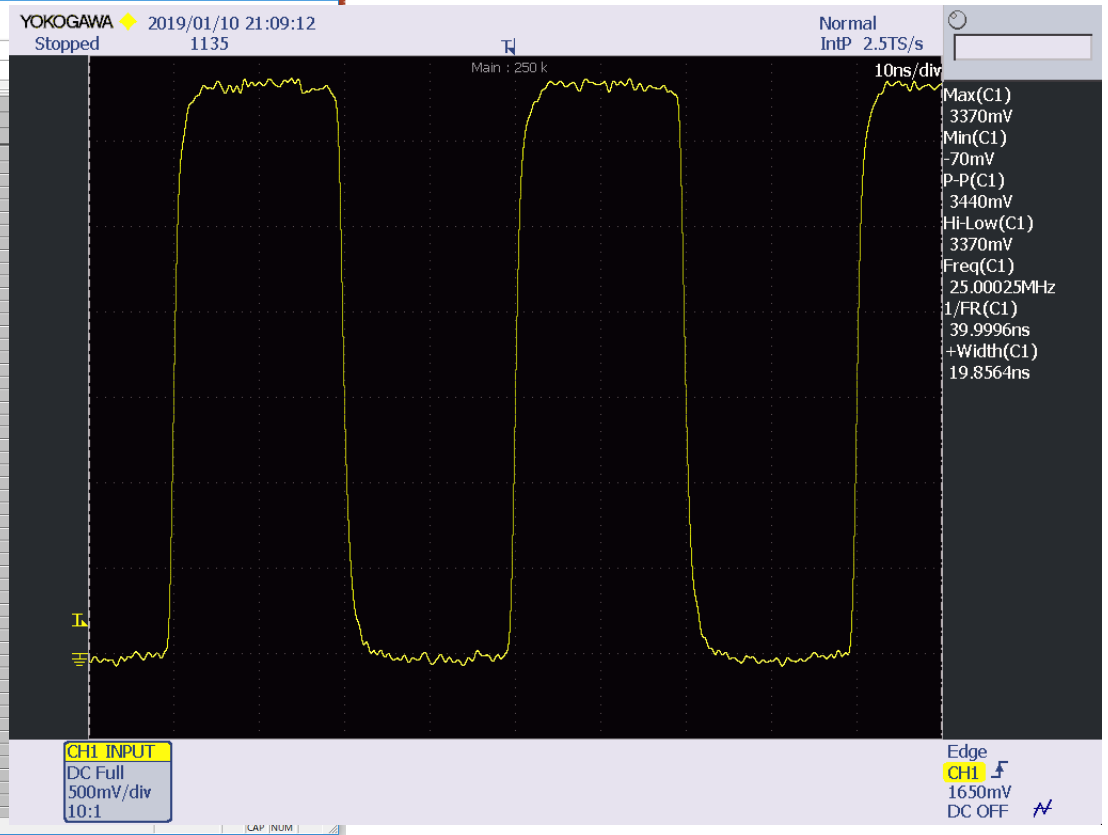
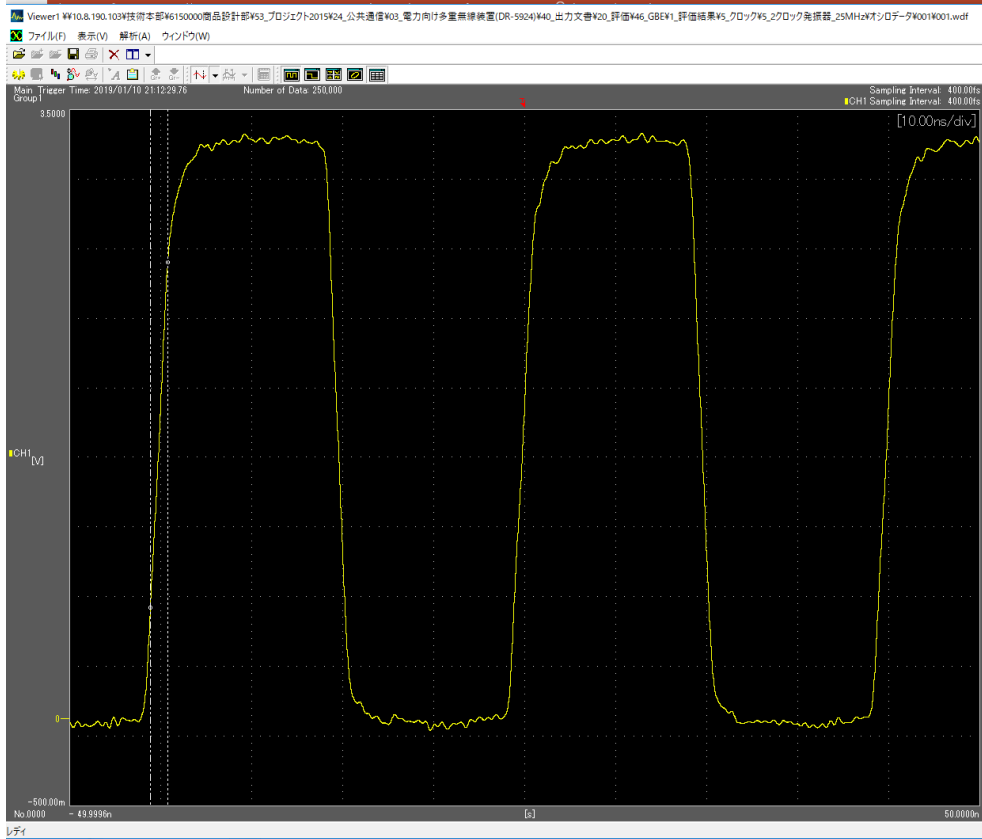
XU4001
2725T-25.000000M-NSA6293E
CMOS出力

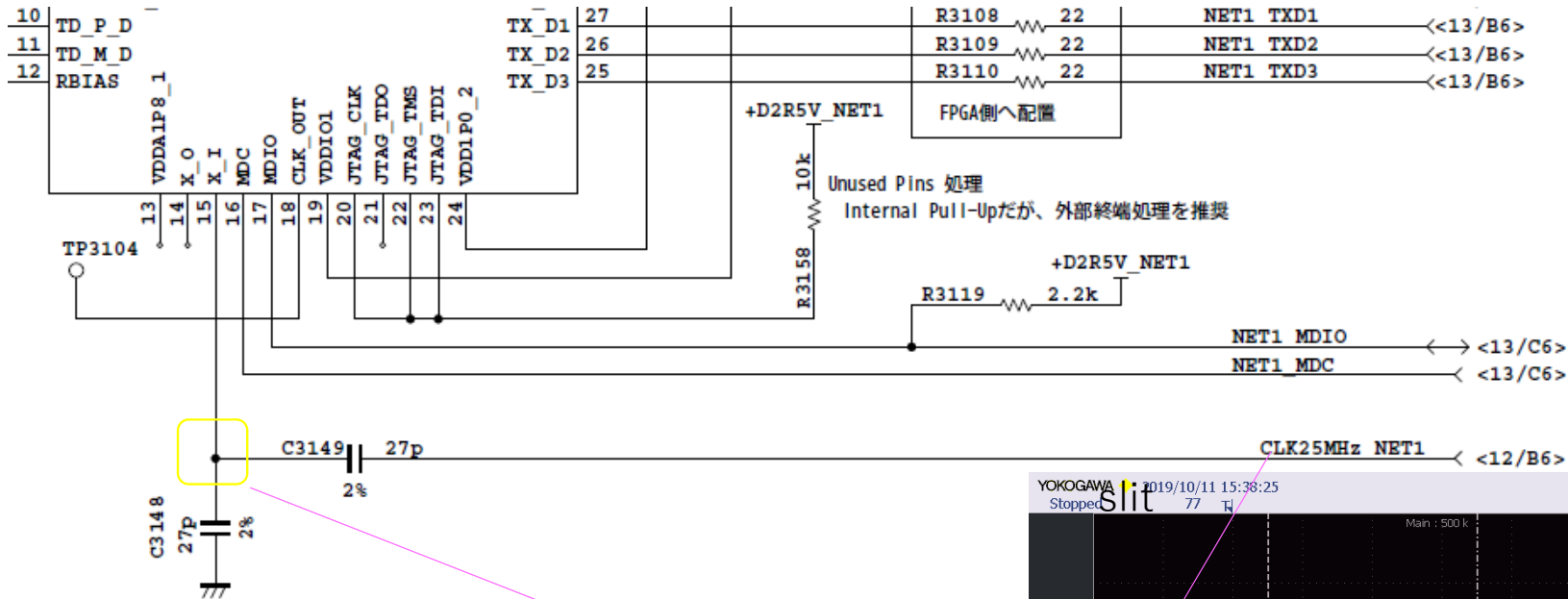
ST H : output ON
L : High impedance
open : output ON

Clock Distribution

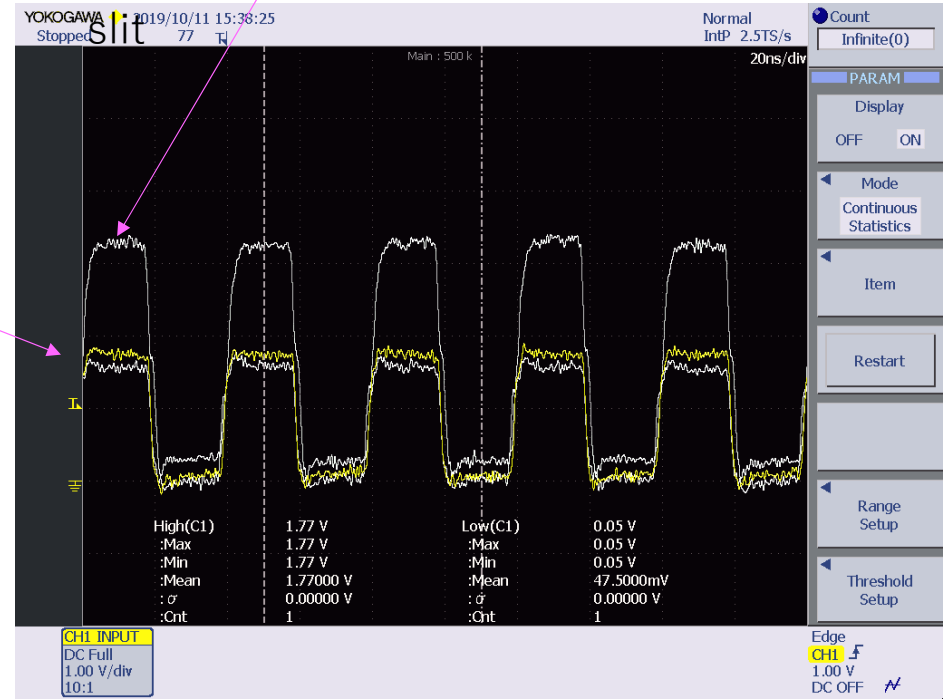
TP4001:CLK25MHZ_NET1

TP4008





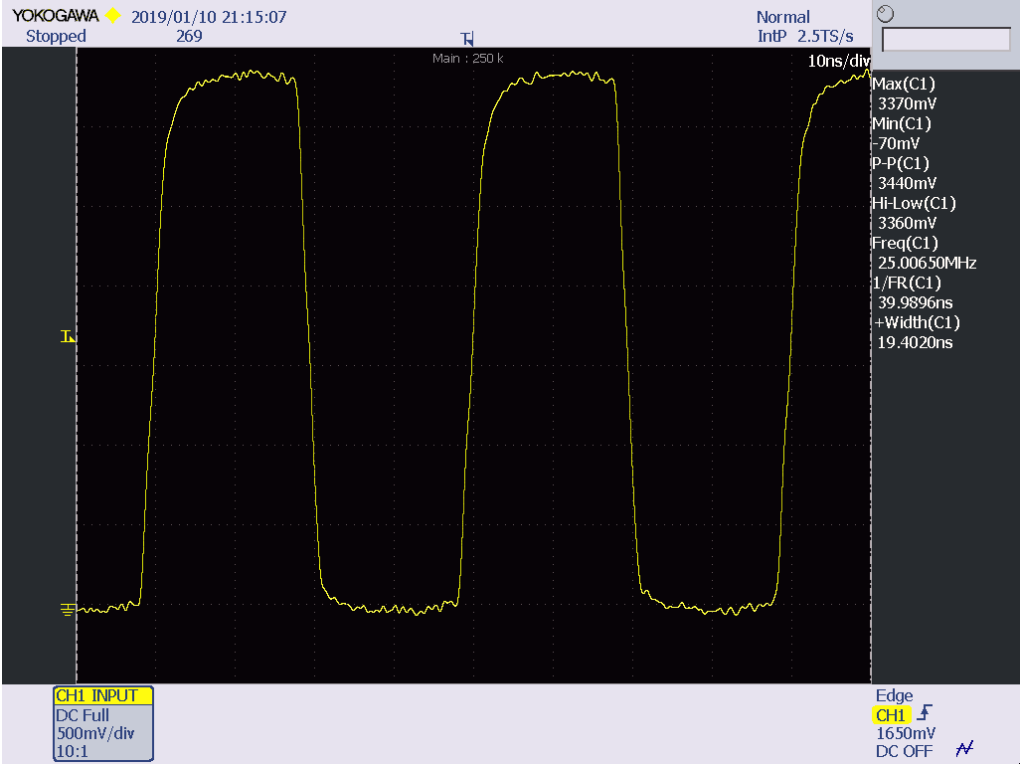
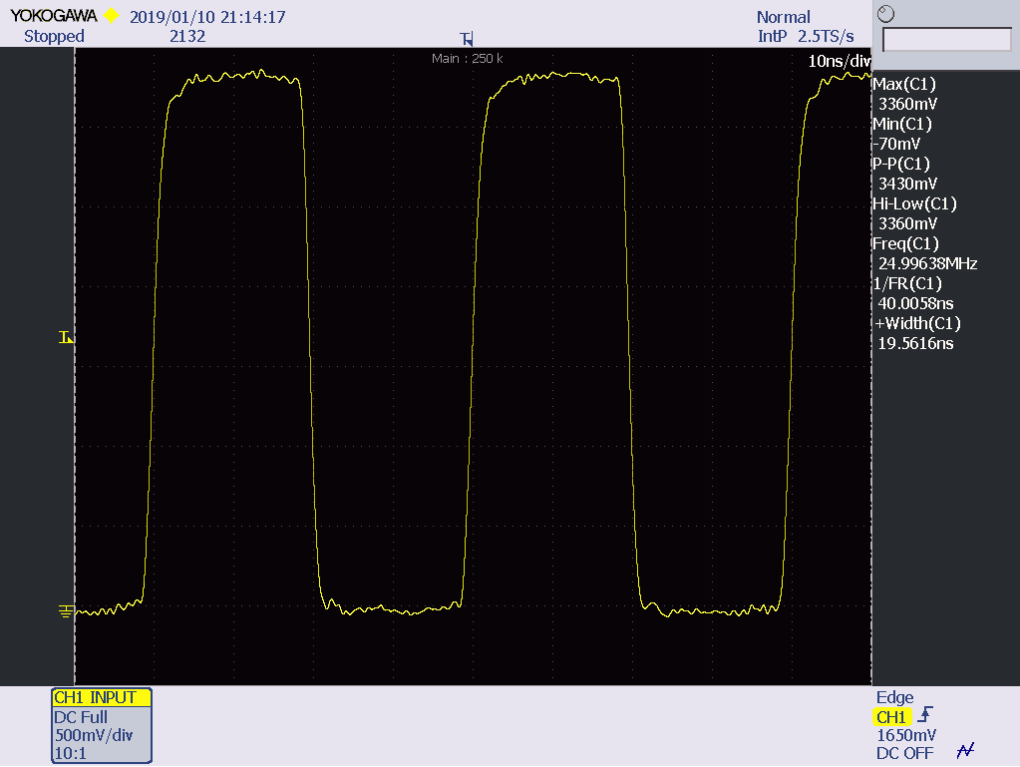
Yellow
 $V_h = 1.77V$
 $V_l = 0.05V$



Clock Distribution

TP4002:CLK25MHZ_NET2

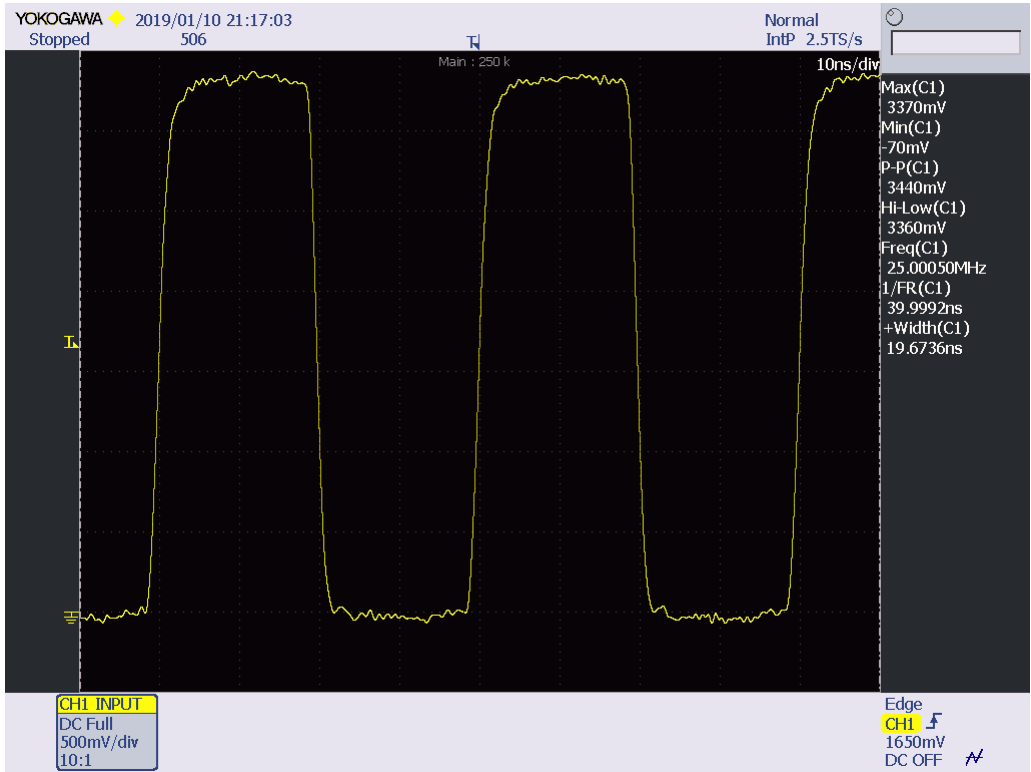
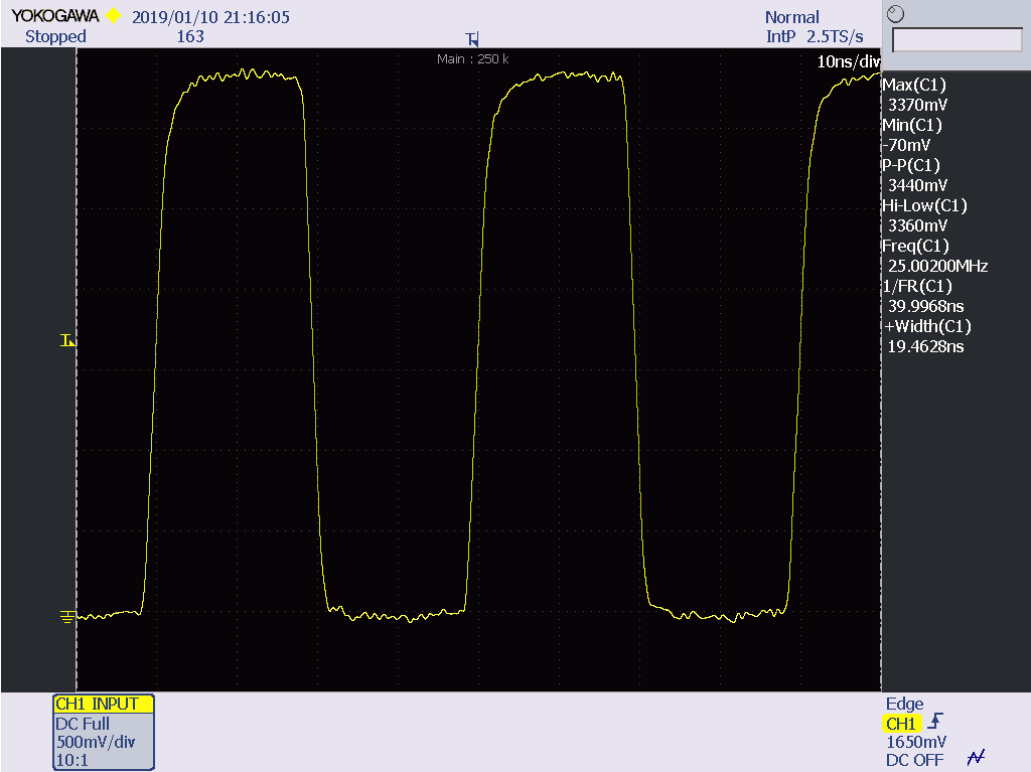
TP4003:CLK25MHZ_NET3



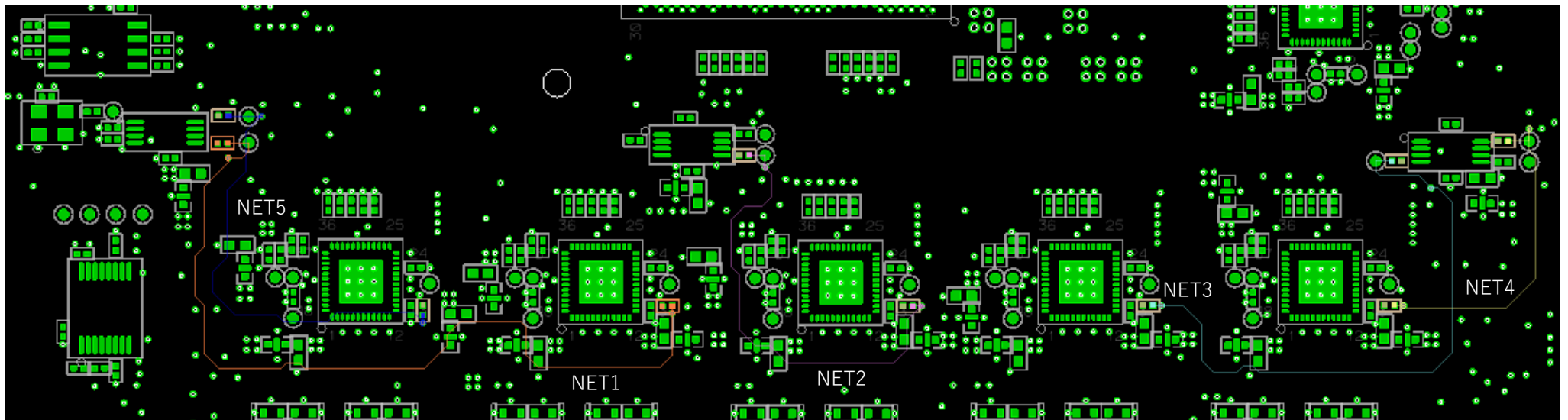
Clock Distribution

TP4004:CLK25MHZ_NET4

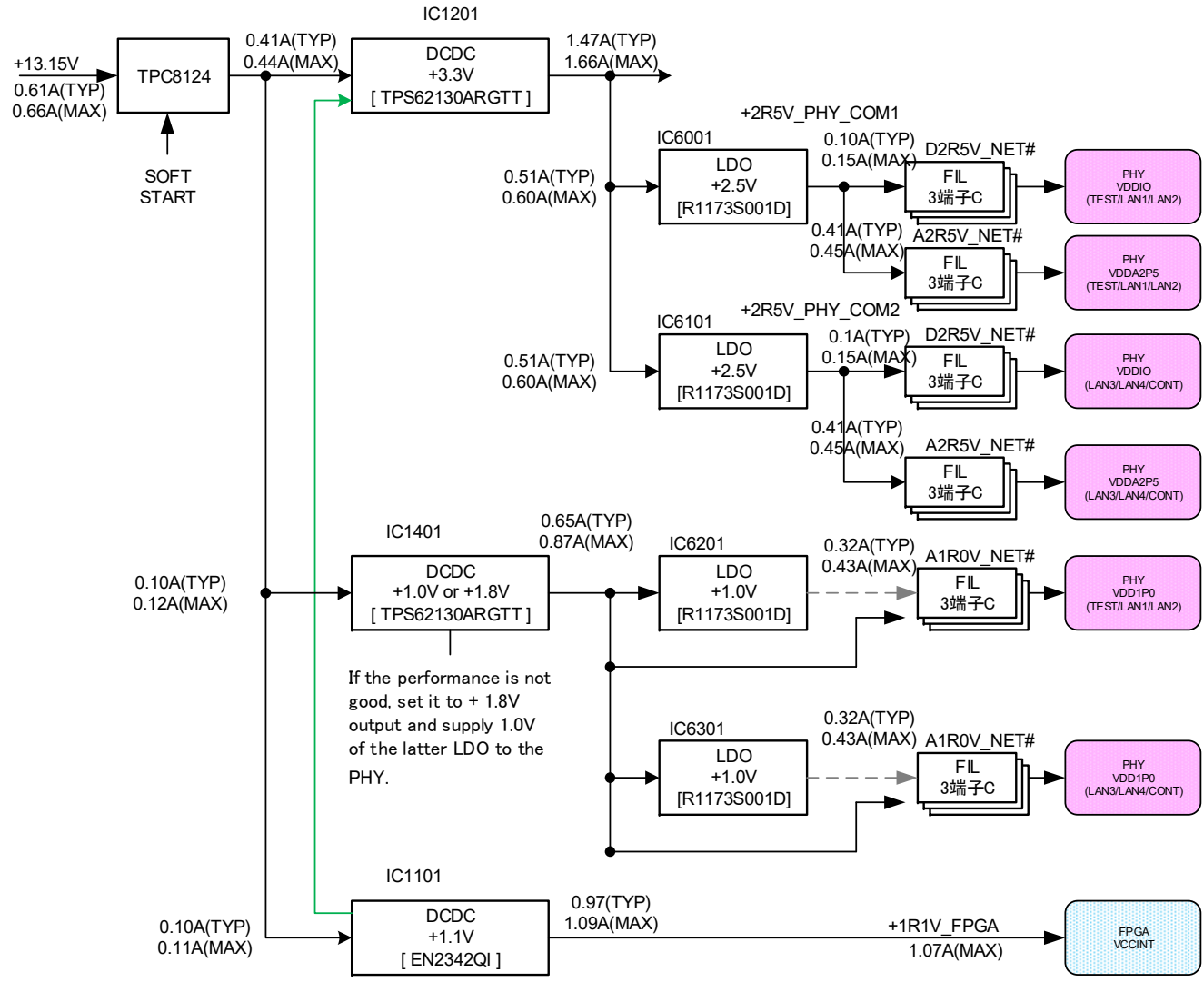
TP4005:CLK25MHZ_NET5

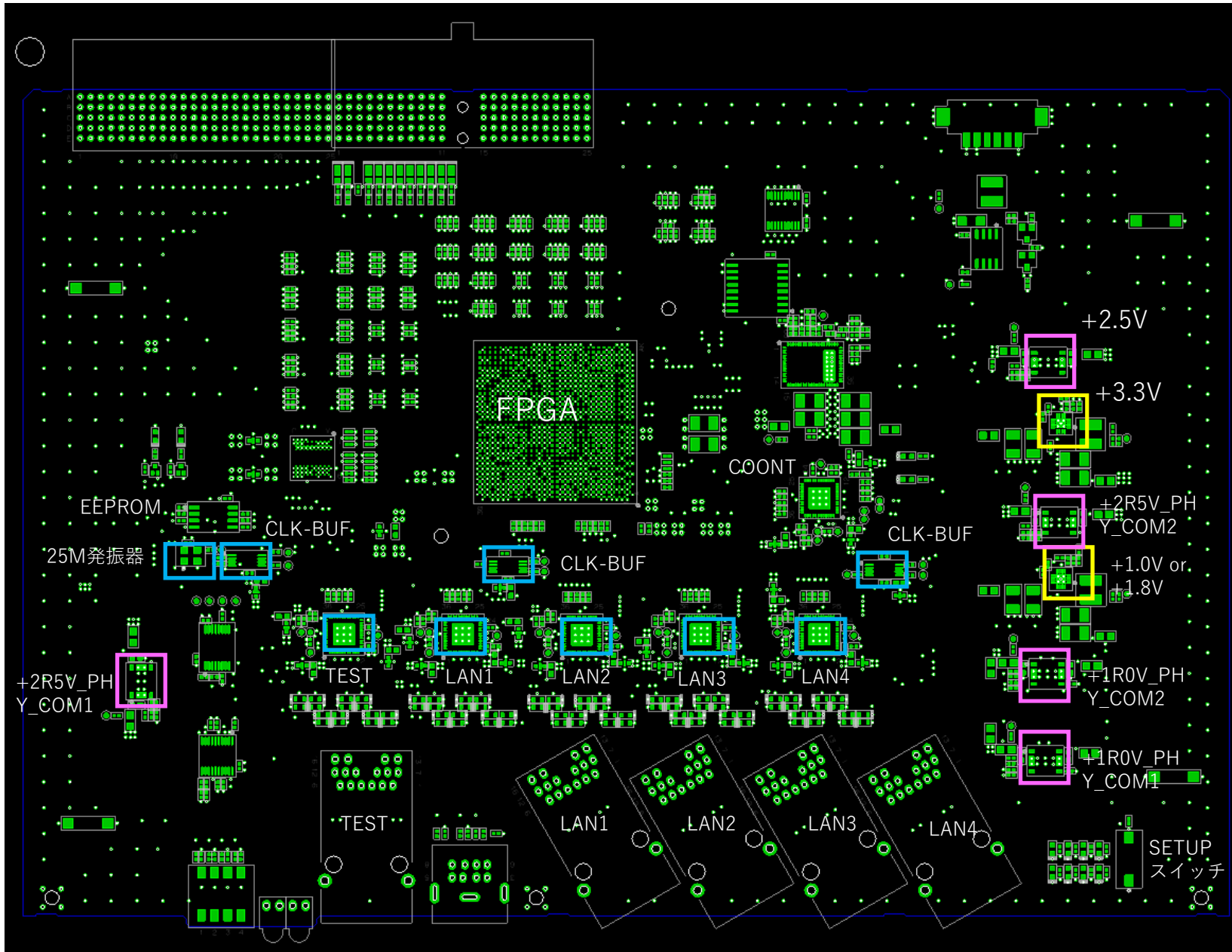


Clock Distribution



Power Supply Tree





SW-DC

LDO

EOF