Schematic Review Form

Pin #	Name	Info	Violations	*Description*
N/A	RX0-R	AC coupling present good.		Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs need to be AC coupled.
N/A	TX0-T)		Please ensure AC coupling is present in signal chain.	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs. These outputs need to be AC coupled.
F1	CAL_C		CAL_CLK_IN is not 3.3V tolerant. Please use 2.5V clock.	25 MHz (±100 PPM) 2.5-V single-ended clock from external oscillator. No stringent phase noise or jitter requirements on this clock. Used to calibrate VCO frequency range. In JTAG mode (EN_SMB = 1 kΩ to GND), this is JTAG Test Data In (TDI).
F11	CAL_C	Good		2.5-V buffered replica of calibration clock input (pin E1) for connecting multiple devices in a daisy-chained fashion. In JTAG mode (EN_SMB = 1 kΩ to GND), this is JTAG Test Data Out (TDO).
D11	ADDR(	Good, addr 0x4E selected.		4-level strap pins used to set the SMBus address of the device. The pin state is read on power-up. The multi-level nature of these pins allows for 16 unique device addresses. The four strap options include: 0: 1 kΩ to GND R: 20 kΩ to GND F: Float 1: 1 kΩ to VDD Refer to Device SMBus Address for more information. In JTAG mode (EN_SMB = 1 kΩ to GND), ADDR1 is JTAG Test Reset (TRS).

D1	ADDR	Good, addr 0x4E selected.		4-level strap pins used to set the SMBus address of the device. The pin state is read on power-up. The multi-level nature of these pins allows for 16 unique device addresses. The four strap options include: 0: 1 kΩ to GND R: 20 kΩ to GND F: Float 1: 1 kΩ to VDD Refer to Device SMBus Address for more information. In JTAG mode (EN_SMB = 1 kΩ to GND), ADDR1 is JTAG Test Reset (TRS).
G1	EN_SM	Good, selects SMBus target (slave) mode.		Four-level 2.5-V input used to select between SMBus master mode (float) and SMBus slave mode (high). The four defined levels are: 0: 1 kΩ to GND - JTAG mode; certain pins take on JTAG functionality R: 20 kΩ to GND - RESERVED, TI test mode F: Float - SMBus Master Mode 1: 1 kΩ to VDD - SMBus Slave Mode
G11	SDA	4.7k pullup (good).		SMBus data input / open drain output. External 2-kΩ to 5-kΩ pull-up resistor is required as per SMBus interface standard. This pin is 3.3V-tolerant.
H11	SDC	4.7k pullup (good).		SMBus clock input / open drain clock output. External 2-kΩ to 5-kΩ pull-up resistor is required as per SMBus interface standard. This pin is 3.3Vtolerant.
E1	ALL_D	Good	ALL_DONE_N is not 3.3V tolerant. Probably should not have option for pullup R to 3.3V.	Indicates the completion of a valid EEPROM register load operation when in SMBus Master Mode (EN_SMB=Float): High = External EEPROM load failed or incomplete Low = External EEPROM load successful and complete When in SMBus slave mode (EN_SMB=1), this output reflects the status of the READ_EN_N input.

E11	READ_	Pulled high, good.		SMBus Master Mode (EN_SMB=Float): When asserted low, initiates the SMBus master mode EEPROM read function. Once EEPROM read is complete (indicated by assertion of ALL_DONE_N low), this pin can be held low for normal device operation. SMBus Slave Mode (EN_SMB=1): When asserted low, this causes the device to be held in reset (SMBus state machine reset and register reset). This pin should be pulled high or left floating for normal operation in SMBus Slave Mode. This pin is 3.3V-tolerant.
H1	INT_N	Good		Open-drain 3.3-V tolerant active-low interrupt output. This pin is pulled low when an interrupt occurs. The events which trigger an interrupt are programmable through SMBus registers. INT_N can be connected in a wired-OR fashion with other device's interrupt pin. A single pull-up resistor in the 2-kΩ to 5-kΩ range is adequate for the entire INT_N net.
D1(	TEST0	Good		Reserved TI test pins. During normal (non-test-mode) operation, these pins are configured as inputs and therefore they are not affected by the presence of a signal. These pins may be left floating, tied to GND, or connected to a 2.5-V (max) output. In JTAG mode (EN_SMB = 1 kΩ to GND), TEST0 is JTAG Test Clock (TCK) and TEST1 is JTAG Test Mode Select (TMS).
D2	TEST1	Good		Reserved TI test pins. During normal (non-test-mode) operation, these pins are configured as inputs and therefore they are not affected by the presence of a signal. These pins may be left floating, tied to GND, or connected to a 2.5-V (max) output. In JTAG mode (EN_SMB = 1 kΩ to GND), TEST0 is JTAG Test Clock (TCK) and TEST1 is JTAG Test Mode Select (TMS).
E10	TEST2	Good		Reserved TI test pins. During normal (non-test-mode) operation, these pins are configured as inputs and therefore they are not affected by the presence of a signal. These pins may be left floating, tied to GND, or connected to a 2.5-V (max) output.
A3,	GND	Good		Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

C3,	VDD	Decoupling capacitors good.		Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six decoupling capacitors between the DS250DF410's VDD plane and GND as close to the DS250DF410 as possible. For example, four 0.1-µF capacitors and two 1-µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a low resistance path to the board VDD plane.

Comments

Violations

TX0-TX3: Please ensure AC coupling is present in signal chain.
CAL_CLK_IN/ JTAG_TDI: CAL_CLK_IN is not 3.3V tolerant. Please use 2.5V clock.
ALL_DONE_N: ALL_DONE_N is not 3.3V tolerant. Probably should not have option for pullup R to 3.3V.