Schematic Review Form

Tejas Networks

Pin #	Name	Info	Violations	*Description*
N/A	RX[7:0] P/N	Good		Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220 nF capacitors assembled on the package substrate.
N/A	TX[7:0] P/N	Please ensure AC coupling is present in signal chain.		Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs.
E1	CAL_CLK_IN	25 MHz clock is not required, but is good to add for potential upgrade to pin-compatible Retimer.		25-MHz (±100 PPM) 2.5-V single-ended clock from external oscillator. No stringent phase noise or jitter requirements on this clock. A 25-MHz input clock is only required if there is a need to support a future upgrade to the pin-compatible Retimer device. If there is no need to support a future upgrade to a pin-compatible Retimer device, then a 25-MHz clock is not required. This input pin has a weak active pull down and can be left floating if the CAL_CLK feature is not required.
E15	CAL_CLK_ OUT	Good		2.5-V buffered replica of calibration clock input (pin E1) for connecting multiple devices in a daisy-chained fashion.
D13, E13	ADDR[1:0]	Good		4-level strap pins used to set the SMBus address of the device. The pin state is read on power-up. The multi-level nature of these pins allows for 16 unique device addresses, see Table 8-1. The four strap options include: 0: 1 kΩ to GND R: 10 kΩ to GND F: Float 1: 1 kΩ to VDD

E3	EN_SMB	Good		4-level 2.5-V input used to select between SMBus master mode (float) and SMBus slave mode (high). The four defined levels are: 0: 1 kΩ to GND - RESERVED R: 10 kΩ to GND - RESERVED, TI test mode F: Float - SMBus master mode 1: 1 kΩ to VDD - SMBus slave mode
E12	SDA	Good; Single set of pull up R present for each bus; Each DS280MB810 has a unique address.		SMBus data input or open drain output. External 2-kΩ to 5-kΩ pull-up resistor is required. This pin is 3.3-V LVCMOS tolerant.
F12	SDC	Good; Single set of pull up R present for each bus; Each DS280MB810 has a unique address.		SMBus clock input or open drain clock output. External 2-kΩ to 5-kΩ pull-up resistor is required. This pin is 3.3-V LVCMOS tolerant.
F13	READ_EN_N	Please note that current configuration will hold devices in reset if external stimulus is not present.		SMBus master mode (EN_SMB = Float): When asserted low, initiates the SMBus master mode EEPROM read function. Once EEPROM read is complete (indicated by assertion of ALL_DONE_N low), this pin can be held low for normal device operation. SMBus slave mode (EN_SMB = 1 kΩ to VDD): When asserted low, this causes the device to be held in reset (SMBus state machine reset and register reset). This pin should be pulled high or left floating for normal operation in SMBus slave mode. This pin has an internal weak pull-up and is 3.3-V LVCMOS tolerant.
D3	ALL_DONE_N	Good		Indicates the completion of a valid EEPROM register load operation when in SMBus master mode (EN_SMB = Float): High = External EEPROM load failed or incomplete. Low = External EEPROM load successful and complete.

				When in SMBus slave mode (EN_SMB = 1 kΩ to VDD), this output will be high-Z until READ_EN_N is driven low, at which point ALL_DONE_N will be driven low. This behavior allows the reset signal connected to READ_EN_N of one device to propagate to the subsequent devices when ALL_DONE_N is connected to READ_EN_N in an SMBus slave mode application.
F3	INT_N	Good		No connect on package. For applications using DS280MB810 and pin-compatible TI Retimers, this pin can be connected to other devices' INT_N pins. This is a recommendation for cases where there is a need to support a potential future upgrade to the pin-compatible Retimer device, which uses this pin as an interrupt signal to a system controller.
E2, E14	MUXSEL0_ TEST0 / MUXSEL1_ TEST1	Good		When operating the cross-point in pin-control mode (Shared Reg_0x05[1]=1), MUXSEL0 controls the cross-point for channels 0–1 and 4–5, and MUXSEL1 controls the cross-point for channels 2–3 and 6–7. If these pins are not used for cross-point control, they may be left floating or tied to GND. These pins also serve as TI test pins when in test mode (EN_SMB = 10 kΩ to GND). These pins have an internal weak pull-up.
N/A	VDD	Good, decoupling adequate.		Power supply, VDD = 2.5 V +/- 5%. Use at least six de-coupling capacitors between the Repeater's VDD plane and GND as close to the Repeater as possible. For example, four 0.1-µF capacitors and two 1-µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a low resistance path to the board VDD plane. For more information, see Section 10.

Comments