** Power Down Mode
1V1_SERDES_DSI : 140mA
1V8_SERDES_DSI : 19mA

1V8_VCC
1V1_VCC

L4506
BLM18PG121SZ1D

L4507
BLM18PG121SZ1D

(MAX 55mA)
1V8_SERDES_HUD

(MAX 500mA)
1V1_SERDES_HUD

Artwork 시 IC와 근접 배치
(Bypass CAP 은 낮은 용량 부터 IC Pin 에 근접 배치)

106P/6.3V/Q C3621
105P/16V/1608/Q C3619
104P/16V/Q C3620

106P/6.3V/Q C3624
105P/16V/1608/Q C3622
104P/16V/Q C3623

105P/16V/1608/Q C3625
104P/16V/Q C3626

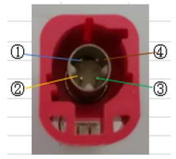
105P/16V/1608/Q C3627
104P/16V/Q C3628

Artwork 시 IC와 근접 배치
(Bypass CAP 은 낮은 용량 부터 IC Pin 에 근접 배치)

C3629 106P/6.3V/Q
C3631 105P/16V/1608/Q
C3630 104P/16V/Q
C3632 104P/16V/Q
C3633 106P/6.3V/Q
C3638 105P/16V/1608/Q
C3639 104P/16V/Q
C3640 104P/16V/Q
C3641 104P/16V/Q
C3642 104P/16V/Q
C3643 106P/6.3V/Q
C3645 105P/16V/1608/Q
C3644 104P/16V/Q
C3646 104P/16V/Q
C3647 106P/6.3V/Q
C3649 105P/16V/1608/Q
C3648 104P/16V/Q

J8409
D4S20W-40MA5-Y

HUD_FPD_LINK0+ 1
HUD_FPD_LINK1- 2
HUD_FPD_LINK0- 3
HUD_FPD_LINK1+ 4
5 IC_FPD_LINK0+ [33]
6 IC_FPD_LINK1- [33]
7 IC_FPD_LINK0- [33]
8 IC_FPD_LINK1+ [33]
9 10 11



1	FPD_LINK0+
2	FPD_LINK1-
3	FPD_LINK0-
4	FPD_LINK1+
5	SH

Table 8-9. Strap Configuration MODE_SEL0

MODE NO.	V_{RS} VOLTAGE			V_{RS} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		SPLITTER	DSI LANES
	V_{MIN}	V_{TYP}	V_{MAX}	$V_{(VDD18)} = 1.8$ V	R_3 (kΩ)	R_4 (kΩ)		
0	0	0	0.126 × $V_{(VDD18)}$	0	OPEN	10.0	0	1
1	0.179 × $V_{(VDD18)}$	0.211 × $V_{(VDD18)}$	0.244 × $V_{(VDD18)}$	0.38	73.2	20.0	0	2
2	0.286 × $V_{(VDD18)}$	0.325 × $V_{(VDD18)}$	0.364 × $V_{(VDD18)}$	0.585	60.4	30.1	0	3
3	0.404 × $V_{(VDD18)}$	0.441 × $V_{(VDD18)}$	0.472 × $V_{(VDD18)}$	0.794	51.1	40.2	0	4
4	0.526 × $V_{(VDD18)}$	0.556 × $V_{(VDD18)}$	0.590 × $V_{(VDD18)}$	1.001	40.2	51.1	1	1
5	0.643 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.708 × $V_{(VDD18)}$	1.211	30.1	61.9	1	2
6	0.763 × $V_{(VDD18)}$	0.790 × $V_{(VDD18)}$	0.825 × $V_{(VDD18)}$	1.421	18.7	71.5	1	3
7	0.880 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	1	4

Table 8-10. Strap Configuration MODE_SEL1

MODE NO.	V_{RS} VOLTAGE			V_{RS} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		CLOCK	COAX	DISABLE DSI
	V_{MIN}	V_{TYP}	V_{MAX}	$V_{(VDD18)} = 1.8$ V	R_3 (kΩ)	R_4 (kΩ)			
0	0	0	0.126 × $V_{(VDD18)}$	0	OPEN	10.0	1	0	0
1	0.179 × $V_{(VDD18)}$	0.211 × $V_{(VDD18)}$	0.244 × $V_{(VDD18)}$	0.380	73.2	20.0	1	0	1
2	0.286 × $V_{(VDD18)}$	0.325 × $V_{(VDD18)}$	0.364 × $V_{(VDD18)}$	0.585	60.4	30.1	1	1	0
3	0.404 × $V_{(VDD18)}$	0.441 × $V_{(VDD18)}$	0.472 × $V_{(VDD18)}$	0.794	51.1	40.2	1	1	1
4	0.526 × $V_{(VDD18)}$	0.556 × $V_{(VDD18)}$	0.590 × $V_{(VDD18)}$	1.001	40.2	51.1	0	0	0
5	0.643 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.708 × $V_{(VDD18)}$	1.211	30.1	61.9	0	0	1
6	0.763 × $V_{(VDD18)}$	0.790 × $V_{(VDD18)}$	0.825 × $V_{(VDD18)}$	1.421	18.7	71.5	0	1	0
7	0.880 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	0	1	1

Table 8-12. Serial Control Bus Addresses for IDX

NO.	V_{IDX} VOLTAGE RANGE			V_{IDX} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		ASSIGNED I2C ADDRESS	
	V_{MIN}	V_{TYP}	V_{MAX}	$V_{(VDD18)} = 1.8$ V	R_1 (kΩ)	R_2 (kΩ)	7-BIT	8-BIT
0	0	0	0.135 × $V_{(VDD18)}$	0	OPEN	10.0	0x0C	0x18
1	0.176 × $V_{(VDD18)}$	0.213 × $V_{(VDD18)}$	0.247 × $V_{(VDD18)}$	0.38	73.2	20.0	0x0E	0x1C
2	0.289 × $V_{(VDD18)}$	0.327 × $V_{(VDD18)}$	0.363 × $V_{(VDD18)}$	0.589	60.4	30.1	0x10	0x20
3	0.407 × $V_{(VDD18)}$	0.441 × $V_{(VDD18)}$	0.467 × $V_{(VDD18)}$	0.793	51.1	40.2	0x12	0x24
4	0.526 × $V_{(VDD18)}$	0.555 × $V_{(VDD18)}$	0.584 × $V_{(VDD18)}$	0.999	40.2	51.1	0x14	0x28
5	0.640 × $V_{(VDD18)}$	0.671 × $V_{(VDD18)}$	0.701 × $V_{(VDD18)}$	1.208	30.1	61.9	0x16	0x2C
6	0.757 × $V_{(VDD18)}$	0.787 × $V_{(VDD18)}$	0.814 × $V_{(VDD18)}$	1.417	18.7	71.5	0x18	0x30
7	0.877 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10	OPEN	0x1A	0x34

U8026
DS90UB941AS-Q1

VDD18 24, VDD18 61
VDDIO 16, VDDIO 33
VDD11_L 9, VDD11_A 12
VDD11_P0 17, VDD11_HS1 21, VDD11_S 25, VDD11_HS0 28
VDD11_L 42, VDD11_P1 50
VDD11_DSI 64

1.71V ~ 1.89V
1.045V ~ 1.155V

R2575 OPEN-101/F
[4] CPU_HUD_DSI_A_CLK_P 60 DSI0_CLKP
[4] CPU_HUD_DSI_A_CLK_N 59 DSI0_CLKN

R2576 OPEN-101/F
[4] CPU_HUD_DSI_A_D0_P 58 DSI0_D0P
[4] CPU_HUD_DSI_A_D0_N 57 DSI0_D0N

R2577 OPEN-101/F
[4] CPU_HUD_DSI_A_D1_P 56 DSI0_D1P
[4] CPU_HUD_DSI_A_D1_N 55 DSI0_D1N

R2578 OPEN-101/F
[4] CPU_HUD_DSI_A_D2_P 54 DSI0_D2P
[4] CPU_HUD_DSI_A_D2_N 53 DSI0_D2N

R2579 OPEN-101/F
[4] CPU_HUD_DSI_A_D3_P 52 DSI0_D3P
[4] CPU_HUD_DSI_A_D3_N 51 DSI0_D3N

I3469 8 DSI1_CLKP
I3470 7 DSI1_CLKN
I3471 6 DSI1_D0P
I3472 5 DSI1_D0N
I3473 4 DSI1_D1P
I3474 3 DSI1_D1N
I3475 2 DSI1_D2P
I3476 1 DSI1_D2N
I3477 63 DSI1_D3P
I3478 62 DSI1_D3N

[8] CPU_HUD_DSI_A_PWDN R2586 102 31 PDB
Internal Pull Down 50Kohm
Low Power Down

I3466 34 I2S_WC/GPIO7/REG
I3467 35 I2S_CLK/GPIO8/REG
I3468 36 I2S_DA/GPIO6_REG
I3453 37 I2S_DB/GPIO5_REG
I3454 38 I2S_DC/GPIO2
I3455 39 I2S_DC/GPIO3

DOUT0+ 27 C3650 104P/50V/Q HUD_FPD_LINK0+
DOUT0- 26 C3651 104P/50V/Q HUD_FPD_LINK0-
DOUT1+ 23 C3652 104P/50V/Q HUD_FPD_LINK1+
DOUT1- 22 C3653 104P/50V/Q HUD_FPD_LINK1-

DSI Loop Filter LFDSI 49 C3654 103P/50V/Q

REFCLK0 41 R2593 OPEN-000
If unused REFCLK, floating or connect GND.

FPD-LINK3 Loop Filter LFT 20 C3655 103P/50V/Q

IDX 19 HUD_I2C_ADDR

MODE_SEL0 18 HUD_MODE_SEL0

MODE_SEL1 32 HUD_MODE_SEL1

1V8_SERDES_HUD
R3224
R3190
OPEN-472
472

D_GPIO0/MOSI 46 I3456
D_GPIO1/MISO 45 I3457
D_GPIO2/SPLK 44 I3458
D_GPIO3/SS 43 I3459

I2C_SDA 48 CPU_HUD_I2C_SDA [6]
I2C_SCL 47 CPU_HUD_I2C_SCL [6]

INTB 30 HUD_CPU_DSI_A_INTB [8]
REM_INTB 10 R2595 OPEN-000 HUD_CPU_DSI_A_REM_INTB [8]

GPIO0 14 I3460
GPIO1 15 I3461
REFCLK1 11 R2594 OPEN-000
If unused REFCLK, floating or connect GND.

RES2 13
RES1 40
RES0 29

DAP_GND 65

1V8_SERDES_HUD
R3146 5112/F/Q
R3188 OPEN
R3144 OPEN
HUD_MODE_SEL0
HUD_MODE_SEL1
HUD_I2C_ADDR
R3187 4022/F
R3189 103/F
R3145 103/F

**** Configulation SET**

MODE_SEL0	No SPLITTER / DSI 4 LANE
MODE_SEL1	STP / DSI ENABLE
I2C_ADDR	I2C Device Adress : 0X18 (8 bit)

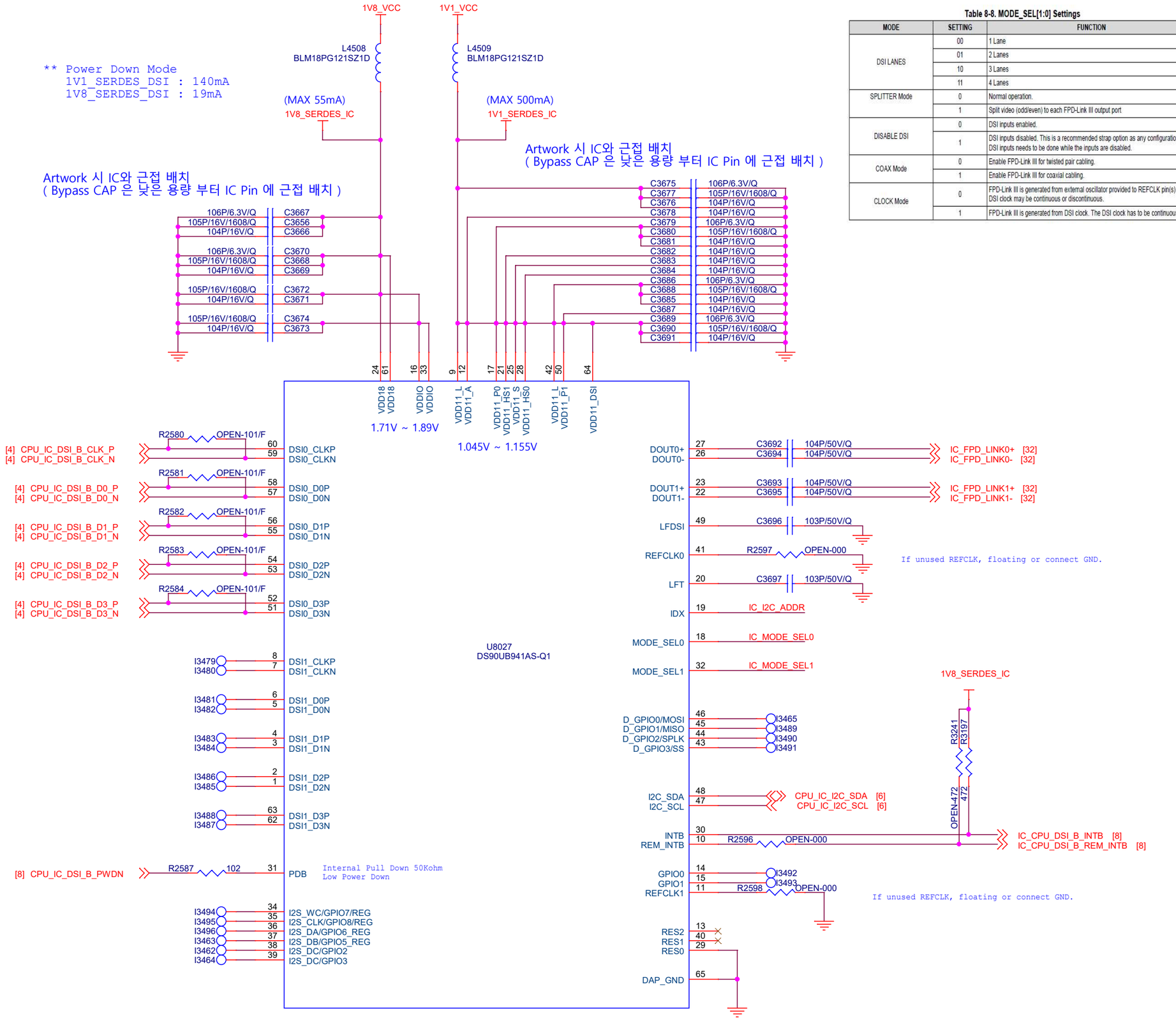


Table 8-8. MODE_SEL[1:0] Settings

MODE	SETTING	FUNCTION
DSI LANES	00	1 Lane
	01	2 Lanes
	10	3 Lanes
	11	4 Lanes
SPLITTER Mode	0	Normal operation.
	1	Split video (odd/even) to each FPD-Link III output port
DISABLE DSI	0	DSI inputs enabled.
	1	DSI inputs disabled. This is a recommended strap option as any configuration of DSI inputs needs to be done while the inputs are disabled.
COAX Mode	0	Enable FPD-Link III for twisted pair cabling.
	1	Enable FPD-Link III for coaxial cabling.
CLOCK Mode	0	FPD-Link III is generated from external oscillator provided to REFCLK pin(s). The DSI clock may be continuous or discontinuous.
	1	FPD-Link III is generated from DSI clock. The DSI clock has to be continuous.

Table 8-9. Strap Configuration MODE_SEL0

MODE NO.	V_{RS} VOLTAGE			V_{RS} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		SPLITTER	DSI LANES
	V_{MIN}	V_{TYP}	V_{MAX}	$V_{(VDD18)}$ = 1.8 V	R_3 (kΩ)	R_4 (kΩ)		
0	0	0	0.126 × $V_{(VDD18)}$	0	OPEN	10.0	0	1
1	0.179 × $V_{(VDD18)}$	0.211 × $V_{(VDD18)}$	0.244 × $V_{(VDD18)}$	0.38	73.2	20.0	0	2
2	0.286 × $V_{(VDD18)}$	0.325 × $V_{(VDD18)}$	0.364 × $V_{(VDD18)}$	0.585	60.4	30.1	0	3
3	0.404 × $V_{(VDD18)}$	0.441 × $V_{(VDD18)}$	0.472 × $V_{(VDD18)}$	0.794	51.1	40.2	0	4
4	0.526 × $V_{(VDD18)}$	0.556 × $V_{(VDD18)}$	0.590 × $V_{(VDD18)}$	1.001	40.2	51.1	1	1
5	0.643 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.708 × $V_{(VDD18)}$	1.211	30.1	61.9	1	2
6	0.763 × $V_{(VDD18)}$	0.790 × $V_{(VDD18)}$	0.825 × $V_{(VDD18)}$	1.421	18.7	71.5	1	3
7	0.880 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	1	4

Table 8-10. Strap Configuration MODE_SEL1

MODE NO.	V_{RS} VOLTAGE			V_{RS} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		CLOCK	COAX	DISABLE DSI
	V_{MIN}	V_{TYP}	V_{MAX}	$V_{(VDD18)}$ = 1.8 V	R_1 (kΩ)	R_2 (kΩ)			
0	0	0	0.126 × $V_{(VDD18)}$	0	OPEN	10.0	1	0	0
1	0.179 × $V_{(VDD18)}$	0.211 × $V_{(VDD18)}$	0.244 × $V_{(VDD18)}$	0.380	73.2	20.0	1	0	1
2	0.286 × $V_{(VDD18)}$	0.325 × $V_{(VDD18)}$	0.364 × $V_{(VDD18)}$	0.585	60.4	30.1	1	1	0
3	0.404 × $V_{(VDD18)}$	0.441 × $V_{(VDD18)}$	0.472 × $V_{(VDD18)}$	0.794	51.1	40.2	1	1	1
4	0.526 × $V_{(VDD18)}$	0.556 × $V_{(VDD18)}$	0.590 × $V_{(VDD18)}$	1.001	40.2	51.1	0	0	0
5	0.643 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.708 × $V_{(VDD18)}$	1.211	30.1	61.9	0	0	1
6	0.763 × $V_{(VDD18)}$	0.790 × $V_{(VDD18)}$	0.825 × $V_{(VDD18)}$	1.421	18.7	71.5	0	1	0
7	0.880 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	0	1	1

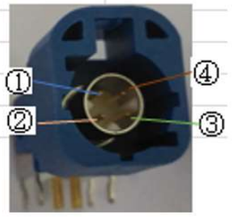
Table 8-12. Serial Control Bus Addresses for IDX

NO.	V_{IDX} VOLTAGE RANGE			V_{IDX} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		ASSIGNED I2C ADDRESS	
	V_{MIN}	V_{TYP}	V_{MAX}	$V_{(VDD18)}$ = 1.8 V	R_1 (kΩ)	R_2 (kΩ)	7-BIT	8-BIT
0	0	0	0.135 × $V_{(VDD18)}$	0	OPEN	10.0	0x0C	0x18
1	0.176 × $V_{(VDD18)}$	0.213 × $V_{(VDD18)}$	0.247 × $V_{(VDD18)}$	0.384	73.2	20.0	0x0E	0x1C
2	0.289 × $V_{(VDD18)}$	0.327 × $V_{(VDD18)}$	0.363 × $V_{(VDD18)}$	0.589	60.4	30.1	0x10	0x20
3	0.407 × $V_{(VDD18)}$	0.441 × $V_{(VDD18)}$	0.467 × $V_{(VDD18)}$	0.793	51.1	40.2	0x12	0x24
4	0.526 × $V_{(VDD18)}$	0.555 × $V_{(VDD18)}$	0.584 × $V_{(VDD18)}$	0.999	40.2	51.1	0x14	0x28
5	0.640 × $V_{(VDD18)}$	0.671 × $V_{(VDD18)}$	0.701 × $V_{(VDD18)}$	1.208	30.1	61.9	0x16	0x2C
6	0.757 × $V_{(VDD18)}$	0.787 × $V_{(VDD18)}$	0.814 × $V_{(VDD18)}$	1.417	18.7	71.5	0x18	0x30
7	0.877 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10	OPEN	0x1A	0x34

**** Configulation SET**

MODE_SEL0	No SPLITTER / DSI 4 LANE
MODE_SEL1	STP / DSI ENABLE
I2C_ADDR	I2C Device Adress : 0X34 (8 bit)

** Power Down Mode
1V2_SERDES_DVB-T2 : 30mA
3V3_SERDES_DVB-T2 : 8mA
1V8_SERDES_VDDIO : 0.3mA



J7403

FPD_LINK1+ 1
FPD_LINK0- 2
FPD_LINK1- 3
FPD_LINK0+ 4
5
6
7
8

D4S20L-40MA5-C/Rosenberger

1V2_VCC
(MAX 300mA)
1V2_SERDES_DVB-T2
L4513 BLM18PG121SZ1D

106P/6.3V/Q C3498
105P/16V/1608/Q C3499
104P/16V/Q C3496
103P/50V/Q C3497
103P/50V/Q C3500

106P/6.3V/Q C3701
105P/16V/1608/Q C3702
104P/16V/Q C3700
103P/50V/Q C3501
103P/50V/Q C3502

106P/6.3V/Q C3704
105P/16V/1608/Q C3705
104P/16V/Q C3703
103P/50V/Q C3503
103P/50V/Q C3504
103P/50V/Q C3719

106P/6.3V/Q C3708
105P/16V/1608/Q C3707
104P/16V/Q C3706
103P/50V/Q C3720
103P/50V/Q C3721

3V3_VCC
L4512 BLM18PG121SZ1D
(MAX 122mA)
3V3_SERDES_DVB-T2

1V8_VCC
L4524 BLM18PG121SZ1D
(MAX 6mA)
1V8_SERDES_DVB-T2

C3507 106P/6.3V/Q
C3508 105P/16V/1608/Q
C3505 104P/16V/Q
C3722 103P/50V/Q
C3698 103P/50V/Q

C3510 106P/6.3V/Q
C3511 105P/16V/1608/Q
C3509 104P/16V/Q
C3699 103P/50V/Q

Common Mode Filter C3512 104P/16V/Q
C3713 104P/16V/Q

51 VDDP12_CH0
52 VDDR12_CH0
60 VDDP12_CH1
57 VDDR12_CH1
20 VDD12_CSI0
33 VDD12_CSI1
32 VDDP12_CSI
6 VDDL12_0
44 VDDL12_1
56 VDD33_A
31 VDD33_B
3 VDDIO
55 CMF
2 CAP_I2S

100옴 임피던스

L2545
FPD_LINK0+ 1 2
FPD_LINK0- 4 3
C3709 104P/50V/Q 53 RIN0+
C3710 104P/50V/Q 54 RIN0-
OPEN-DLW21SZ900HQ2

L2546
FPD_LINK1+ 1 2
FPD_LINK1- 4 3
C3712 104P/50V/Q 58 RIN1+
C3711 104P/50V/Q 59 RIN1-
OPEN-DLW21SZ900HQ2

* BIST : Built-In Self Test, High Active
BISTC : 0-PCLK / 1-33MHz

DVB-T2_BISTEN 5 BISTEN
DVB-T2_BISTC 4 BISTC/INTB_IN
[8] CPU_DVB-T2_CSI_B_PWDN R3575 102 48 PDB
R3209 103
102P/50V/Q C3716

R5276 103 19 D_GPIO0/MOSI
R5297 103 18 D_GPIO1/MISO
R5298 103 17 D_GPIO2/SPLK
R5299 103 16 D_GPIO3/SS

* If unused, tie to an external pulldown.

[6] CPU_DVB-T2_I2C_SDA R3552 220/Q 46 I2C_SDA
[6] CPU_DVB-T2_I2C_SCL R3557 220/Q 45 I2C_SCL

* Channel Monitoring Output (Optional)

I3498 C3717 OPEN-104P/50V 63 CMLOUTN
C3718 OPEN-104P/50V 62 CMLOUTP

R3107 OPEN-49R9/F
R3112 OPEN-000 R3108 OPEN-49R9/F
I3499

DVB-T2_IDX 47 IDX
DVB-T2_MODE_SEL0 61 MODE_SEL0
DVB-T2_MODE_SEL1 50 MODE_SEL1

3V3_SERDES_DVB-T2
R3205 OPEN
R3204 OPEN
R3207 6652/F/Q
R3199 OPEN
R3201 OPEN
DVB-T2_IDX
DVB-T2_MODE_SEL0
DVB-T2_MODE_SEL1
DVB-T2_BISTEN
DVB-T2_BISTC
R3206 103/F
R3203 103/F
R3208 203/F
R3200 103
R3202 103

** Configulation SET

CFG0	I2C Device Adress : 0X58
SEL0	4 Data Lanes, 1CSI Port
SEL1	STP 20Mbps

U1
DS90UB940-Q1

CSI0_CLK- 21 DVB_CPU_CSI_B_CLK0_N [3]
CSI0_CLK+ 22 DVB_CPU_CSI_B_CLK0_P [3]
CSI0_D0- 23 DVB_CPU_CSI_B_D0_N [3]
CSI0_D0+ 24 DVB_CPU_CSI_B_D0_P [3]
CSI0_D1- 25 DVB_CPU_CSI_B_D1_N [3]
CSI0_D1+ 26 DVB_CPU_CSI_B_D1_P [3]
CSI0_D2- 27 DVB_CPU_CSI_B_D2_N [3]
CSI0_D2+ 28 DVB_CPU_CSI_B_D2_P [3]
CSI0_D3- 29 DVB_CPU_CSI_B_D3_N [3]
CSI0_D3+ 30 DVB_CPU_CSI_B_D3_P [3]

CSI1_CLK- 34 R5262 OPEN-000 I2417
CSI1_CLK+ 35 R5263 OPEN-000 I2416
CSI1_D0- 36 R5264 OPEN-000 I2418
CSI1_D0+ 37 R5265 OPEN-000 I2419
CSI1_D1- 38 R5266 OPEN-000 I2420
CSI1_D1+ 39 R5267 OPEN-000 I2421
CSI1_D2- 40 R5268 OPEN-000 I2422
CSI1_D2+ 41 R5269 OPEN-000 I2423
CSI1_D3- 42 R5270 OPEN-000 I2424
CSI1_D3+ 43 R5271 OPEN-000 I2425

* Error Detect (1:No Error, 0: Error)
SDOUT/PASS/GPIO0 7
SWC/GPIO1 8 R5272 103
DVB-T2_CPU_PASS [3]

RES0 49 C3714 OPEN-104P/16V
RES1 64 C3715 OPEN-104P/16V

* PLL Lock Detect (1:Lock, 0: Unlock)
LOCK 1
DVB-T2_CPU_LOCK [3]

I2S_WC/GPIO7_REG 14 R5295 100 DVT-T2_DSP_I2S_LRCK [43]
I2S_CLK/GPIO8_REG 13 R5294 100 DVT-T2_DSP_I2S_BCLK [43]
I2S_DA/GPIO6_REG 12 R5293 100 DVB-T2_CPU_I2S_LRCK [2]
I2S_DB/GPIO5_REG 11 R5274 100 DVB-T2_CPU_I2S_BCLK [2]
I2S_DC/GPIO2 10 R5275 100 DVB-T2_CPU_I2S_DOUT [2]
I2S_DD/GPIO3 9 R5296 100 DVT-T2_DSP_I2S_DOUT [43]
MCLK/GPIO9 15
I2426
I2427
I2428
I2429

PAD_GND 65
R5277 103
R5278 103
R5279 103
R5280 103

Table 10. Serial Control Bus Addresses for IDx

NO.	V_{IDX} VOLTAGE	V_{IDX} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOLERANCE)		PRIMARY ASSIGNED I2C ADDRESS	
	V_{TYP}	VDD33 = 3.3 V	R_1 (kΩ)	R_2 (kΩ)	7-BIT	8-BIT
0	0	0	Open	10	0x2C	0x58
1	0.169 × $V_{(VDD33)}$	0.559	73.2	15	0x2E	0x5C
2	0.230 × $V_{(VDD33)}$	0.757	66.5	20	0x30	0x60
3	0.295 × $V_{(VDD33)}$	0.974	59	24.9	0x32	0x64
4	0.376 × $V_{(VDD33)}$	1.241	49.9	30.1	0x34	0x68
5	0.466 × $V_{(VDD33)}$	1.538	46.4	40.2	0x36	0x6C
6	0.556 × $V_{(VDD33)}$	1.835	40.2	49.9	0x38	0x70
7	0.801 x $V_{(VDD33)}$	2.642	18.7	75	0x3C	0x78

Table 7. Configuration Select (MODE_SEL0)

NO.	V_{MODE} VOLTAGE	V_{MODE} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOLERANCE)		OUTPUT MODE
	V_{TYP}	VDD33 = 3.3 V	R_1 (kΩ)	R_2 (kΩ)	
0	0	0	Open	10	4 data lanes. 1 CSI port active (determined by MODE_SEL1 CSI_SEL bit).
1	0.169 × $V_{(VDD33)}$	0.559	73.2	15	4 data lanes. Both CSI ports active (overrides MODE_SEL1).
2	0.230 × $V_{(VDD33)}$	0.757	66.5	20	2 data lanes. 1 CSI port active (determined by MODE_SEL1 CSI_SEL bit).
3	0.295 × $V_{(VDD33)}$	0.974	59	24.9	2 data lanes. Both CSI port active (overrides MODE_SEL1).
4	0.376 × $V_{(VDD33)}$	1.241	49.9	30.1	RESERVED
5	0.466 × $V_{(VDD33)}$	1.538	46.4	40.2	RESERVED
6	0.556 × $V_{(VDD33)}$	1.835	40.2	49.9	RESERVED
7	0.801 × $V_{(VDD33)}$	2.642	18.7	75	RESERVED

Table 8. Configuration Select (MODE_SEL1)

NO.	V_{MODE} VOLTAGE	V_{MODE} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOLERANCE)		CSI_SEL (CSI PORT)	HIGH-SPEED BACK CHANNEL	INPUT MODE
	V_{TYP}	VDD33 = 3.3 V	R_1 (kΩ)	R_2 (kΩ)			
0	0	0	Open	10	CSI0	5 Mbps	STP
1	0.169 × $V_{(VDD33)}$	0.559	73.2	15	CSI0	5 Mbps	Coax
2	0.230 × $V_{(VDD33)}$	0.757	66.5	20	CSI0	20 Mbps	STP
3	0.295 × $V_{(VDD33)}$	0.974	59	24.9	CSI0	20 Mbps	Coax
4	0.376 × $V_{(VDD33)}$	1.241	49.9	30.1	CSI1	5 Mbps	STP
5	0.466 × $V_{(VDD33)}$	1.538	46.4	40.2	CSI1	5 Mbps	Coax
6	0.556 × $V_{(VDD33)}$	1.835	40.2	49.9	CSI1	20 Mbps	STP
7	0.801 × $V_{(VDD33)}$	2.642	18.7	75	CSI1	20 Mbps	Coax