Forvia H97 Serializer Configuration Overview

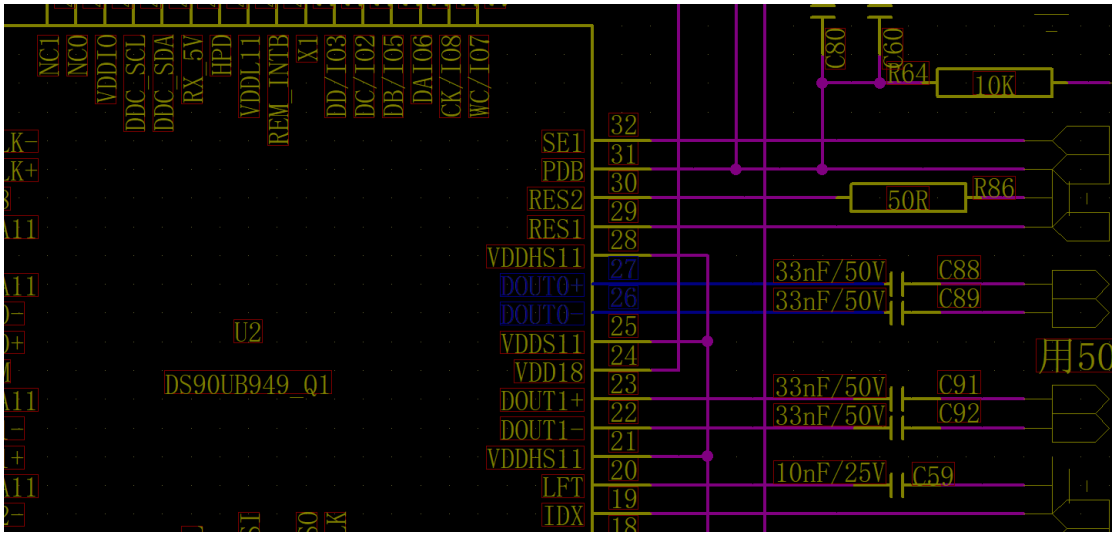
Project Name: H97
Serializer: DS90UB949
Deserializer: DS90UB948
Number of Pixels: 1920×720×60Hz×RGB

1. LVDS：

3.5.3 Timing Parameter

Parameter	Symbol	1920xRGBx720			Unit
		Min.	Typ.	Max.	
CLK frequency	FCLK	47.88	48	48.12	MHZ
Horizontal valid data	thd		960		CLK
Hsync pulse Width	thpw	-	16	-	CLK
Hsync back porch	thbp	-	16	-	CLK
Hsync front porch	thfp	-	32	-	CLK
1 horizontal line	th	1008	1024	1088	CLK
Vertical valid data	tvd		720		H
Vsync pulse width	tvpw	-	8	-	H
Vsync back porch	tvbp	-	8	-	H
Vsync front porch	tvfp	-	45	-	H
1 vertical field	tv	779	781	783	H
Frame rate	FR	60	60	60	Hz

2. Cluster image output port of Serializer (FAKRA, Coax, Single-Channel)

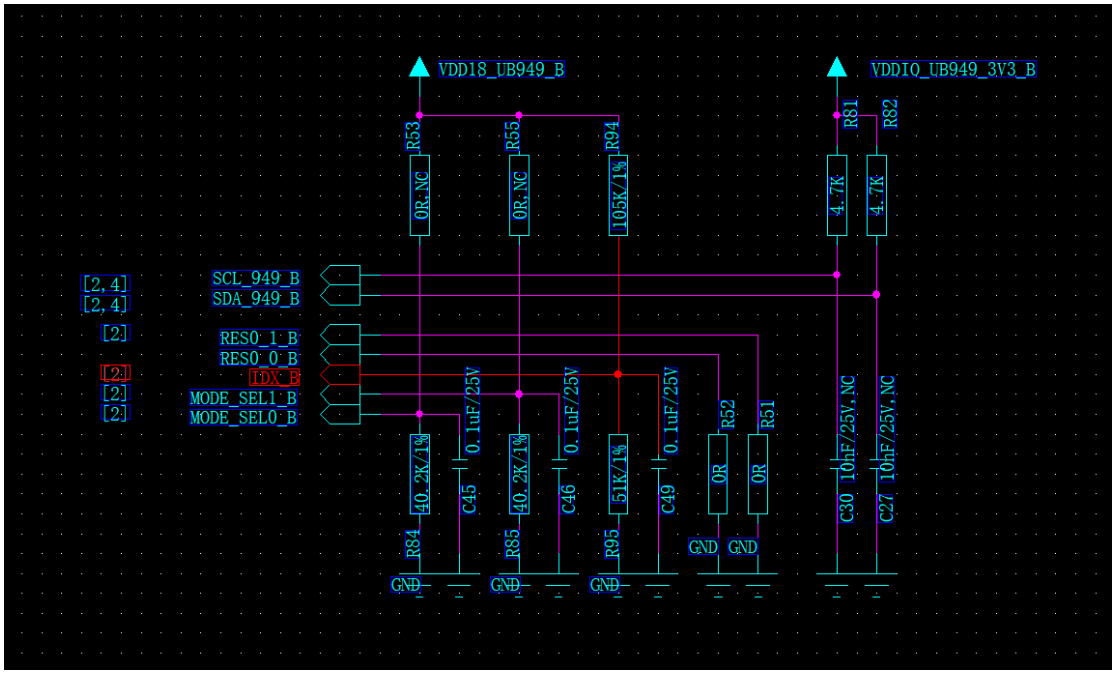


3. Cluster serializer address：

Table 9. Serial Control Bus Addresses For IDx

#	Ratio V_{R2} / V_{DD18}	Ideal V_{R2} (V)	Suggested Resistor R1 kΩ (1% tol)	Suggested Resistor R2 kΩ (1% tol)	7-Bit Address	8-Bit Address
1	0	0	OPEN	40.2	0x0C	0x18
2	0.208	0.374	118	30.9	0x0E	0x1C
3	0.323	0.582	107	51.1	0x10	0x20
4	0.440	0.792	113	88.7	0x12	0x24
5	0.553	0.995	82.5	102	0x14	0x28
6	0.668	1.202	68.1	137	0x16	0x2C
7	0.789	1.420	56.2	210	0x18	0x30
8	1	1.8	13.3	OPEN	0x1A	0x34

Configure PIN for IO



4. Cluster deserializer address

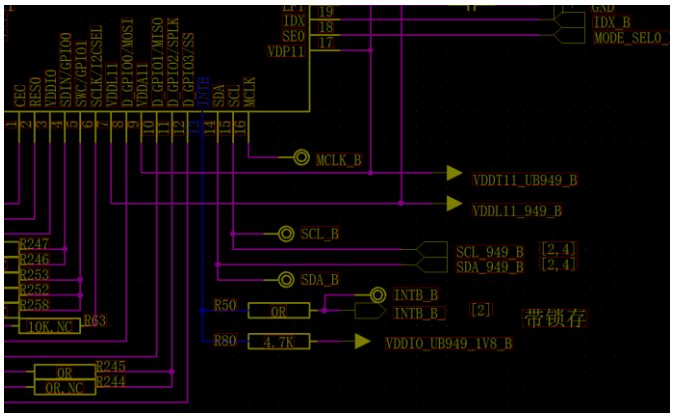
Table 10. Serial Control Bus Addresses for IDx

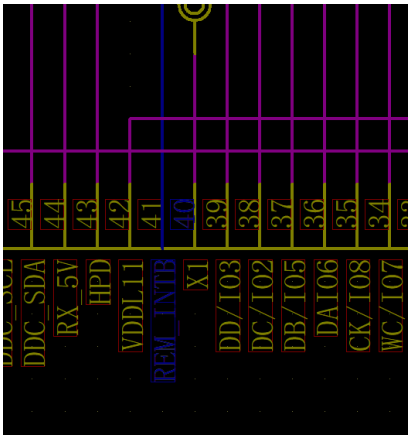
#	Ideal Ratio V_{R2} / VDD33	Ideal V_{R2} (V)	Suggested Resistor R1 kΩ (1% tol)	Suggested Resistor R2 kΩ (1% tol)	7-bit Address	8-bit Address
1	0	0	Open	40.2 or >10	0x2C	0x58
2	0.169	0.559	232	47.5	0x2E	0x5C
3	0.230	0.757	107	31.6	0x30	0x60
4	0.295	0.974	113	47.5	0x32	0x64
5	0.376	1.241	113	68.1	0x34	0x68
6	0.466	1.538	107	93.1	0x36	0x6C
7	0.556	1.835	90.9	113	0x38	0x70
8	0.801	2.642	45.3	182	0x3C	0x78

Cluster: 7Bit 0x2C

Cluster: 8Bit 0x58

5. Cluster serializer interrupt pin





6. I2C Configuration:

I2C rate: 400KB

PassThough

7. 948 Mode selection(Cluster)

Mode0： Dual OLDI output

Table 8. Configuration Select (MODE_SEL0)

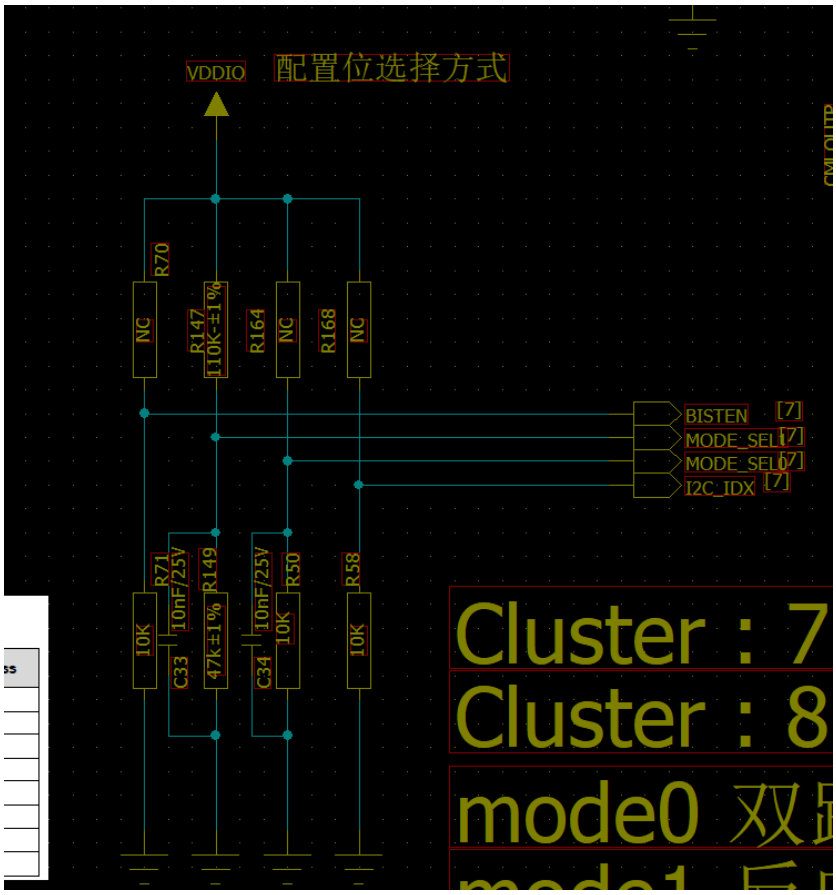
#	Ideal Ratio V_{R1}/VDD33	Target V_{R1} (V)	Suggested Resistor R1 kΩ (1% tol)	Suggested Resistor R2 kΩ (1% tol)	MAP_SEL	OUTPUT_MODE [1:0]	Output Mode
1	0	0	Open	40.2 or Any	0	00	Dual OLDI output
2	0.169	0.559	232	47.5	0	01	Dual SWAP output
3	0.230	0.757	107	31.6	0	10	Single OLDI output
4	0.295	0.974	113	47.5	0	11	Replicate
5	0.376	1.241	113	68.1	1	00	Dual OLDI output
6	0.466	1.538	107	93.1	1	01	Dual SWAP output
7	0.556	1.835	90.9	113	1	10	Single OLDI output
8	0.801	2.642	45.3	182	1	11	Replicate

Mode1 : Coax 20Mbps

Table 9. Configuration Select (MODE_SEL1)

#	Ideal Ratio V_{R1}/VDD33	Target V_{R1} (V)	Suggested Resistor R1 kΩ (1% tol)	Suggested Resistor R2 kΩ (1% tol)	Repeater	MODE	High Speed Back Channel	Input Mode
1	0	0	Open	40.2 or Any	0	00	5 Mbps	STP
2	0.169	0.559	232	47.5	0	01	5 Mbps	Coax
3	0.230	0.757	107	31.6	0	10	20 Mbps	STP
4	0.295	0.974	113	47.5	0	11	20 Mbps	Coax
5	0.376	1.241	113	68.1	1	00	5 Mbps	STP
6	0.466	1.538	107	93.1	1	01	5 Mbps	Coax
7	0.556	1.835	90.9	113	1	10	20 Mbps	STP
8	0.801	2.642	45.3	182	1	11	20 Mbps	Coax

948 corresponding PIN pin configuration:



8. 949 Mode selection(EJmaster)

Table 7. Configuration Select (MODE_SEL0)

#	Ratio V_{R4}/V_{DD18}	Target V_{R4} (V)	Suggested Resistor Pull-Up R3 kΩ (1% tol)	Suggested Resistor Pull-Down R4 kΩ (1% tol)	EDID_SEL	AUTO_SS	AUX_I2S
1	0	0	OPEN	40.2	0	0	0
2	0.208	0.374	118	30.9	0	0	1
3	0.323	0.582	107	51.1	0	1	0
4	0.440	0.792	113	88.7	0	1	1
5	0.553	0.995	82.5	102	1	0	0
6	0.668	1.202	68.1	137	1	0	1
7	0.789	1.420	56.2	210	1	1	0
8	1	1.8	13.3	OPEN	1	1	1

Table 8. Configuration Select (MODE_SEL1)

#	Ratio V_{R6}/V_{DD18}	Target V_{R6} (V)	Suggested Resistor Pull-Up R5 kΩ (1% tol)	Suggested Resistor Pull-Down R6 kΩ (1% tol)	EXT_CTL	COAX	REM_EDID_LOAD
1	0	0	OPEN	40.2	0	0	0
2	0.208	0.374	118	30.9	0	0	1
3	0.323	0.582	107	51.1	0	1	0
4	0.440	0.792	113	88.7	0	1	1
5	0.553	0.995	82.5	102	1	0	0
6	0.668	1.202	68.1	137	1	0	1
7	0.789	1.420	56.2	210	1	1	0
8	1	1.8	13.3	OPEN	1	1	1