ANGUS TECHNOLOGY LIMITED

Tel: (852) 2345 0540 Fax: (852) 2345 9948 Web Site: www.angus.com.hk

Datasheet
V1.03

January 14, 2012

T123AI Video Display Controller

Revisions Note

Revisions	Description of changes	Date	Note
0.8	First draft release	May 17, 2012	
0.9	beta release	Sep 14, 2012	
1.0	official release	Nov 9, 2012	
1.01	fix ADC mux description OSD register offset RGB565 input pin description TTL input endian/swap restriction	Nov 14, 2012	
1.02	add interrupt register set (P6_12~17) information fix RGB888 pin infomation	Nov 23, 2012	
1.03	Add electrical characteristics chapter	Jan 14, 2012	

Contents

1 Introduction

1.1 Features

- **Cost Effective Highly Integrated Triple ADC + ITU656/601 Decoder + digital RGB + 2D Video Decoder + 8051 + OSD + Scalar + TTL + DC-to-DC**
  - Integrates 10-bit Triple Analog to Digital Converters (ADC) & Phase Locked Loop (PLL)
  - Scaler supports 2-D adaptive intra-field de-interlacer and non-linear 16:9 aspect ration.
  - Requires no external Frame Buffer Memory for de-interlacer
  - Integrate CCIR656 and 601 8/16-bit Decoder
  - Support digital RGB565/666/888 inputs
  - Built-in 8051 MCU
  - Advanced On Screen Display (OSD) function
  - Multi-standard color decoder with 2D adaptive comb filter
  - SPI Flash control supports MCU and OSD concurrently

- **Analog Inputs**
  - Supports RGB and YPbPr inputs, and built-in Line-Lock PLL. Support resolution up-to 720p/1080i
  - Supports RGB composite sync input(CSync), Hsync and VSync
  - Built-in Pre-amp, mid-level & ground clamp
  - Automatic Clamp Control for CVBS, Y and C
  - Programmable Static Gain Control or Automatic Gain Control for CVBS or Y/C
  - Max Input configuration up to 9xCVBS, 3xS-video, 3xYPbPr, 3xRGB
  - Phases Tracking and Boundary for adjusting input quality.
  - ADC built-in programmable low-pass filter for reducing input source noise

- **Digital Inputs**
  - CCIR656 and 601 8/16-bit support
  - TTL RGB565/666/888 support
  - Support RGB565 and CCIR656 inputs at the same time

- **Digital Video Processing**
  - 2D video de-interlacer
  - Vivid Color by 3D reproduction color management engine including skin tone adjustment
  - Adaptive contrast enhancement to deepen depth of view
  - 2D adaptive noise reduction
  - Brightness, contrast, saturation and hue adjustment
  - Digital Luminance Transient Improvement (DLTI)
  - Digital Chrominance Transient Improvement (DCTI)
  - Coef. Programmable YcbCr-to-RGB Color Space Converter
  - 3-channel gamma correction/adjustment
  - Black Level Extension(BLE) and White Level Extension(WLE)
  - Independent vertical and horizontal scaling
  - Supports horizontal non-linear scaling for 16:9/16:10 panels
  - Coefficient based sharpness filters
  - 2-D edge enhancement
  - Programmable standard & special panel burn-in test patterns
  - Support special border frame blocking mode
  - Horizontal Fish-eye correction (480i/p input)

- **Video Decoder**
  - TV standard supported: NTSC, PAL, NTSC 4.43, SECAM
  - TV standard auto-detection and configuration
  - Auto gain control enhancement
  - 2D adaptive comb filter

- **LCD interface**
  - Provides 3x256 Gamma correction for panel compensation
  - Supports image pan functions
  - Programmable Timing Controller
  - 24-bit TTL output, single/dual LVDS output, serial RGB output
  - CCIR656 encode
  - Integrated DC-DC power conversion controller for gate and source drivers
  - Output(LCD) resolution support up-to 1280x1024 and 1366x768
  - Support DDC/EDID

- **Built-in On Screen Display Engine**
  - Support 1/2/4/8 bits/pixel
  - 16K-word OSD2 memory
  - Supports text or bitmap modes
  - Supports character blinking and overlay functions
  - Fully programmable character mapping
  - Supports alpha blending & Zoom-in/Zoom-out function
  - Built-in 114+ fonts (12 x18, 16 x24 each)

- Pattern-Filled background
- Optional fonts stored in off-chip serial ROM
- Supports free run OSD mode

■ **SPI Flash Based On Screen Display Engine**
- Support bitmap background images on SPI NOR flash, and having various transition effects. Also support Terawins Bitmap Compression(TWBC) to save storage space
- Support Sprite layer for animation icon
- Standard RGBA 8888 index color palette with two lookup tables
- Full screen support up-to 1024x768

■ **Peripherals/Misc.**
– Direct interface to a (27.0MHz) Crystal, other frequencies are also applicable.
– Also provide a buffered clock output for external Micro-controller
– Digital PWM controller for DC-DC convert
- Supports 2-wire I^2C (Slave/Master)
- SPI NOR flash controller supports both MCU and OSD concurrently
- SPI NOR flash 4-bit read/write support
- Supports SAR*2
- 4-wire/5-wire touch panel controller
- Pulse Width Modulation(PWM) Outputs
- General Purpose Input/Output (GPIO)
- UART *2
- Built-in 8051 MCU with 4K bytes code cache
- Built-in command queue for issuing write command to internal registers

■ **Power Supply: +3.3V, Build in +1.8V LDO**

■ **Package: 128-pin LQFP**

1.2 General Description

The T123AI is a highly integrated All-in-one Visual Processor that provides major cost saving solution for the portable applications. T123AI has built-in high performance +1.8V LDO, Triple ADCs, TCON, 24-bits TTL, single/dual LVDS, serial RGB output, Scaling Machine with sophisticated upscaling and downscaling algorithms. The Innovative integrated "Frame-Buffer-Less" De-interlacer can significantly reduce system cost. The T123AI also integrates enhanced two layer OSD engines. The device can interface to an external micro-controller through 2-wire serial bus interface or use internal MCU (8051) with ROM code in external SPI Flash ROM.

1.3 Applications

1. Small to medium sized displayer, In-car TV
2. Video Door Phone
3. Multi-Function Monitor

1.4 System Architecture

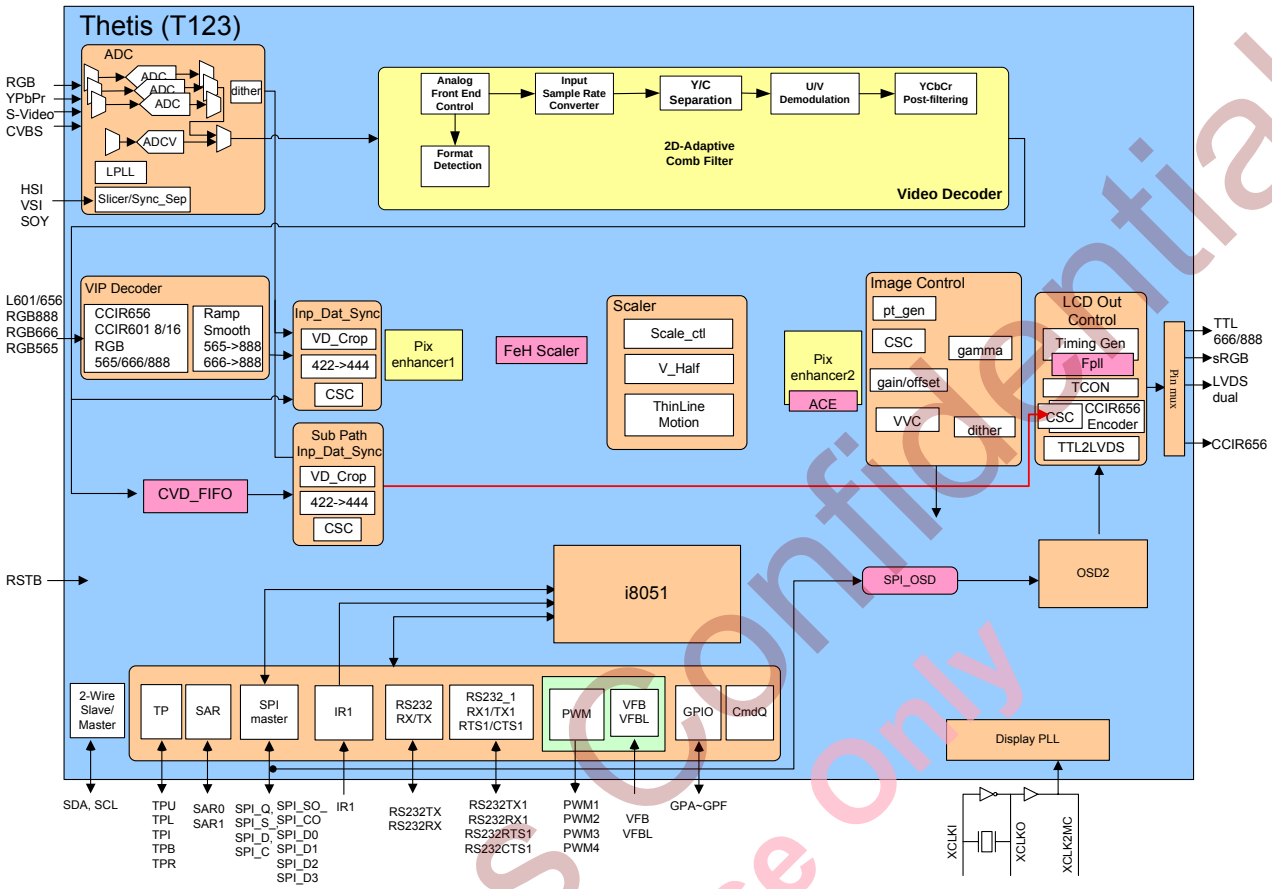


Figure 1-1 System Architecture

1.5 System Configurations

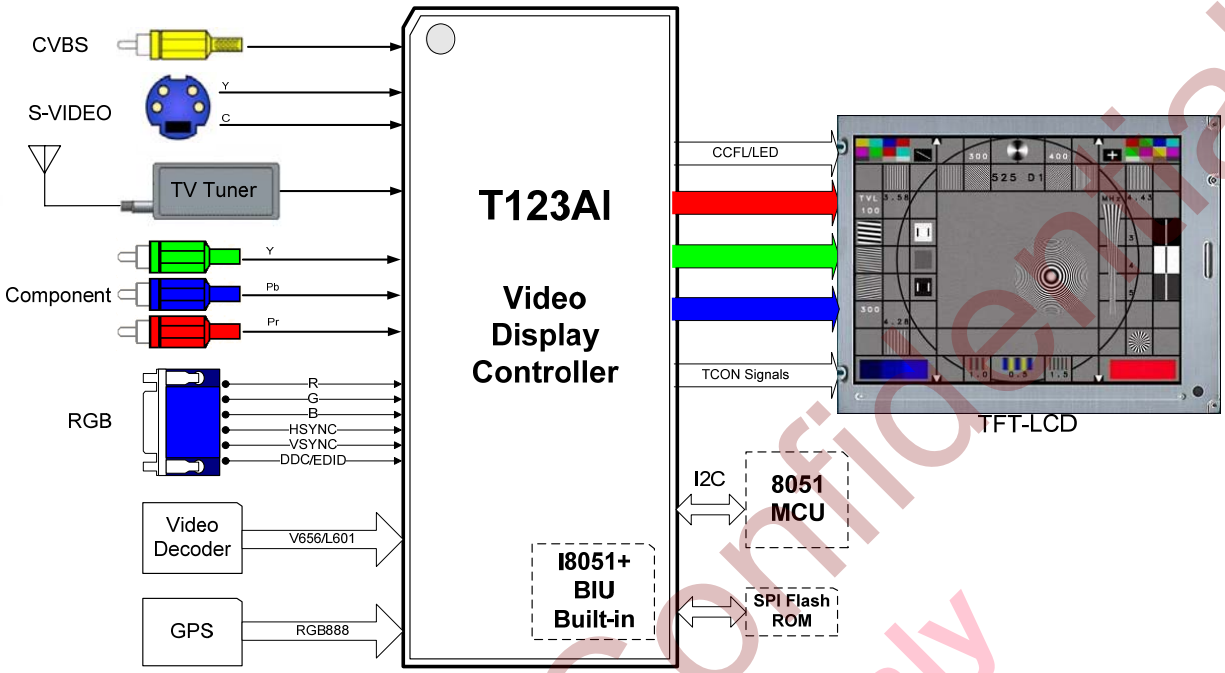


Figure 1-2 System Configurations

1.6 Pinout Diagram

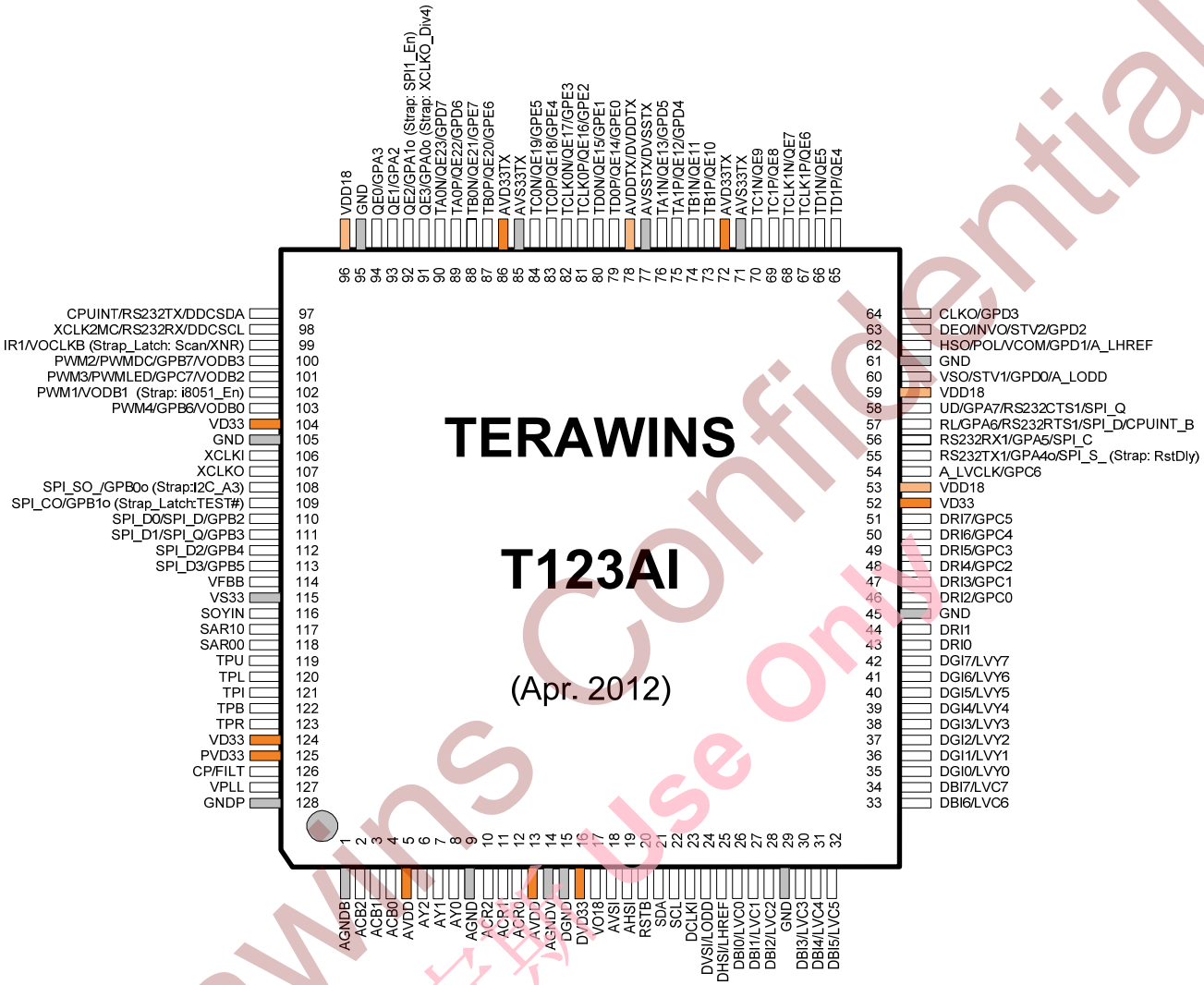


Figure 1-3 T123AI Pinout Diagram

1.7 Pin Description

Table 1-1 T123AI Pin Description

Symbol	Pin #	Type	Description
Power Supplies			
VDD18	53, 59, 96	PWR	+1.8V digital core power supply
VDD33	52, 104	PWR	+3.3V digital output power supply
GND	29,45, 61, 95,105	GND	digital core ground
AVDDB	5	PWR	+3.3V analog power supply for ADC1
AGNDB	1	GND	+3.3V analog ground for ADC1
AVDDG	5	PWR	+3.3V analog power supply for ADC3
AGNDG	9	GND	+3.3V analog ground for ADC3
AVDDR	13	PWR	+3.3V analog power supply for ADC2
AGNDR	9	GND	+3.3V analog ground for ADC2
AVDDV	13	PWR	+3.3V analog power supply for ADC4
AGNDV	14	GND	+3.3V analog ground for ADC4
DGND	15	GND	+3.3V digital ground for ADCs
BVDD33	124	PWR	+3.3V analog power supply for bias block
BVS33	115	GND	+3.3V analog ground for bias block
VD33PWM	124	PWR	+3.3V analog power supply for SARADC and PWM
VS33PWM	115	GND	+3.3V analog ground for SARADC and PWM
PVD33	125	PWR	+3.3V analog power supply for LPLL
GNDP	128	GND	+3.3V analog ground for LPLL
AVD33TX	72,86	PWR	+ 3.3V analog power supply for LVDSTX
AVS33TX	71,85	GND	+ 3.3V analog ground for LVDSTX
AVDDTX	78	PWR	+ 1.8V analog power supply for LVDSTX
AVSSTX	77	GND	+ 1.8V analog ground for LVDSTX
DVD33	16	PWR	+ 3.3V digital power supply for LDO and ADCs
Timing Controller Interface Signals			
VSO/STV1	60	DO	Vertical Synchronization Output Control Signal Gate driver start pulse1 share w/ VSO
HSO/POL/VCOM	62	DO	Horizontal Synchronization Output Control Signal
DEO/INVO/STV2	63	DO	Horizontal Output Data Enable Signal Gate driver start pulse2 share w/DEO
CLKO	64	DO	Output pixel clock
RL	57	DO	Horizontal Right/Left control
UD	58	DO	Vertical Up/Down control
Parallel Panel TTL Interface Signals – 24 bits			
DBO0~DBO7	74,73, 70~65	DO	TTL Blue channel output data
DGO0~DGO7	84~79, 76,75	DO	TTL Green channel output data
DRO0~DRO7	94~87	DO	TTL Red channel output data
Parallel Panel TTL Interface Signals – 18 bits			
DBO2~DBO7	70~65	DO	TTL Blue channel output data
DGO2~DGO7	80~79, 76~73	DO	TTL Green channel output data

Symbol	Pin #	Type	Description
DRO2~DRO7	88~87 84~81	DO	TTL Red channel output data
LVDS TX			
TD1P	65	AO	LVDSTX port1 DATA channel DP
TD1N	66	AO	LVDSTX port1 DATA channel DN
TCLK1P	67	AO	LVDSTX port1 CLOCK channel CLKP
TCLK1N	68	AO	LVDSTX port1 CLOCK channel CLKN
TC1P	69	AO	LVDSTX port1 DATA channel CP
TC1N	70	AO	LVDSTX port1 DATA channel CN
TB1P	73	AO	LVDSTX port1 DATA channel BP
TB1N	74	AO	LVDSTX port1 DATA channel BN
TA1P	75	AO	LVDSTX port1 DATA channel AP
TA1N	76	AO	LVDSTX port1 DATA channel AN
TD0P	79	AO	LVDSTX port0 DATA channel DP
TD0N	80	AO	LVDSTX port0 DATA channel DN
TCLK0P	81	AO	LVDSTX port0 CLOCK channel CLKP
TCLK0N	82	AO	LVDSTX port0 CLOCK channel CLKN
TC0P	83	AO	LVDSTX port0 DATA channel CP
TC0N	84	AO	LVDSTX port0 DATA channel CN
TB0P	87	AO	LVDSTX port0 DATA channel BP
TB0N	88	AO	LVDSTX port0 DATA channel BN
TA0P	89	AO	LVDSTX port0 DATA channel AP
TA0N	90	AO	LVDSTX port0 DATA channel AN
Serial Panel Interface Signals			
VSO	60	DO	Vertical Synchronization Output Control Signal
HSO	62	DO	Horizontal Synchronization Output Control Signal
DEO	63	DO	Horizontal Output Data Enable Signal
CLKO	64	DO	sPanel clock
sD0~sD7	74,73, 70~65	DO	sPanel data
ITU 656 Output Interface Signals			
VOCLK	64	DO	Video clock output
VOD0~7	74,73, 70~65	DO	Video output 8-bit data port
SPI 1-bit/4-bit Interface			
SPI_SO_	108	DO	Chip Select
SPI_CO	109	DO	Data clock output
SPI_D0~3	110~113	DI/DO	SPI OSD data port
LDO			
VO18	17	AO	1.8V output voltage of LDO
LPLL			
CP	126	AO	connect to external LPLL loop filter
FILT	126	AO	connect to external LPLL loop filter
VPLL	127	AO	Connect to external 100uF//0.1uF capacitor
Slicer Interface			
SOYIN	116	AI	Sync-on-Luminance Y or Sync-on-Green input

Symbol	Pin #	Type	Description
Configuration Interface Signals			
RSTB	20	DI	Whole chip reset
SDA	21	DIO	2-wire serial bus data. Power down does not affect SDA
SCL	22	DIO	2-wire serial bus clock. Power down does not affect SCL. This pin should be high when RSTB asserted for avoid entering Scan test mode
XCLK2MC	98	DO	Buffered XCLKI for external microprocessor
CPUINT	97	DO	Internal Interrupt
ADC/Analog input Interface			
ACB2	2	AI	ADC1 analog positive input 2
ACB1	3	AI	ADC1 analog positive input 1
ACB0	4	AI	ADC1 analog positive input 0
ACR2	10	AI	ADC2 analog positive input 2
ACR1	11	AI	ADC2 analog positive input 1
ACR0	12	AI	ADC2 analog positive input 0
ACY2	6	AI	ADC3 analog positive input 2
ACY1	7	AI	ADC3 analog positive input 1
ACY0	8	AI	ADC3 analog positive input 0
AVSI	18	DI	RGB Vertical Synchronous input
AHSI	19	DI	RGB Horizontal Synchronous input
Video-In Interface: ITU-656			
LVC0~7	26~28, 30~34	DI	Video data port of the ITU-656 input port
LVCLK	23	DI	Video clock of the ITU-656 (2x pixel rate)
Video-In Interface: Alternative ITU-656			
A_LVC0~7	43~44, 46~51	DI	Video data port of the ITU-656 input port
A_LVCLK	54	DI	Video clock of the ITU-656 (2x pixel rate)
Video-In Interface: L601_8bits			
LVC0~7	26~28, 30~34	DI	Video data port of 8-bit 601 or Chroma
LVCLK	23	DI	Video clock (2x pixel rate)
LODD	24	DI	ITU-601 Odd or VSync input
LHREF	25	DI	ITU-601 HREF(HDE) or Hsync input
Video-In Interface: Alternative L601_8bits			
LVC0~7	43~44, 46~51	DI	Video data port of 8-bit 601 or Chroma
LVCLK	54	DI	Video clock (2x pixel rate)
LODD	60	DI	ITU-601 Odd or Vsync input
LHREF	62	DI	ITU-601 HREF(HDE) or Hsync input
Video-In Interface: L601_16bits			
LVC0~7	26~28, 30~34	DI	Video chroma data port of 16-bit 601
LVY0~7	35~42	DI	Video Luma data port of 16-bit 601
LVCLK	23	DI	Video clock of the ITU-656 (2x pixel rate)
LODD	24	DI	ITU-601 Odd or Vsync input
LHREF	25	DI	ITU-601 HREF(HDE) or Hsync input

Symbol	Pin #	Type	Description
Video-In Interface: RGB565 Input			
DRI3~DRI7	38~42	DI	Digital RGB input: 5 bits of Color R
DGI2~DGI7	32~37	DI	Digital RGB input: 6 bits of Color G
DBI3~DBI7	26~28 30~31	DI	Digital RGB input: 5 bits of Color B
DCLKI	23	DI	Video clock (1x pixel rate)
DVSI	24	DI	Digital RGB Vsync input
DHSI	25	DI	Digital RGB Hsync input
Video-In Interface: RGB666 Input			
DRI2~DRI7	39~44	DI	Digital RGB input: 6 bits of Color R
DGI2~DGI7	33~38	DI	Digital RGB input: 6 bits of Color G
DBI2~DBI7	26~28, 30~32	DI	Digital RGB input: 6 bits of Color B
DCLKI	23	DI	Video clock (1x pixel rate)
DVSI	24	DI	Digital RGB Vsync input
DHSI	25	DI	Digital RGB Hsync input
Video-In Interface: RGB888 Input			
DRI0~DRI7	43~44, 46~51	DI	Digital RGB input: 8 bits of Color R
DGI0~DGI7	35~42	DI	Digital RGB input: 8 bits of Color G
DBI0~DBI7	26~28, 30~34	DI	Digital RGB input: 8 bits of Color B
DCLKI	23	DI	Video clock (1x pixel rate)
DVSI	24	DI	Digital RGB Vsync input
DHSI	25	DI	Digital RGB Hsync input
PLL Reference Clock			
XCLKI	106	DI	Output PLL reference clock input
XCLKO	107	DO	Output PLL reference clock output
Power Management Interface Signals			
VFB	114	AI	Feedback of DC-to-DC voltage
Peripheral			
SAR00	118	AI	12B SARADC0 input channel 0
SAR10	117	AI	8B SARADC1 input channel 0
TPU	119	AI	Touch panel analog input TPU
TPL	120	AI	Touch panel analog input TPL
TPI	121	AI	Touch panel analog input TPI
TPB	122	AI	Touch panel analog input TPB
TPR	123	AI	Touch panel analog input TPR
PWM1	102	DO	Pulse Width Modulation 1 for backlight control / Volume / …
PWM2	100	DO	PWM output
PWM3	101	DO	PWM output
PWM4	103	DO	Pulse Width Modulation 4 for backlight control / Volume / …
IR1	99	DI	IR input
RS232TX	97	DO	RS232 Transmitting signal
RS232RX	98	DI	RS232 Receiving signal
RS232TX1	55	DO	RS232_1 Transmitting signal
RS232RX1	56	DI	RS232_1 Receiving signal
RS232RTS1	57	DO	RS232_1 request to set

Symbol	Pin #	Type	Description
RS232CTS1	58	DI	RS232_1 clear to set
DDCSDA	97	DI/DO	2-wire serial bus data for DDC
DDCSCL	98	DI	2-wire serial bus clock for DDC
GPA~GPF	Refer to Section 1.8	DI/DO	General purpose digital input/output
Hardware Trapping			
RstDly	55	DI	0 : use external signal to reset 1 : use internal timer signal to reset
XCLKO_Div4	91	DI	1 : use the clock frequency divide by 4 or 2 internally 0 : use the clock frequency the same as input internally
SPI1_En	92	DI	1 : Enable specific SPI 1bit flash for i8051
Scan/XNR	99	DI	When chip enter test mode, 0 : test mode is XNOR test 1 : test mode is scan test
I8051_En	102	DI	0 : disable on-chip 8051 1 : enable on-chip 8051
I2C_A3	108	DI	I2C device ID bit3
TEST#/ Scan_Shift	109	DI	When reset is asserted, 0 : test mode 1 : normal mode When reset is de-asserted, and chip is under scan test, it is used for the shift enable signal of scan chain

1.8 GPIO Pin Configuration

1.8.1 GPC

In-Video Type	CCIR656	CCIR601-8	CCIR601-16	TTL565	TTL666	TTL888	TTL565+ CCIR656
GPC0	46	46	46	46	46	N/A	N/A
GPC1	47	47	47	47	47	N/A	N/A
GPC2	48	48	48	48	48	N/A	N/A
GPC3	49	49	49	49	49	N/A	N/A
GPC4	50	50	50	50	50	N/A	N/A
GPC5	51	51	51	51	51	N/A	N/A
GPC6	54	54	54	54	54	54	N/A
Total Available#	7	7	7	7	7	1	0

	PWM3 En	No PWM3
GPC7	N/A	101
Total Available#	0	1

1.8.2 GPA4~7

Case 1: full GPA4~GPA7 available, no UART1 w/AFC, no SPI1_En, no RL/UD
Case 2: UART1 w/o AFC, no RL/UD, no SPI1_En

	Case1	Case2	SPI1_En
GPA4	55	N/A	N/A
GPA5	56	N/A	N/A
GPA6o	57	57	N/A
GPA7	58	58	N/A
Total Available#	4	2	0

1.8.3 GPA0~3, GPD, GPE

Output Panel Type	TTL666	TTL888	sRGB	CCIR656	LVDS Single	LVDS Dual
GPE0	N/A	N/A	79	79	79	N/A
GPE1	N/A	N/A	80	80	80	N/A
GPE2	N/A	N/A	81	81	81	N/A
GPE3	N/A	N/A	82	82	82	N/A
GPE4	N/A	N/A	83	83	83	N/A
GPE5	N/A	N/A	84	84	84	N/A
GPE6	N/A	N/A	87	87	87	N/A
GPE7	N/A	N/A	88	88	88	N/A
GPD0	N/A	N/A	N/A	60	60	60
GPD1	N/A	N/A	N/A	62	62	62
GPD2	N/A	N/A	N/A	63	63	63
GPD3	N/A	N/A	N/A	N/A	64	64
GPD4	N/A	N/A	75	75	N/A	N/A
GPD5	N/A	N/A	76	76	N/A	N/A
GPD6	89	N/A	89	89	89	N/A
GPD7	90	N/A	90	90	90	N/A
GPA0	91	N/A	91	91	91	91
GPA1	92	N/A	92	92	92	92
GPA2	93	N/A	93	93	93	93
GPA3	94	N/A	94	94	94	94
Total Available#	6	0	16	19	18	8

1.8.4 GPB

	SPI 4-bit	SPI 1-bit
GPB0	N/A	N/A
GPB1	N/A	N/A
GPB2	N/A	N/A
GPB3	N/A	N/A
GPB4	N/A	112
GPB5	N/A	113
Total Available#	0	2

	No	No	No

	PWM2	PWM4	PWM2/PWM4
GPB6 GPB7	100 N/A	N/A 103	100 103
Total Available#	1	1	2

2 Theory of Operations

2.1 I²C Command Protocol

Before your tester writes I²C commands to T123AI, slave address must be set at 50h. The timing sequence can be shown as below. After 4 cycles, the tester can get started IIC commands. SPI_SO_(A4) can affect slave address. Set it low for 40h, and high for 60h.

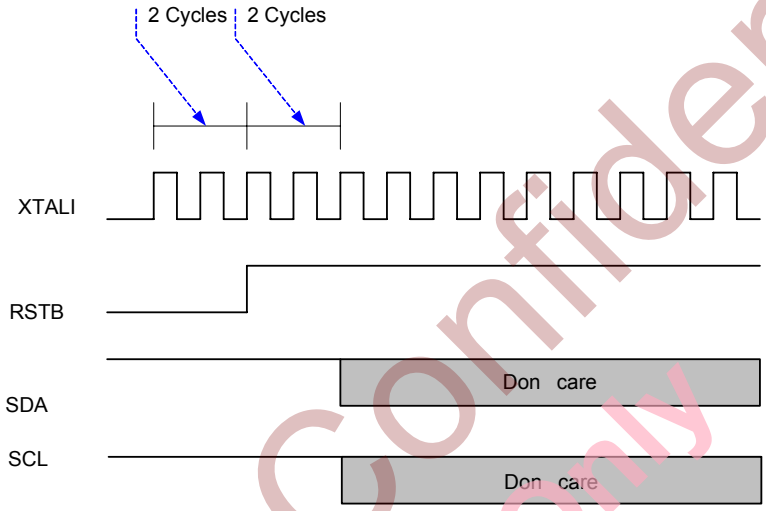


Figure 2-1 Power-Up Initialization

When tester issues commands to the T123AI, the only way the user can program the T123AI is using the 2-wire serial bus protocol. This section describes the 2-wire serial bus protocol. Data transfers on the 2-wire serial bus are initiated with a START condition and are terminated with a STOP condition. Normal data on the SDA line must be stable during the high period of the SCL. The transition on the SDA is only allowed while SCL is low. The START condition is unique case and is defined by a high-to-low transition on the SDA while the SCL is high. The STOP condition is a unique case and is defined by a low-to-high transition on the SDA while the SCL is high. Each data packet on the 2-wire serial bus consists of 8 bits of data followed by an ACK bit. Data is transferred with MSB first. The transmitter releases the SDA line during the ACK bit and the receiver of data transfer must drive the SDA line low during the ACK bit to acknowledge receipt of the data. The frequency of SCL can be from 50 KHz up to 500KHz.

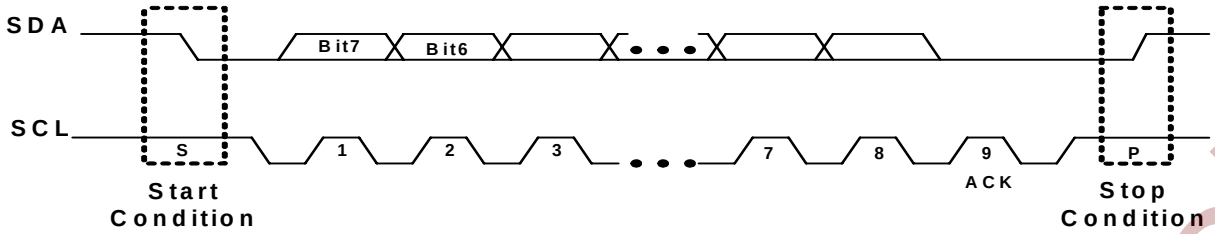


Figure 2-2 Basic I²C Bus Protocol

The timing below shows a typical T123AI I²C single byte write command,

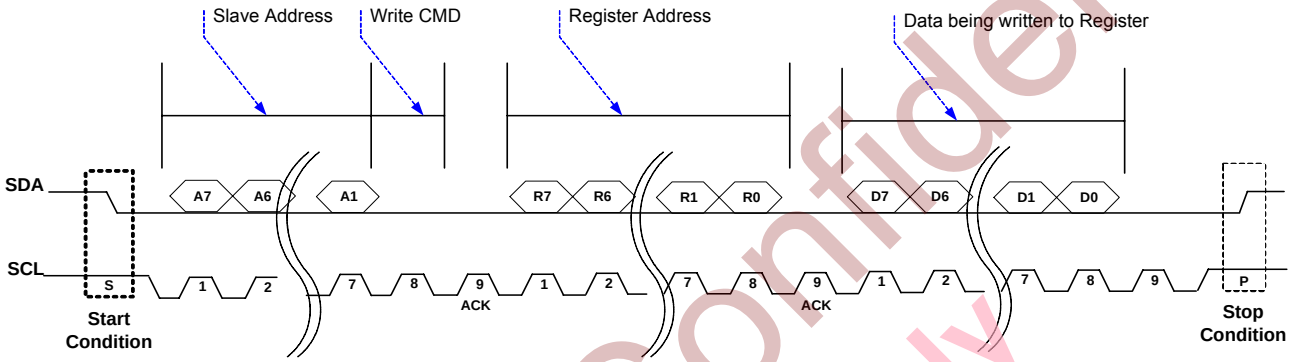


Figure 2-3 T123AI I²C Single Byte Write Command

The timing below shows a typical T123AI I²C single byte read command,

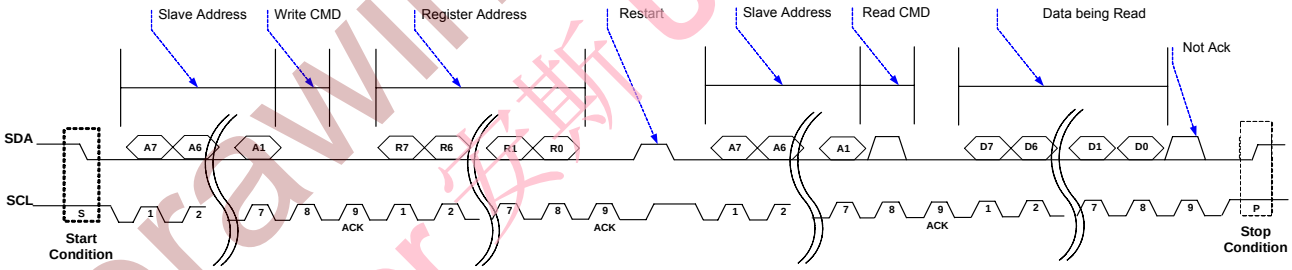


Figure 2-4 T123AI I²C Single Byte Write Command

2.2 Analog Front End

T123AI contains 4 ADCs in Analog Front End. Each channel of ADCs can digitalize SDTV/HDTV signals from analog to digital. The figure shown below can describe how to select a SDTV/HDTV signal from 4 inputs prior to ADC.

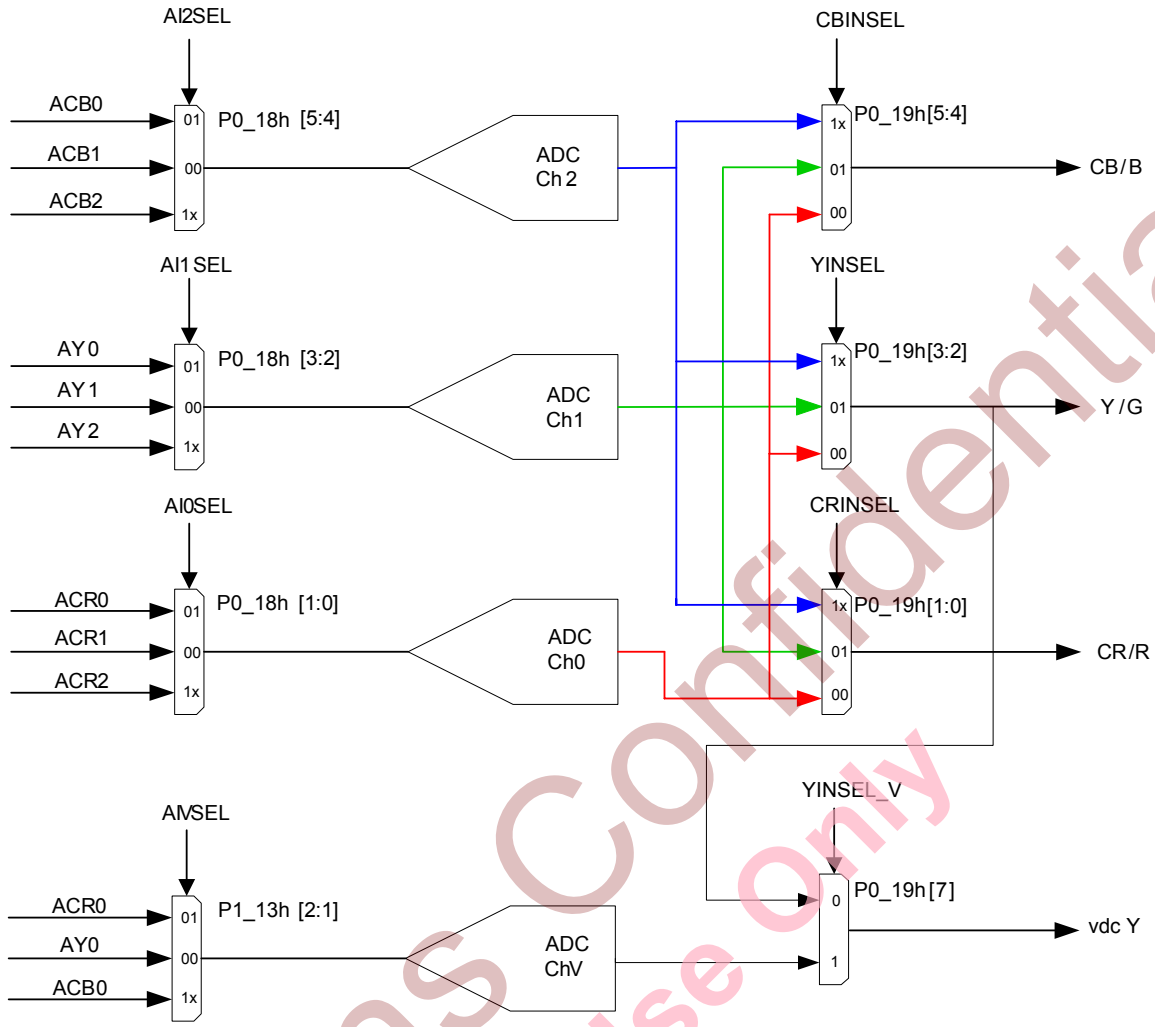


Figure 2-5 Analog Front End MUX

2.3 Y/C Separation and Chroma Decoder

A composite video has luma(Y) and chromal information mixed in the same video signal. This video signal can also be represented by the equation below,

$$CVBS = Y + U * Sin(wt) + V * \cos(wt)$$

Where $w = 2\pi f_{SC}$, f_{SC} =3.58Mhz if NTSC, f_{SC} =4.43Mhz if PAL

The figure below shows a typical composite signal. The 2-D adaptive comb filter inside T123AI is designed to separate Y and C from a composite video signal.

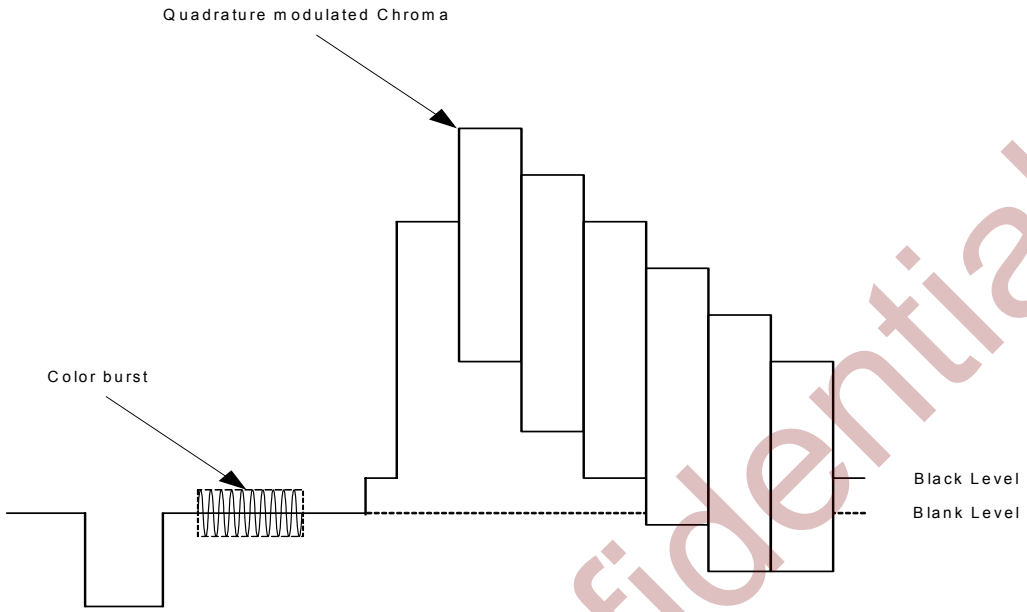


Figure 2-6 CVBS Input

. The conventional 3-line comb filter fails to separate Y and C if there is a vertical transition. The 2-D adaptive comb filter is based on equally weighting factors that color changes along vertical and horizontal edges. Let the amount of color change along vertical and horizontal direction DCv and DCh, the weighting factor can be expressed as following equations,

$$Wh = \frac{DCv}{DCv + DCh}$$

$$Wv = \frac{DCh}{DCv + DCh}$$

By employing adaptive method, chroma can be recovered by following equation,

$$C = Ch * Wh + Cv * Wv$$

After Y/C separation, Y and C should look like waveforms shown as in following figure. Y only contains low frequency part, while C contains high frequency part that is centered around sub-carrier f_{SC}.

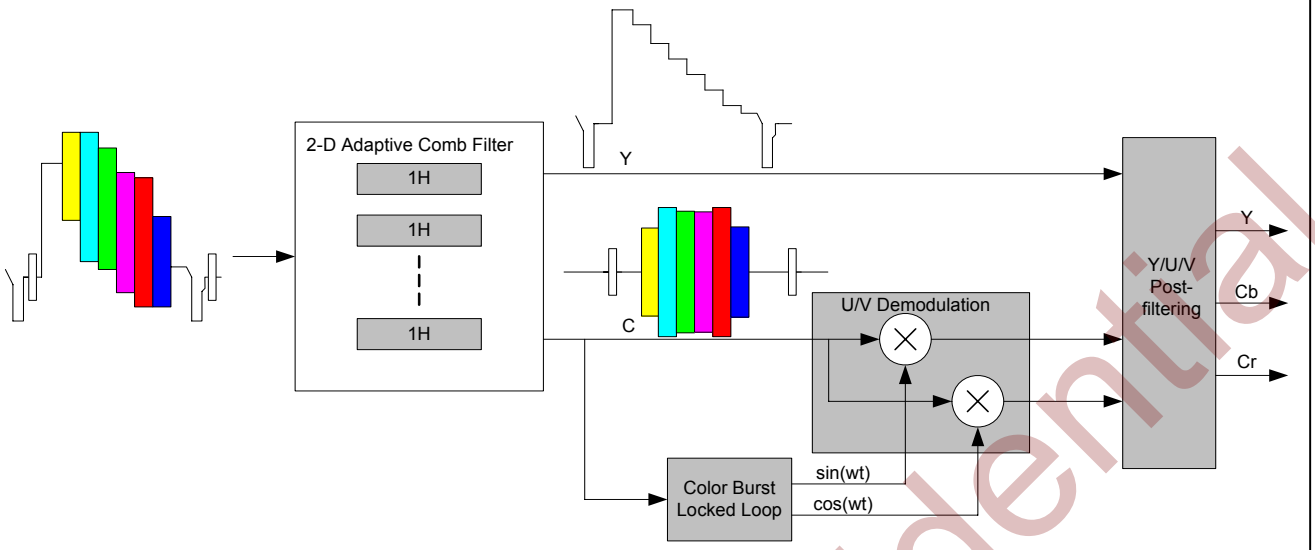


Figure 2-7 Separate Y/Cb/Cr

2.4 Digital Color Transient Improvement (DCTI)

Usually, a composite or S-video SDTV signal may have bandwidth limitation that causes the loss chroma detail around two different color bars. Two pictures shown below illustrate the result before and after DCTI block. Without DCTI(the upper picture), we may see color transient wider than several pixels. A slow transient edge usually blurs image. T123AI DCTI algorithm can sharpen those color transient edges. The lower picture shows that chroma data is enhanced by increasing the slope of edge transient without introducing the ring effects.

Figure 2-8 DCTI

2.5 Black/White-Level Extension (BLE&WLE)

Black Level Expansion (BLE) and White Level Extension (WLE) can enhance image contrast that makes dark regions of image darker, and/or bright regions brighter. The figure shown below is BLE&WLE transfer function.

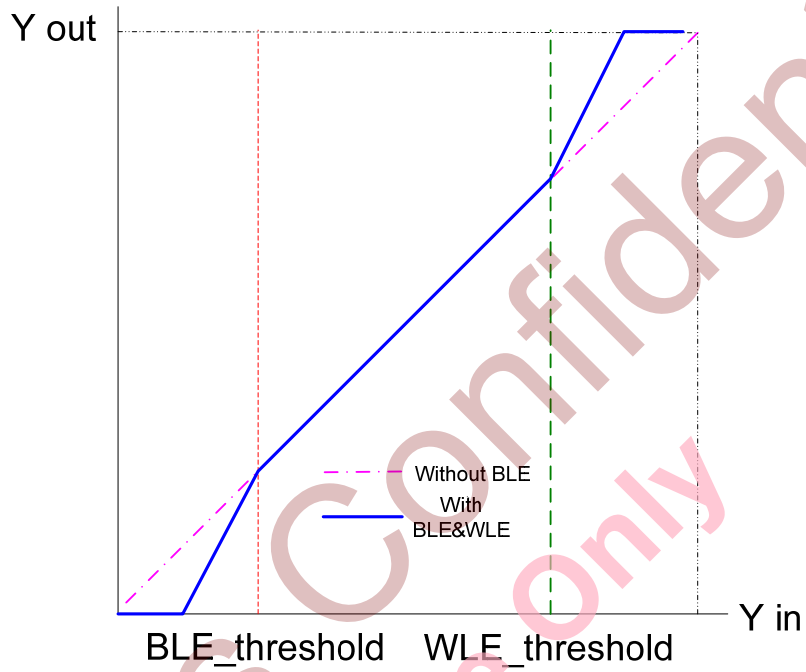


Figure 2-9 Black Level and White Level Extension

$$Yout = Yin - (BLE\_Yoffset - Yin) * BLE\_Gain / 16, \text{ while } Yin < BLE\_Threshold$$
$$Yout = Yin + (Yin - WLE\_Yoffset) * WLE\_Gain / 16, \text{ while } Yin > BLE\_Threshold$$

Where $BLE\_Yoffset$ and BLE_Gain could be programmed by register P0_6Fh; $WLE\_Yoffset$ and WLE_Gain could be programmed by register P0_6Fh and P0_64h respectively.

2.6 Color Space Converter

A pixel in YCbCr color space can be converted to RGB color space by using following equations,

$$R = YCoef\_R * (Y - 16) + /- CbCoef\_R * (Cb - 128) + CrCoef\_R * (Cr - 128)$$
$$G = YCoef\_G * (Y - 16) - CbCoef\_G * (Cb - 128) - CrCoef\_G * (Cr - 128)$$
$$B = YCoef\_B * (Y - 16) + CbCoef\_B * (Cb - 128) + /- CrCoef\_B * (Cr - 128)$$

The equations shown as below correspond to a typical YCbCr-to-RGB converter.

2.7 FIR Scalar

FIR Scaler can scale input H/V sizes to fit any LCD panel resolution. The flexible and independent H/V scalers allow users to program display area in 16:9 Full mode, 16:9 non-linear wide mode and 4:3 mode. FIR scaler also provides coefficient-based 2-D sharpness that can sharpen detail of picture.

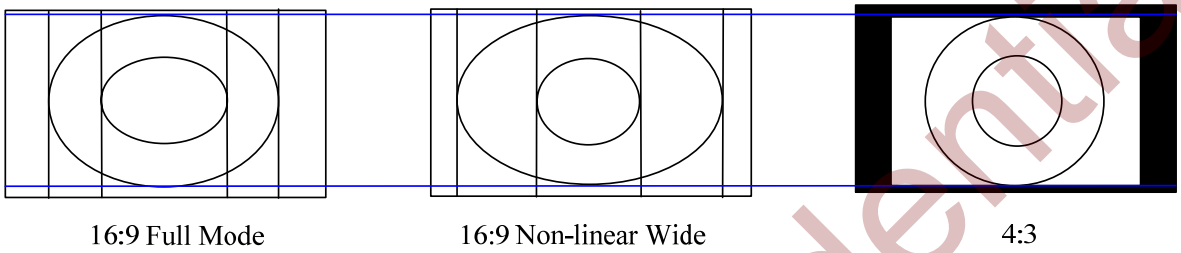


Figure 2-10 Aspect Ratio Adjusting

2.8 Gamma Correction

The relation between input video signal and LCD panel may exist non-linear transfer function such as figure shown below,

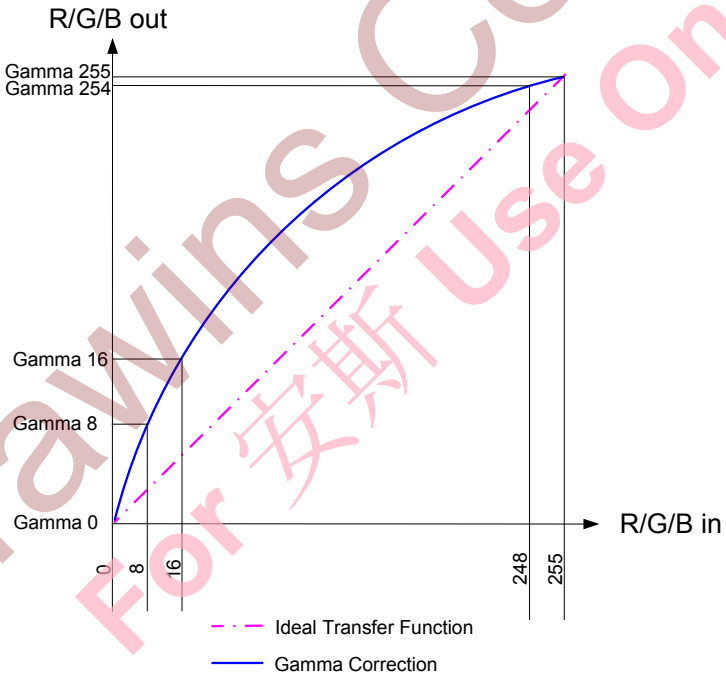


Figure 2-11 Gamma LUT

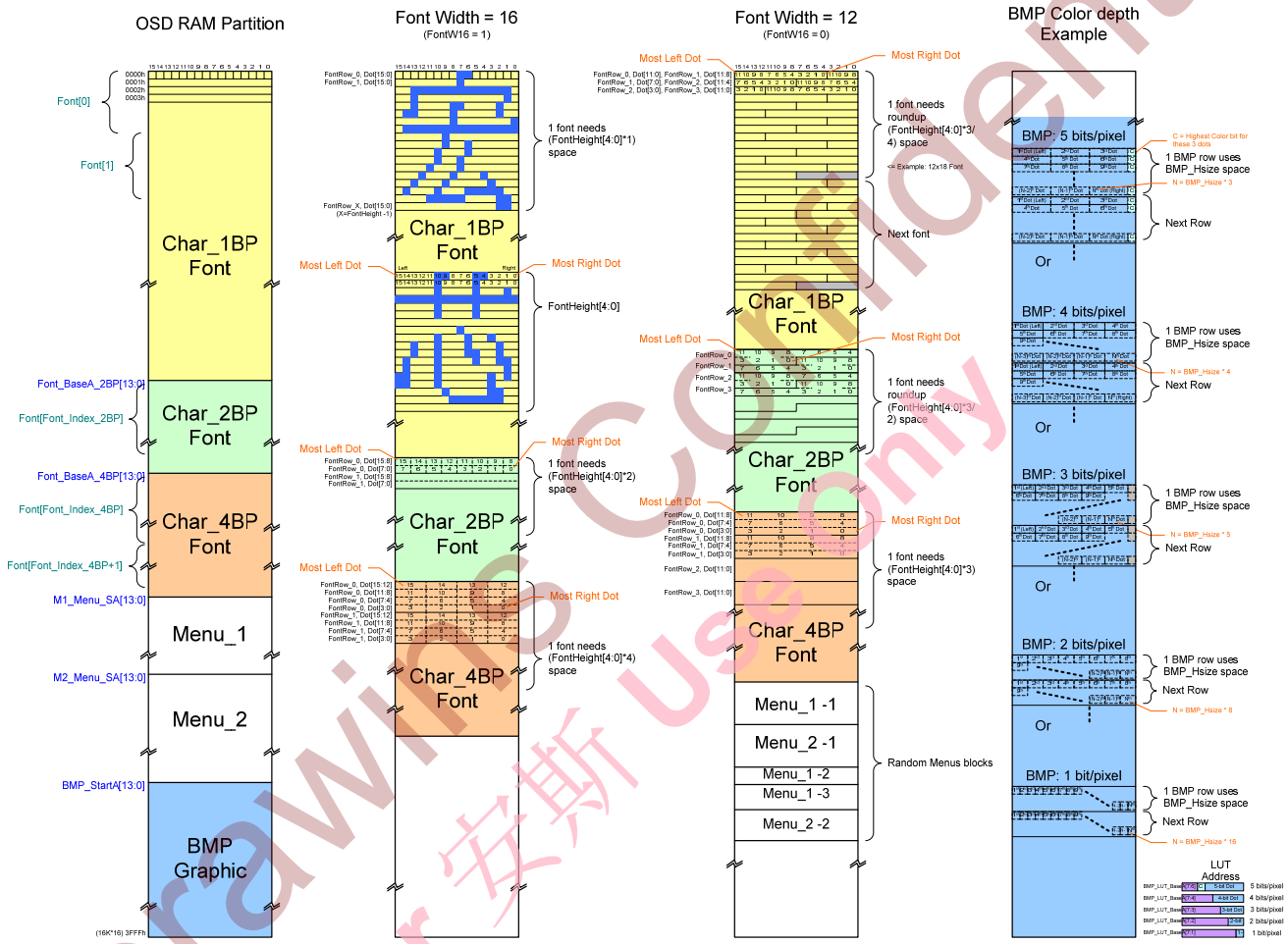
T123AI uses 256-entries for point-to-point gamma LUTs. Each point can be programmed via register at P0_93h and P0_94h.

2.9 OSD2

The OSD2 in T123AI is improved in rendering and efficient memory usage. The legacy OSD is either one thread Menu or one graphic (BMP) mode. T123AI OSD2 supports two threads menus and one graphic rendering simultaneously. So it will be easier to have menu control and Closed Caption.

2.9.1 OSD2 RAM Partition

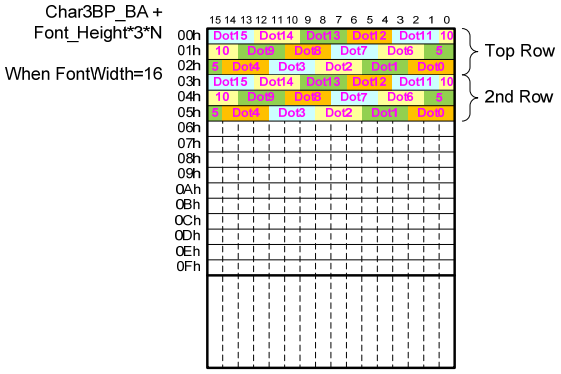
The OSD2 Font/Menus/BMP memory share the same built-in 16Kx16 SRAM.



2.9.2 OSD2 Char3BP (Tw SubFont) Fonts in ORAM/ROM

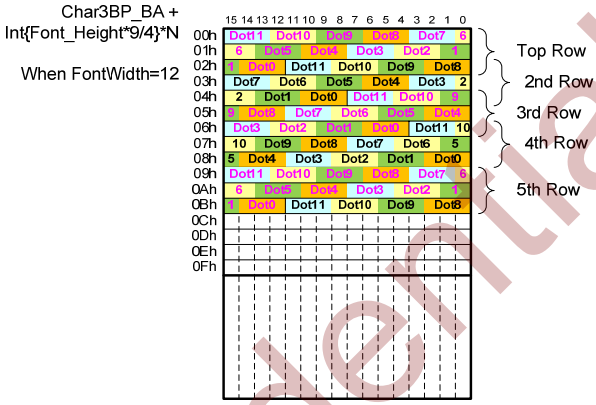
ORAM

(Char3BP Font portion)



ORAM

(Char3BP Font portion)



2.9.3 OSD2 Register Map

I/O Port	Groups	Index	Description
A8h – OSD2_Index A9h – OSD2_Data	Global Setting	00h	OSD2 Enable/Blinking Register
		01h	Font Size
		02h	Char2BP Font Index Base
		03h	Char4BP Font Index Base
		04h	Char2BP Font Memory Base Address, LSB
		05h	Char2BP Font Memory Base Address, MSB
		06h	Char4BP Font Memory Base Address, LSB
		07h	Char4BP Font Memory Base Address, MSB
		08h	OSD2 Color LUT Address port
		09h	OSD2 Color LUT Data Port
		0Ah	OSD2 Window Shadow
		0Bh	Global Alpha Blending Control
		0Ch	Char1BP color high bits offset
		0Dh	ROM Font Index Base
		0Fh	Revision ID
	Menu-1 Setting	10h	Menu-1 Enable
		11h	Menu-1 Start Address, LSB
		12h	Menu-1 Start Address, MSB
		13h	Menu-1 End Address, LSB
		14h	Menu-1 End Address, MSB
	ROM Font	16h	ROM Font Memory Base Address, LSB
		17h	ROM Font Memory Base Address, MSB
	Menu-2 Setting	18h	Menu-2 Enable
		19h	Menu-2 Start Address, LSB
		1Ah	Menu-2 Start Address, MSB

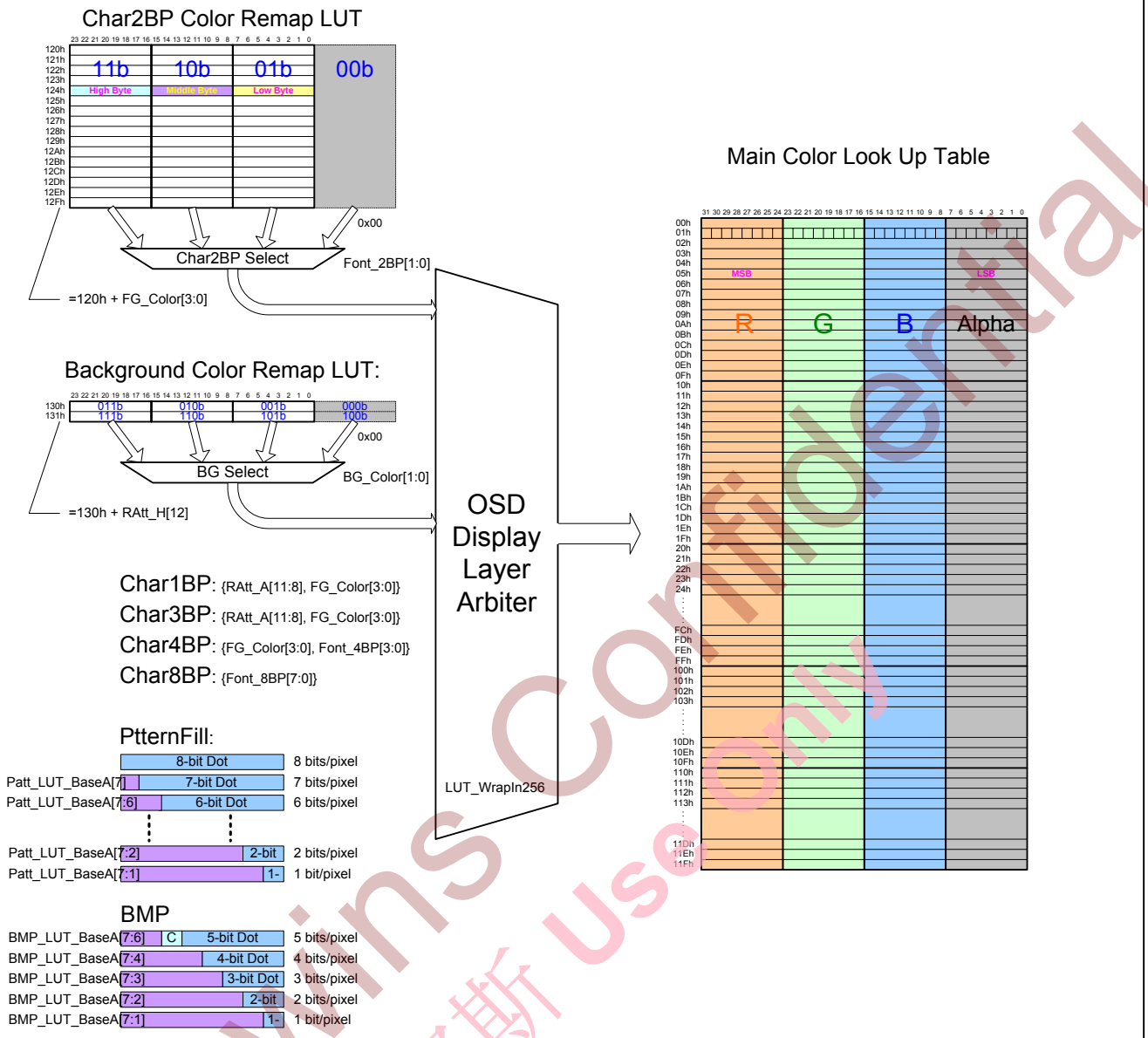
I/O Port	Groups	Index	Description
		1Bh	Menu-2 End Address, LSB
		1Ch	Menu-2 End Address, MSB
		1Fh	BIST results
	BMP Setting	20h	BMP Control Register
		21h	BMP Start Address, LSB
		22h	BMP Start Address, MSB
		23h	BMP Alpha Blending Control
		24h	BMP Horizontal Size, LSB
		25h	BMP Horizontal Size, MSB
		26h	BMP Vertical Size, LSB
		27h	BMP Vertical Size, MSB
		28h	BMP Position, Horizontal Start, LSB
		29h	BMP Position, Horizontal Start, MSB
		2Ah	BMP Position, Vertical Start, LSB
		2Bh	BMP Position, Vertical Start, MSB
		2Ch	BMP LUT Base Address
		2Dh	BMP Background Color

I/O Port	Groups	Index	Description
A8h – OSD2_Index A9h – OSD2_Data	Pattern Fill	30h	Patt Control Register
		31h	Patt LUT Base Address
		32h	Patt Horizontal Size
		33h	Patt Vertical Size
		34h	Patt Row Shift
		35h	Patt Alpha Blending Control
		36h	OSD2 BIST result and Patt Enlarge
		37h	Patt RAM Write Data Port
		38h	Patt Horizontal Start, LSB
		39h	Patt Horizontal Start, MSB
		3Ah	Patt Vertical Start, LSB
		3Bh	Patt Vertical Start, MSB
		3Ch	Patt Horizontal End, LSB
		3Dh	Patt Horizontal End, MSB
		3Eh	Patt Vertical End, LSB
		3Fh	Patt Vertical End, MSB
	Block Write	40h	Block Write Data LSB
		41h	Block Write Data MSB
		42h	Block Write Starting Address LSB
		43h	Block Write Starting Address MSB
		44h	Block Write Count
		45h	Block Write Control
	TrigRd	48h	ORAM Trigger Read Control
	SRAM	4Fh	Misc. ORAM Control

I/O Port	Groups	Index	Description
	Char 8BP	50h	Char8BP Font Index Base
		51h	Char8BP Font SRAM Base Address, LSB
		52h	Char8BP Font SRAM Base Address, MSB
	Sub Font	54h	Char3BP Control
		55h	Char3BP Sharpness
		56h	Char3BP Font SRAM Base Address, LSB
		57h	Char3BP Font SRAM Base Address, MSB
		58h	Char3BP Font ROM Base Address, LSB
		59h	Char3BP Font ROM Base Address, MSB
AAh – ORAM_A			OSD2 RAM Address Port of Starting Access (LSB A[7:0] first, then MSB A[13:8]).
ABh – ORAM_D			OSD2 RAM Data Port (Low Byte first, then High Byte). After two Writes, the address will be increased by 1.

2.9.4 OSD2 Color Scheme

For drawing a graphic menu, a colorful icon or logo, …., T123AI OSD2 provides 1BPP (one bit per pixel) ~ 5BPP (5 bits per pixel) BMP coding. For n-BPP BMP, it has one background color and (2^n – 1) foreground colors.
For character menus with pre-defined fonts, T123AI OSD2 provides mono characters (Char1BP, Char3BP -- SubFont) and color characters (Char2BP, Char4BP, Char8BP), randomly mix-able. So that, simple icon can be implemented by color characters. The color mapping of character/menu is more complicate, please refer to the following drawing.
The OSD2 main Color LUT is 256 + 32 entries SRAM, color in RGBA8888 format. Char8BP color is limited the lower 256 entries.



2.9.5 Character RAM Format

T123AI OSD2 character decoding supports 512 fonts. By setting FontROM, Char2BP, Char4BP and Char8BP Font Index Base, we could assign different percentage for those character fonts, depends on application, menu color requirement, memory size, fonts replacing, ... Note: the Char3BP, as Terawins propriety Sub-Font rendering, behaves similar to Char1BP.

The character “MENU” in T123AI OSD2 is combined with 1~n character “ROW”s, each ROW can have its own rendering behavior, such as alpha blending, position, zooming ratio, color groups, border/shadow modes, row length,…, these are defined as ROW Attributes (RAtt, current version supports 8 types). Or, few rows can share the same setting without redefining those RAtt.

2.9.5.1 Character Format

Each character is 16-bits length, includes foreground/background color, blinking, font index.

Bit	Symbol	Description

[15:14]	BG_Color[1:0]	Background Color, which combined with the RAtt_C<10> to become 3 bit, selects 6 background remap colors. If both 0, then transparent background.
[13]	Blink	Enable this Character display with blinking feature.
[12:9]	FG_Color[3:0]	Foreground (FG) Color, depends font index is Char1BP, Char2BP or Char4BP: 1. When Char1BP, these 4 bits as FG LSB 4 bits, combine with RAtt_A<11:8> (as FG MSB 4 bits), total 8 bits for selecting color LUT as character FG color. If the value is set as 0000b, then there will be no foreground, i.e. transparent. (Char1BP only) 2. When Char2BP, these 4 bits select one of 16 Char2BP remap LUT. Each Char2BP remap LUT entry is 3*8 bits for 2BP font pixel value: 01b, 10b and 11b. For 2BP font pixel value = 00b, then it will render as transparent. 3. When Char4BP, these 4 bits as FG MSB, then combine with 4BP font pixel 4 bits value to become 8 bits for addressing LUT. For 4BP font pixel value = 0000b, then it will render as transparent.
[8:0]	Char_Index[8:0]	Character Address (Index), selects the character font (i.e., 0,1,2,.. A,B,C, a,b,c,$,%,…). If the value is number N, then it selects the N^{th} font, and that font starting address is (N x Font_Height). The Font_Height is defined in OSD2_01h<4:0>.

2.9.5.2 Row Attribute Alpha-Blending Type Format (RAtt_A)

Bit	Symbol	Description
[15:12]	RAtt_ID = 1101b	Must set value 1101b for RAtt_A
[11:8]	FGC_1BP[7:4]	Defines the MSB 4 bits for Char1BP FG color for current row or below in same thread menu.
[7:6]	Reserved	
[5:4]	FG_aB_Mode[1:0]	Defines the FG alpha-Blending mode (see OSD2 configuration register OSD2_0B for detail) for current row or below in same thread menu.
[3:0]	aB_Source_Percentage[3:0]	Defines the alpha-Blending ratio (of source video/graphic) for current row or below in same thread menu.

2.9.5.3 Row Attribute Character Type Format (RAtt_C)

This RAtt_C is a must-have attribute for each menu row, and those content in OSD2 memory followed will be rendering as characters, not other row attributes except exceeding the row length (see Row_Length[5:0] below).

Bit	Symbol	Description
[15:13]	RAtt_ID = 000b	Must set value 000b for RAtt_C
[12]	Skip_This	When set to 1, the following one character row of current thread menu could be skipped, and continues the next row instead.
[11]	End_After	When set to 1, the following all character rows of current thread menu will be skipped.
[10:9]	CharHeight_Scale[1:0]	Defines the enlarge ratio (x1, x2, x3, x4) of the character height of the menu rows following and after.
[8:7]	CharWidth_Scale[1:0]	Defines the enlarge ratio (x1, x2, x3, x4) of the character width of the menu rows following and after.
[6:0]	Row_Length[6:0]	Indicates the following character row length (how many characters), valid value range is 1 to 127.

2.9.5.4 Row Attribute Dummy Type Format (RAtt_D)

This RAtt_D is a dummy attribute, it is used for replacing other non-RAtt_C type attributes when changing rendering behavior if need, also it is used when switch between rows with different BDS behavior, 4 lines will be inserted.

Bit	Symbol	Description

[15:0]	RAtt_ID = E001h	Must set value E001h for RAtt_D

2.9.5.5 Row Attribute Gap Type Format (RAtt_G)

This RAtt_G is used to insert fix vertical null lines between menu rows.

Bit	Symbol	Description
[15:13]	RAtt_ID = 001b	Must set value 001b for RAtt_G
[12:11]	Reserved	
[10:0]	Gap[10:0]	Line number inserted before the following menu row.

2.9.5.6 Row Attribute Jump Menu Type Format (RAtt_J)

This RAtt_J is used to redirect menu to other assigned new menu block in OSD2 memory. This is useful for controlling menu flows.

Bit	Symbol	Description
[15:14]	RAtt_ID = 10b	Must set value 10b for RAtt_J
[13:0]	Jump_MenuA[13:0]	Jump to the OSD2 RAM address, which should still point to a row attribute of menu.

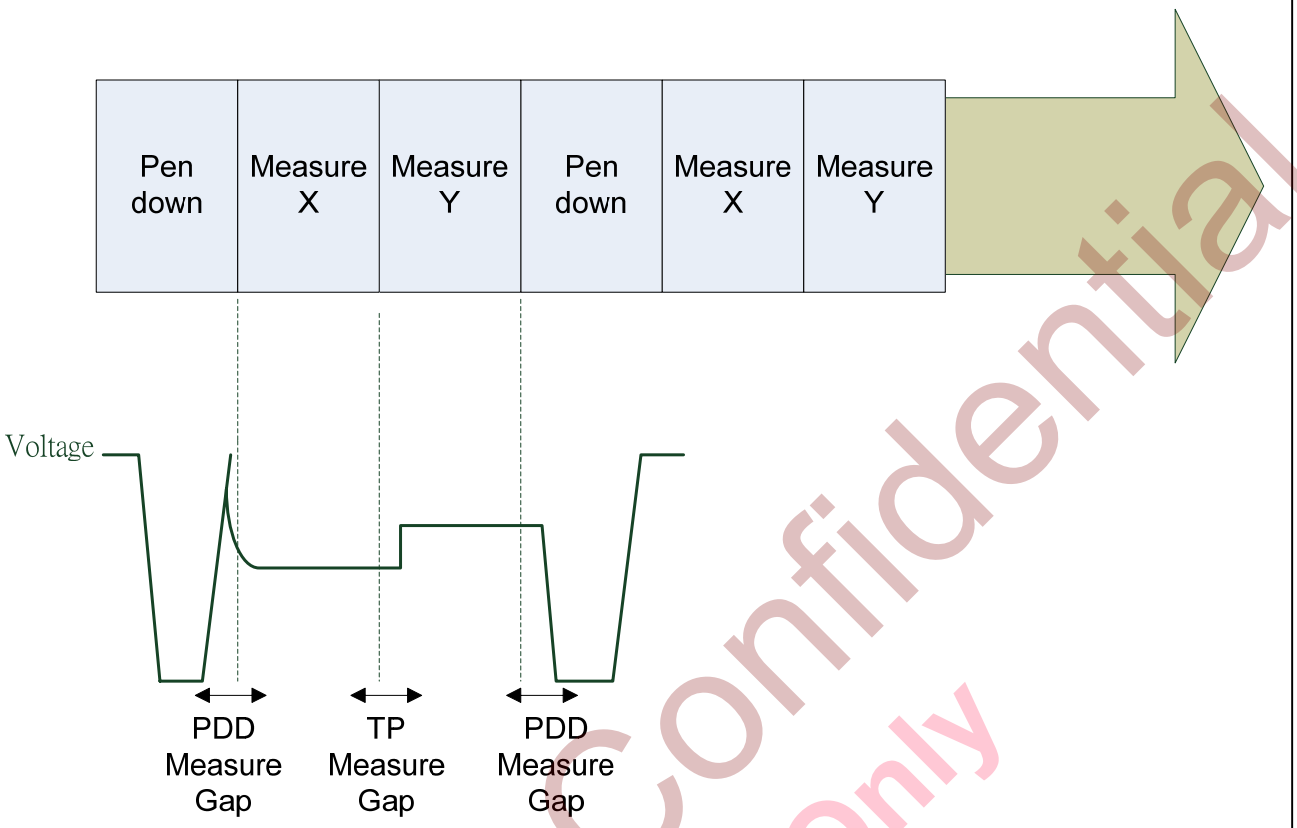
2.9.5.7 Row Attribute Horizontal Position Type Format (RAtt_H)

Bit	Symbol	Description
[15:13]	RAtt_ID = 011b	Must set value 011b for RAtt_H
[12]	BG_RGB[2]	Background color bit 2, combined with the BG_Color[1:0] in each character become 3 bits to select background remap color.
[11]	Char3BP_Yes	1: The following Char1BP index will redirect to Char3BP fonts 0: The following Char1BP index will back to Char1BP fonts
[10:0]	HStart[10:0]	Set the horizontal start position of the following menu rows.

2.9.5.8 Row Attribute Vertical Position Type Format (RAtt_V)

Bit	Symbol	Description
[15:13]	RAtt_ID = 010b	Must set value 010b for RAtt_V
[12:11]	Reserved	
[10:0]	VStart[10:0]	Set the vertical start position of the following menu rows.

2.10 Touch Panel Control



First, the resistive touch panel can provide X/Y/Z(pen down) axis voltage signals which can be converted into digital data through SAR ADC and half VDD comparator. We collected X/Y axis data among each pen down, and implemented a debouncing filter to prevent from too much variation. Having the valid data been latched into registers, we gave an interrupt to CPU and then CPU read status bits to identify pen down, pen release and pen move.

Moreover, we made programmable gaps (P6_50 and P6_60/61) while switching measuring axis to prevent from unwanted signals penetrating into design. Other programmable configurations can help to make it fit more applications, such as measure times(P6_72), SAR0_threshold (P6_41/42), bouncing threshold(P6_70/71), and pen down/release times(P6_75).

2.11 Command Queue

2.11.1 Elements of Command Queue:

- 2-byte command (write 1 ~ 8 byte)

Index	Content							
	b7	b6	b5	b4	b3	b2	b1	b0
0	0	Incr.	Page			Length = L		
1	Initial Address							
2	Data(0)							
…..	…..							
2+L	Data(L)							

- 3-byte command (write 1 ~ 125 byte)

Index	Content							
	b7	b6	b5	b4	b3	b2	b1	b0
0	1	Incr.	Page					
1	Length = L							
2	Initial Address							
3	Data(0)							
…..	…..							
3+L	Data(L)							

2.11.2 Operation:

- Write commands into queue via data port
- Set trigger source
- Debug mode (read queue data via data port)
  - Step 1: enable debug mode (P3_C0[1]=1)
  - Step 2: set queue pointer (P3_C7[6:0])
  - Step 3: read data port (P3_C5)

2.12 SPI Master – SPI Flash Command Protocol

2.12.1 Read Data Bytes at Higher Speed(FAST_Read)

The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction.

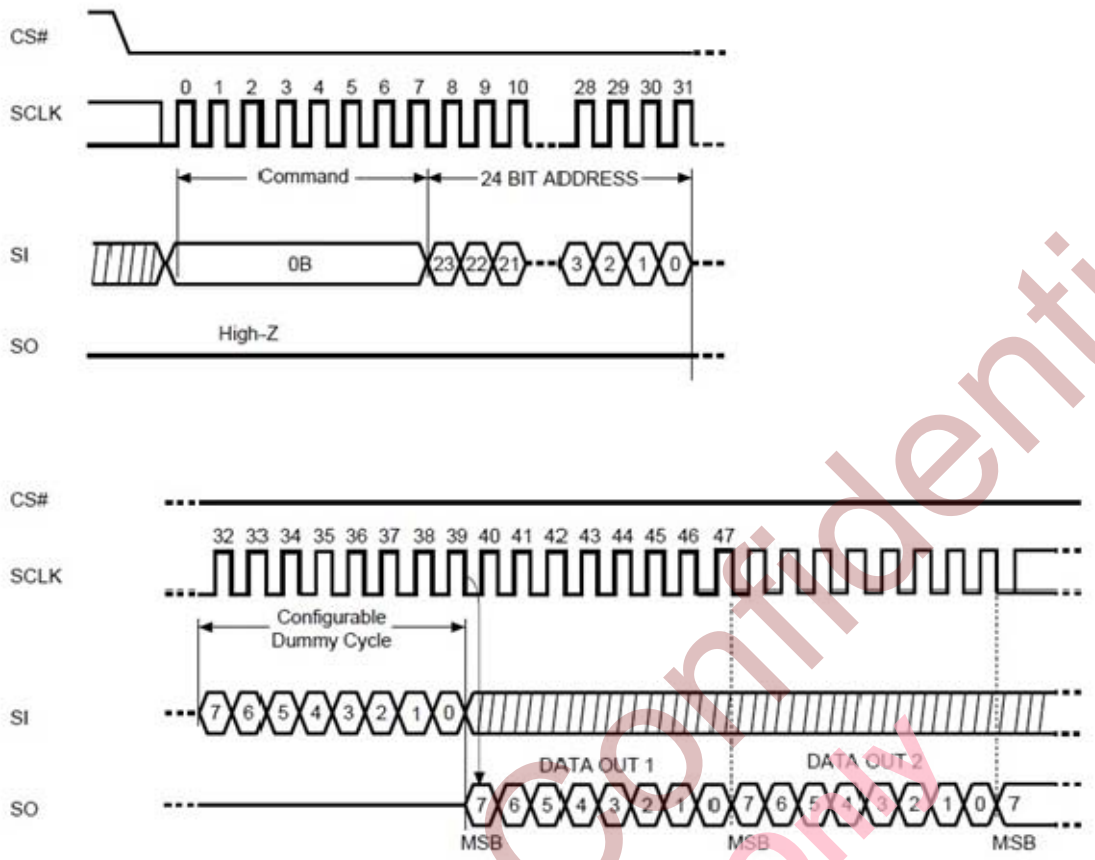
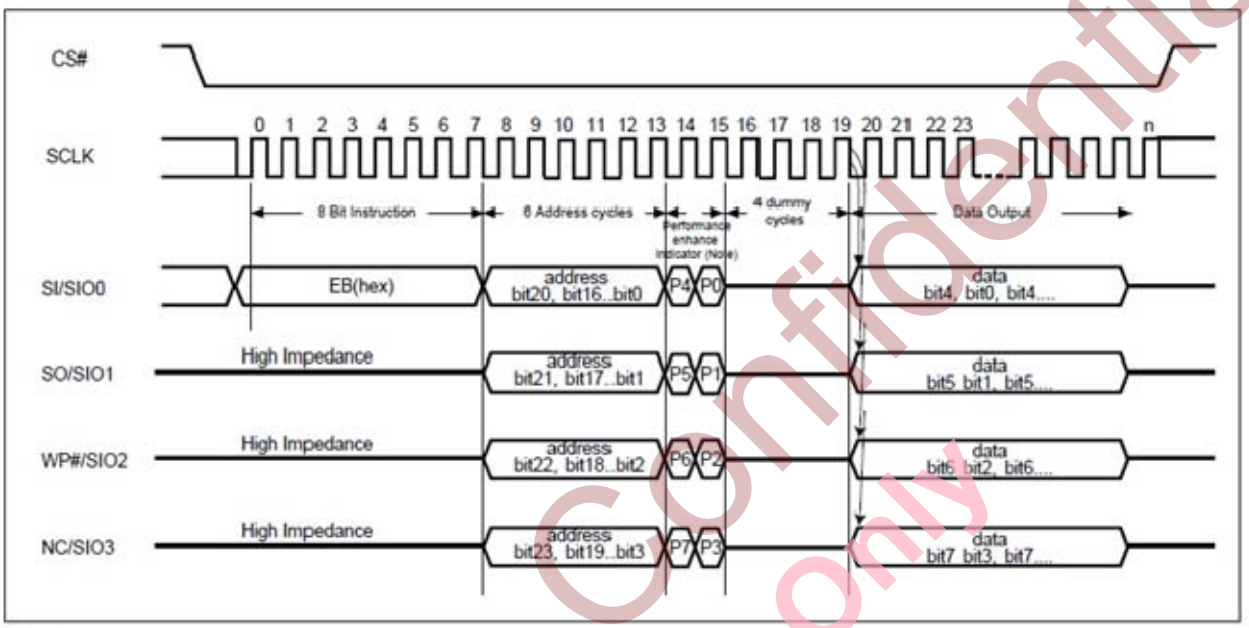


Figure 2-12-1 Read at higher speed(FAST_READ) sequence (command 0B)

2.12.2 4 x I/O Read Mode(4READ)

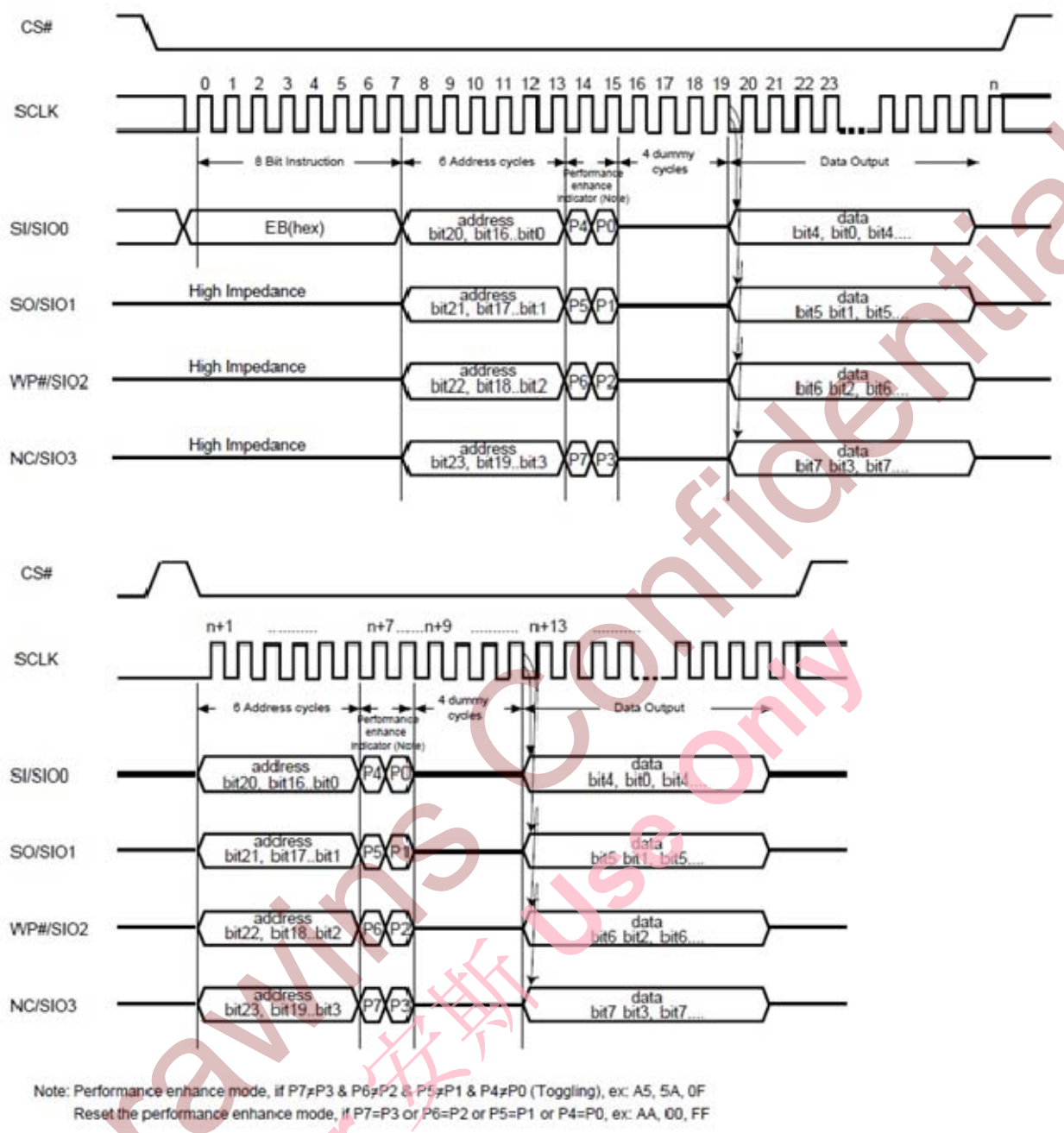
The 4READ instruction enable quad throughput of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. In the performance-enhancing mode, P[7:4] must be toggling with P[3:0]; likewise P[7:0]=A6h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewire P[7:0]==FFh,00h,AAh or 55h and afterwards CS# is raised and the lowered, the system then will escape from performance enhance mode and return to normal operation.



Notes:

1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) will enter the performance enhance mode.

Figure 2-12-2 4x I/O Read Mode sequence (command EB)



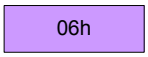
Note: Performance enhance mode, if P7≠P3 & P6≠P2 & P5≠P1 & P4≠P0 (Toggling), ex: A5, 5A, 0F
Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF

Figure 2-12-3 4 x I/O Read enhance performance mode sequence (command EB)

2.13 SPI Master – Programming guide of Instruction

2.13.1 SPI_WREN

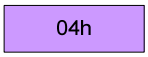
SPI_WREN: Write Enable



P6_70h <= 06h
P6_75h <= 1-000-00-0-0 b

2.13.2 SPI_WRDI

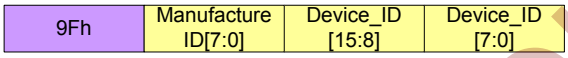
SPI_WRDI: Write Disable



P6_70h <= 04h
P6_75h <= 1-000-00-0-0 b

2.13.3 SPI_ RDID

SPI_RDID: Read ID; (Bug in T108_6S9 version)



P6_70h <= 9Fh
P6_75h <= 1-000-10-0-0 b

2.13.4 SPI_ RDSR

SPI_RDSR: Read Status Register (1 ~ unlimited); % Limited 1 byte in T108

P6_70h <= 05h
P6_75h <= 1-000-01-0-0 b

2.13.5 SPI_WRSR

SPI_WRSR: Write Status Register

WREN;
P6_70h <= 01h
P6_74h <= W_Status[7:0]
P6_75h <= 1-100-00-0-0 b

2.13.6 Windbond: SPI_WRSR

Winbond: SPI_WRSR: Write Status Register

01h	W_Data = Status [7:0]	W_Data = Status [15:8]

WREN;
P6_70h <= 01h
P6_73h <= W_Status[7:0]
P6_72h <= W_Status[15:8]
P6_75h <= 1-0110-00-0-0 b

2.13.7 SPI_READ

SPI_READ: Read Data Byte (1 ~ End), for <= 20MHz; % Not supported in T1XX

03h	Address[23:16]	Address[15:8]	Address[7:0]	R- Data (B0)	R- Data (B1)	R- Data (B2)	- - - - - -	R- Data (Bn-1)

P6_70h <= 03h
P6_71h ~ 73h <= A[7:0], A[15:8], A[23:16]
P6_75h <= 1-101-11-0-0 b

2.13.8 SPI_FAST_READ

SPI_FAST_READ: Read Data Byte (1 ~ End) at Higher Speed; % Limited 3 bytes in T108 when non-DMA

0Bh	Address[23:16]	Address[15:8]	Address[7:0]	Dummy W_Data	R- Data (B0)	R- Data (B1)	R- Data (B2)	- - - - - -	R- Data (Bn-1)

P6_70h <= 0Bh
P6_71h ~ 73h <= A[7:0], A[15:8], A[23:16]
(P6_74h <= Dummy Byte)
P6_75h <= 1-110-11-0-0 b

2.13.9 SPI_PP

SPI_PP: Page Program (for change memory bits from 1 to 0, 1 ~ 256 bytes, wrap if A[7:0] != 00h); % Limited 1 byte in T108 when non-DMA

02h	Address[23:16]	Address[15:8]	Address[7:0]	W_Data (B0)	W_Data (B1)	- - - - - -	W_Data (Bn-1)

WREN;
P6_70h <= 02h
P6_71h ~ 73h <= A[7:0], A[15:8], A[23:16]
P6_74h <= Single Write Data
P6_75h <= 1-110-00-1-0 b

2.13.10 SPI_PE

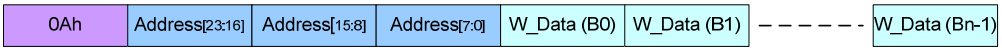
SPI_PE: Page Erase (all 256 bytes, ignore A[7:0])

DBh	Address[23:16]	Address[15:8]	Address[7:0]

WREN;
P6_70h <= DBh
P6_71h ~ 73h <= A[7:0], A[15:8], A[23:16]
P6_75h <= 1-101-00-1-0 b

2.13.11 SPI_PW

SPI_PW: Page Write, = SPI_PE + SPI_PP, sequence as SPI_PP; % Limited 1 byte in T108 when non-DMA



WREN;
P6_70h <= 0Ah
P6_71h ~ 73h <= A[7:0], A[15:8], A[23:16]
P6_74h <= Single Write Data
P6_75h <= 1-110-00-1-0 b

2.13.12 SPI_SE

SPI_SE: Sector Erase (all data in assigned sector, maybe 128 or 256 pages or …. Depends on ROM size)

WREN;
P6_70h <= D8h
P6_71h ~ 73h <= A[7:0], A[15:8], A[23:16]
P6_75h <= 1-101-00-1-0 b

2.13.13 SPI_BE

SPI_BE: Bulk Erase

P6_70h <= 20h
P6_75h <= 1-000-00-1-0 b

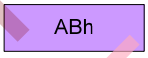
2.13.14 SPI_DP

SPI_DP: Deep Power-Down

P6_70h <= B9h
P6_75h <= 1-000-00-0-0 b

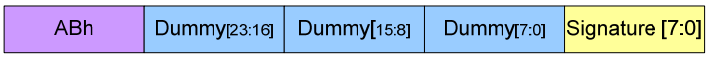
2.13.15 SPI_RES

SPI_RES: Release from Deep Power-down



P6_70h <= ABh
P6_75h <= 1-000-00-0-0 b

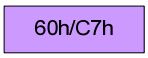
SPI_RES: Release from Deep Power-down and Read Electronic Signature



P6_70h <= ABh
P6_75h <= 1-101-01-0-0 b

2.13.16 SPI_CE

SST: SPI_CE: Chip Erase



P6_70h <= 60h or C7h
P6_75h <= 1-000-00-1-0 b

2.13.17 SST: SPI_SE

SST: SPI_SE: Sector Erase

WREN;
P6_70h <= 20h
P6_71h ~ 73h <= A[7:0], A[15:8], A[23:16]
P6_75h <= 1-101-00-1-0 b

2.13.18 SST: SPI_BE

SST: SPI_BE: Block Erase

WREN;
P6_70h <= 52h or D8h
P6_71h ~ 73h <= A[7:0], A[15:8], A[23:16]
P6_75h <= 1-101-00-1-0 b

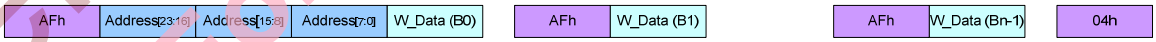
2.13.19 SST: SPI_BP

SST: SPI_BP: Byte Program

WREN;
P6_70h <= 02h
P6_71h ~ 73h <= A[7:0], A[15:8], A[23:16]
P6_74h <= Single Write Data
P6_75h <= 1-110-00-1-0 b

2.13.20 SST: SPI_AAI

SST: SPI_AAI: Auto Address Increment Program



WREN;
P6_70h <= AFh
P6_71h ~ 73h <= A[7:0], A[15:8], A[23:16]
P6_74h <= Single Write Data
P6_75h <= 1-110-00-X-0 b

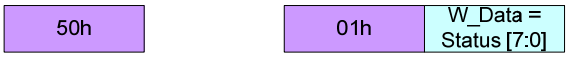
P6_74h <= Single Write Data
P6_75h <= 1-100-00-X-1 b

P6_74h <= Single Write Data
P6_75h <= 1-100-00-X-1 b

WRDI

2.13.21 SST: SPI_EWSR

SST: SPI_EWSR: Enable Write Status Register



P6_70h <= 50h
P6_75h <= 1-000-00-0-0 b

2.13.22 SST: SPI_RDID

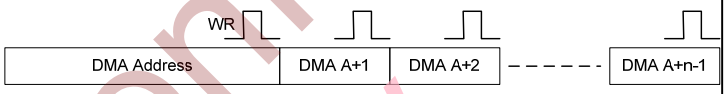
SST: SPI_RDID: Read ID

P6_70h <= 90h or ABh
P6_75h <= 1-101-10-0-0 b

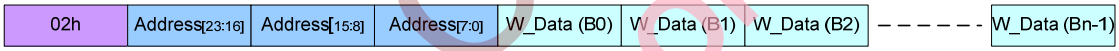
2.13.23 SPI DMA(Legacy 1x Mode)

SPI_DMA_READ: Fast Read SPI Flash ROM, then write to Scalar

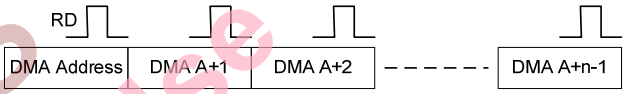
P6_70h <= 0Bh
P6_71h ~ 73h <= A[7:0], A[15:8], A[23:16]
(P6_74h <= Dummy Byte)
P6_75h <= 0-110-11-0-0 b
P6_7Ah <= DMA Transfer Count [7:0]
P6_7Bh <= {5'b0, DMA Transfer Count [10:8]};



SPI_DMA_WRITE: SPI Flash ROM, then write to Scalar



P6_70h <= 02h
P6_71h ~ 73h <= A[7:0], A[15:8], A[23:16]
P6_75h <= 0-111-00-1-0 b
P6_7Ah <= DMA Transfer Count [7:0]
P6_7Bh <= {5'b0, DMA Transfer Count [10:8]};



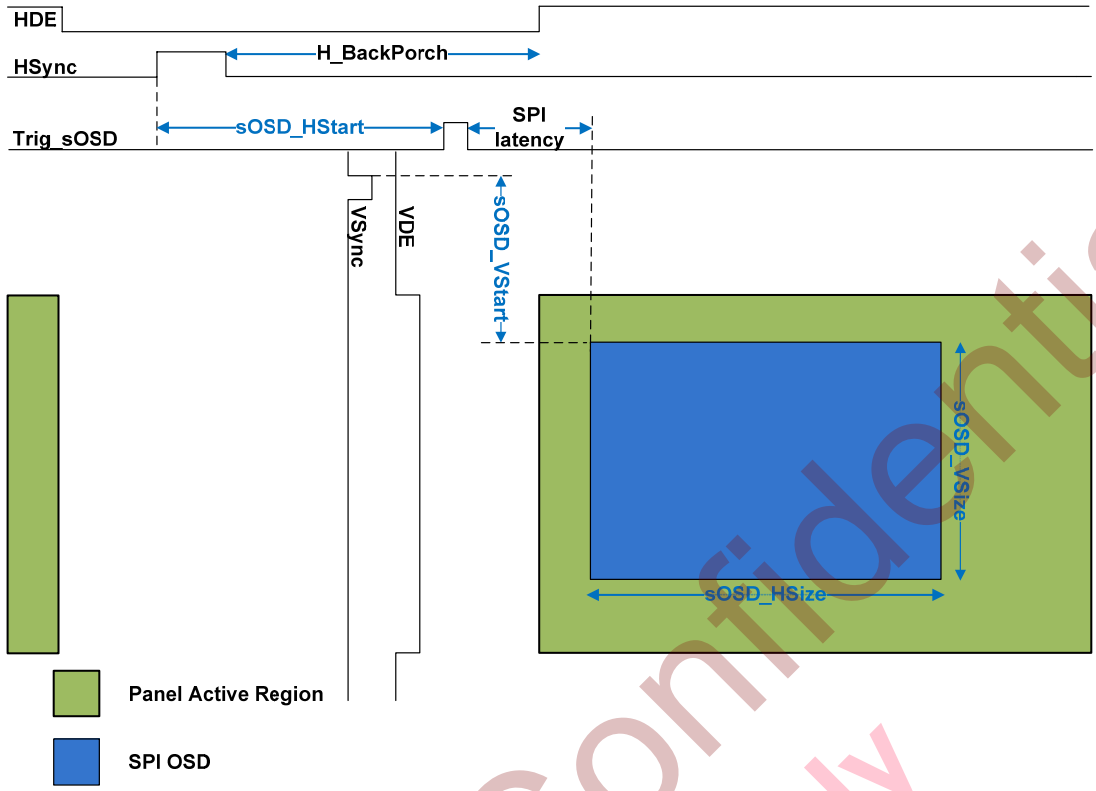
SPI_DMA Can be used as:

1. Load LUT RAM (128 Words) of SPI OSD (when sOSD_En=0)
2. Load Image (when sOSD_En=1)
3. PagePrograming Buffer (256 Bytes)

2.14 SPI-OSD

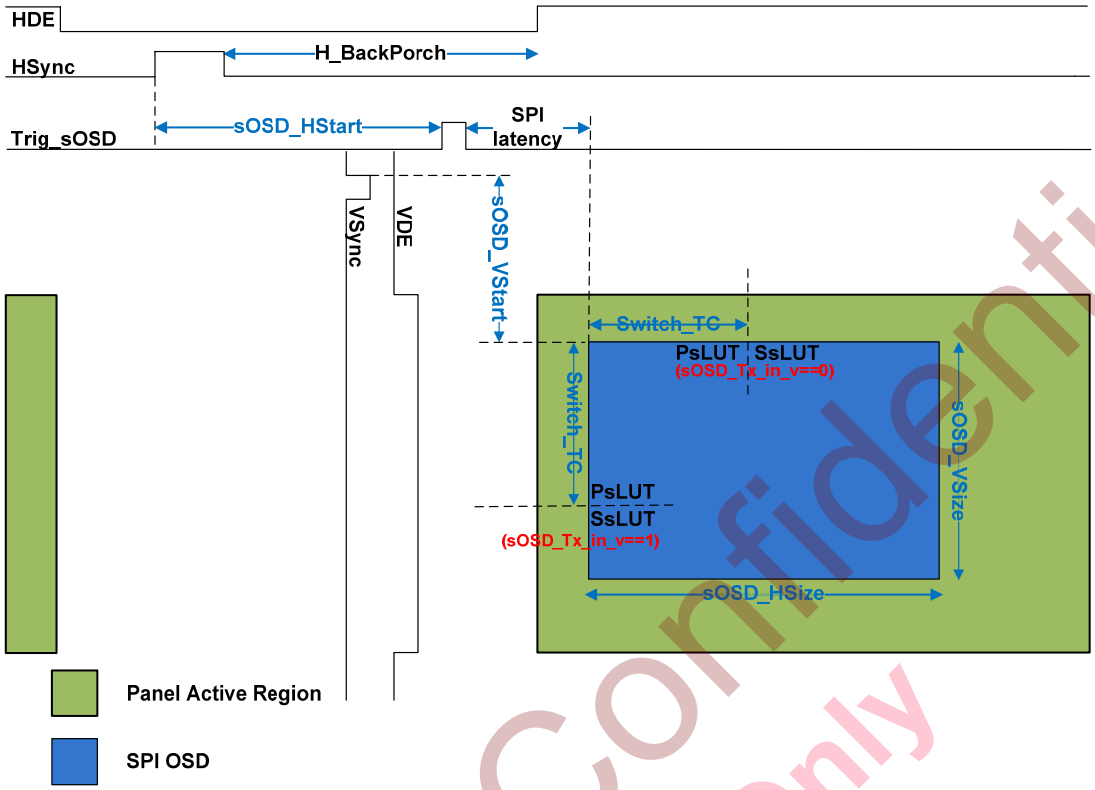
2.14.1 Register Settings to display SPI OSD / Sprite images

2.14.1.1 Display SPI OSD image using PsLUT



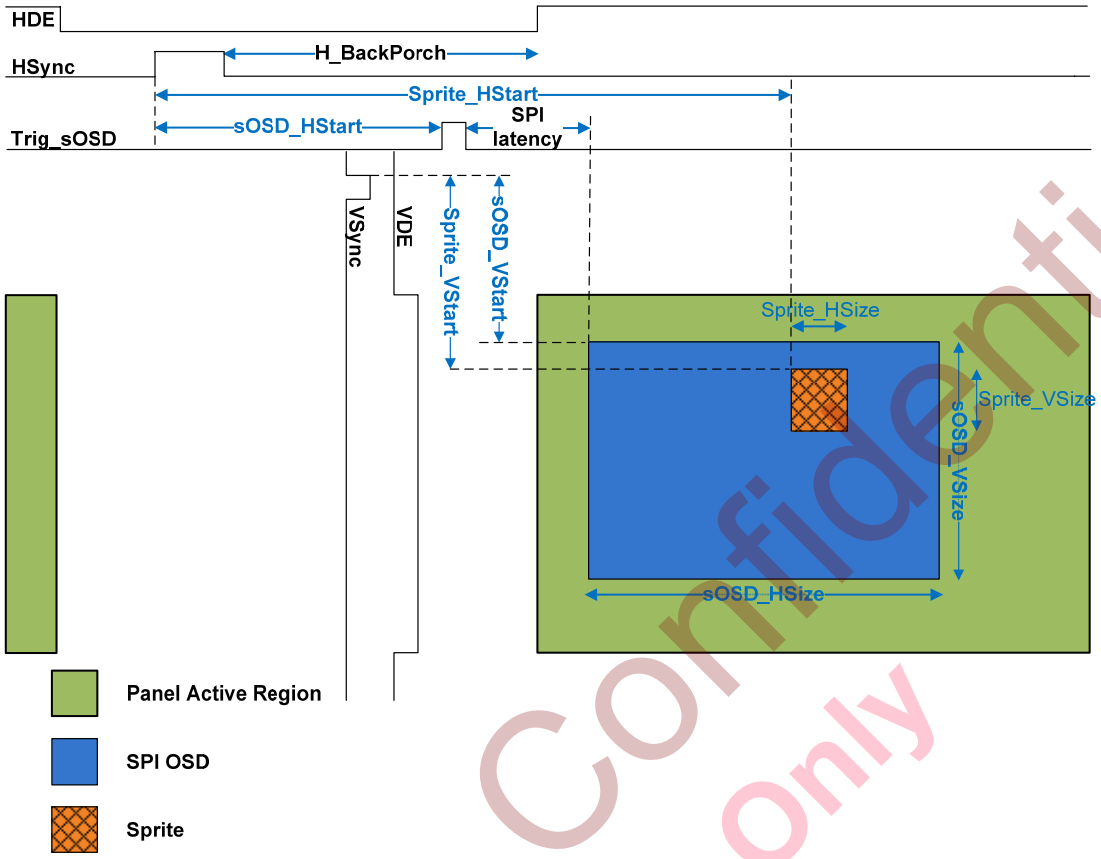
- Setting proper values to registers for the position and size of SPI OSD image
  - sOSD_HStart (P3_88, P3_89[3:0])
  - sOSD_VStart (P3_8A, P3_8B[2:0])
  - sOSD_HSize (P3_8C, P3_8D[2:0])
  - sOSD_VSize (P3_8E, P3_8F[2:0])
- Setting proper value to registers for accessing SPI OSD data in Flash memory
  - oSPI_PsLUTA (P3_93, P3_94, P3_95)
  - oSPI_ImageA (P3_96, P3_97, P3_98)
  - sOSD_LineJumpA (P3_9C, P3_9D)
- Enable SPI OSD and trigger to load PsLUT
  - TrigLoad_PsLUT (P3_9E[3])
  - sLUT_LoadOnce (P3_9E[4])
  - sOSD_En (P3_9E[7])

2.14.1.2 Display SPI OSD image using both PsLUT and SsLUT



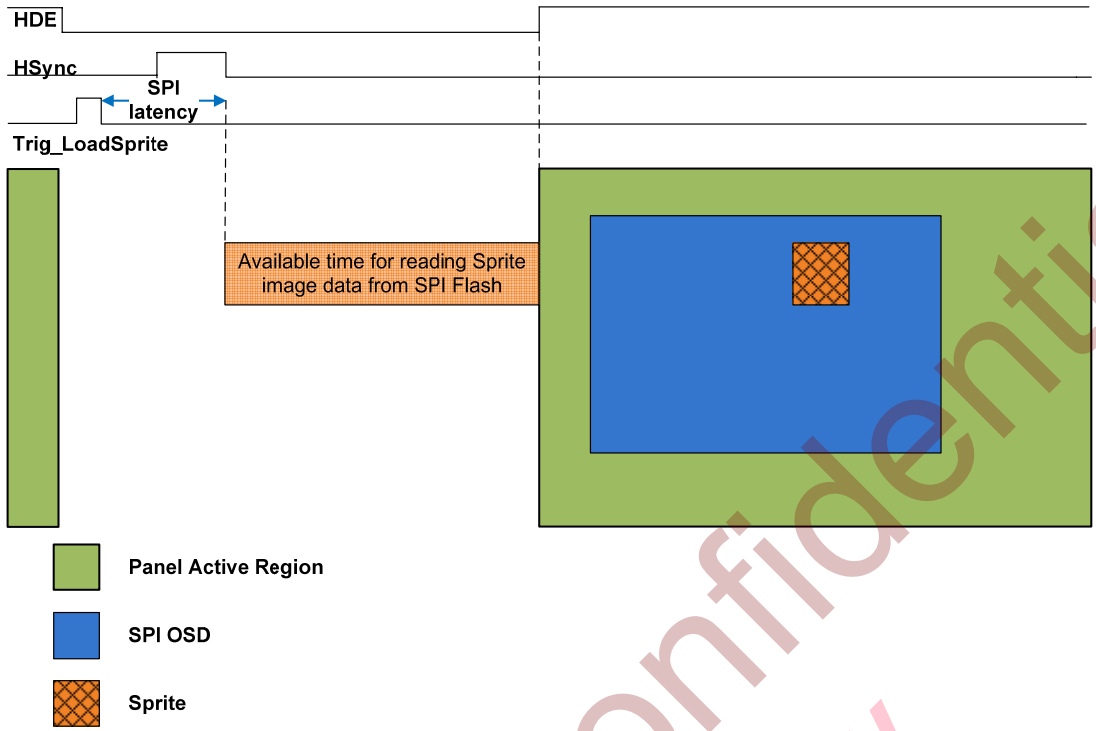
- Setting proper values to registers for the position and size of SPI OSD image (same as 2.14.1.1)
- Setting proper value to registers for accessing SPI OSD data in Flash memory
  - oSPI_PsLUTA (P3_93, P3_94, P3_95)
  - oSPI_ImageA (P3_96, P3_97, P3_98)
  - sOSD_LineJumpA (P3_9C, P3_9D)
  - oSPI_SsLUTA (P3_E0, P3_E1, P3_E2)
- Setting proper value to registers for switching LUTs
  - Switch_TC (P3_9A, P3_9B[2:0])
  - sOSD_Tx_in_v (P3_9B[6])
  - sOSD_Tx_En (P3_9B[7])
- Enable SPI OSD; trigger to load PsLUT and SsLUT
  - TrigLoad_SsLUT (P3_9E[2])
  - TrigLoad_PsLUT (P3_9E[3])
  - sLUT_LoadOnce (P3_9E[4])
  - sOSD_En (P3_9E[7])

2.14.1.2 Display SPI OSD image using PsLUT and Sprite image using SsLUT



- Setting proper values to registers for the position and size of SPI OSD image (same as 2.14.1.1)
- Setting proper value to registers for accessing SPI OSD data in Flash memory (same as 2.14.1.1)
- Setting proper values to registers for the position and size of Sprite image
  - Sprite_HStart (P3_E8, P3_E9[3:0])
  - Sprite_VStart (P3_EA, P3_EB[2:0])
  - Sprite_HSize (P3_EC)
  - Sprite_VSize (P3_ED, P3_EE[2:0])
- Setting proper value to registers for accessing Sprite data in Flash memory
  - oSPI_SsLUTA (P3_E0, P3_E1, P3_E2)
  - oSPI_SpriteA (P3_E3, P3_E4, P3_E5)
  - Sprite_LineJumpA (P3_E6, P3_E7)
- Enable SPI OSD and Sprite; trigger to load PsLUT and SsLUT
  - Sprite_En (P3_EF[7])
  - TrigLoad_SsLUT (P3_9E[2])
  - TrigLoad_PsLUT (P3_9E[3])
  - sLUT_LoadOnce (P3_9E[4])
  - sOSD_En (P3_9E[7])

2.14.2 Limitation to the width of Sprite image



- The Sprite engine reads image data (index for LUT) from SPI Flash to internal SRAM in the duratation of horizontal blanking.
- The maximum horizontal size of Sprite image is 256, while register Sprite_HSize (P3_EC) is set to '0.' But the actual size may be smaller than 256 if the duration of horizontal blanking is not long enough.
- The SPI latency, from asserting Trig_LoadSprite to fisrt Flash data back, includes the time for SPI protocol (command, address, and dummy cycle) and data path delay.

	dPLL_sOSD_2x==1 (clk_sOSD : dclko_2x = 2:1)	dPLL_sOSD_2x==0 (clk_sOSD : dclko_2x = 1:1)
Limitation to Sprite_HSize (unit: clk_sOSD cycle)	HBlanking – (SPI latency / 2)	(HBlanking – SPI latency) / 2

- If the limitation to Sprite_HSize above is smaller than 256, extending the duration of horizontal blanking is recommended.

2.14.3 Other register settings

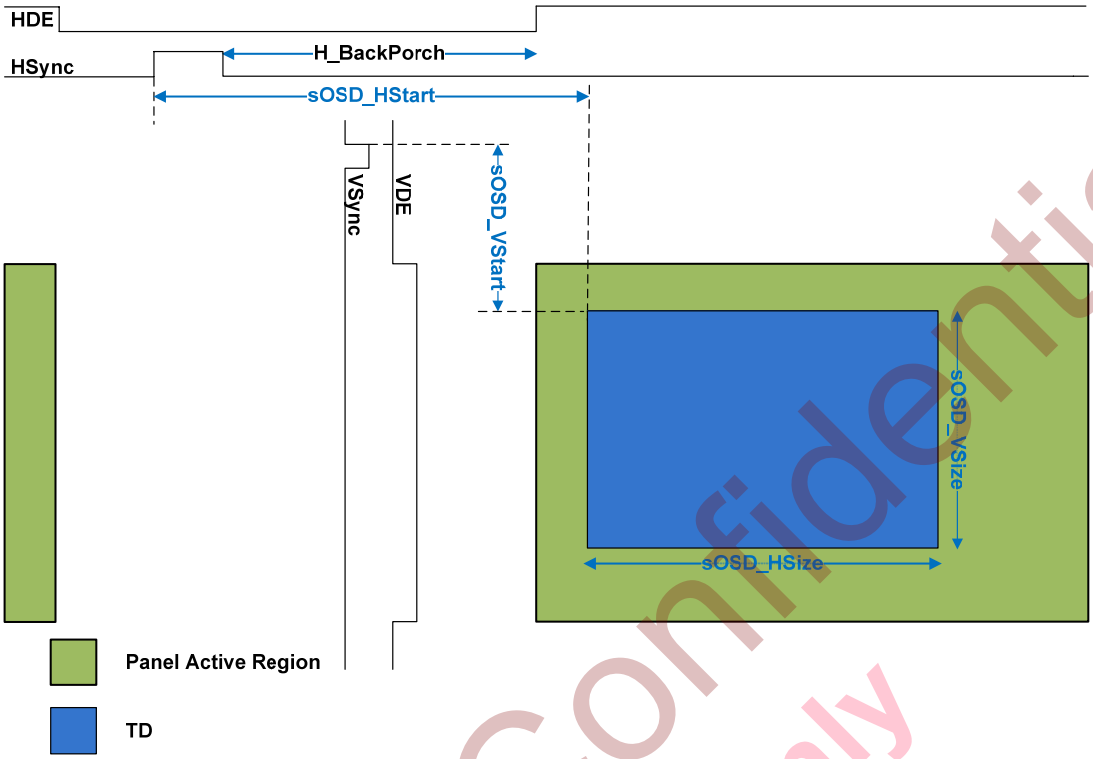
- dPLL_sOSD_2x (P0_C4[5])
  - The SPI OSD image will be 2x scaling up if clk_sOSD and dclko2x are the same ratio, which means register P0_C4[5] is '0'. And the real horizontal size of SPI OSD displayed in panel will be sOSD_HSize*2.
- spi_pre_occupy (P3_99)
  - When sharing the Flash memory with 8051, the vertical edges of SPI OSD image will tremble due to non-constant SPI latency caused by SPI arbitration. To avoid this, setting a proper value **N** to register spi_pre_occupy (P3_99) will let the arbitrator preserve the SPI bus **2*N** cycles earlier before signal Trig_sOSD asserts. It should be noted that the preservation cannot be earlier than HSync.

2.14.4 Terawins Bitmap Compression(TWBC) Decompression

	sOSD_En==1 (P3_9E[7])	sOSD_En==0 (P3_9E[7])
TWBC_enable==0 (P3_D0[7])	SPI OSD	X
TWBC_enable==1 (P3_D0[7])	TWBC Decompression	X

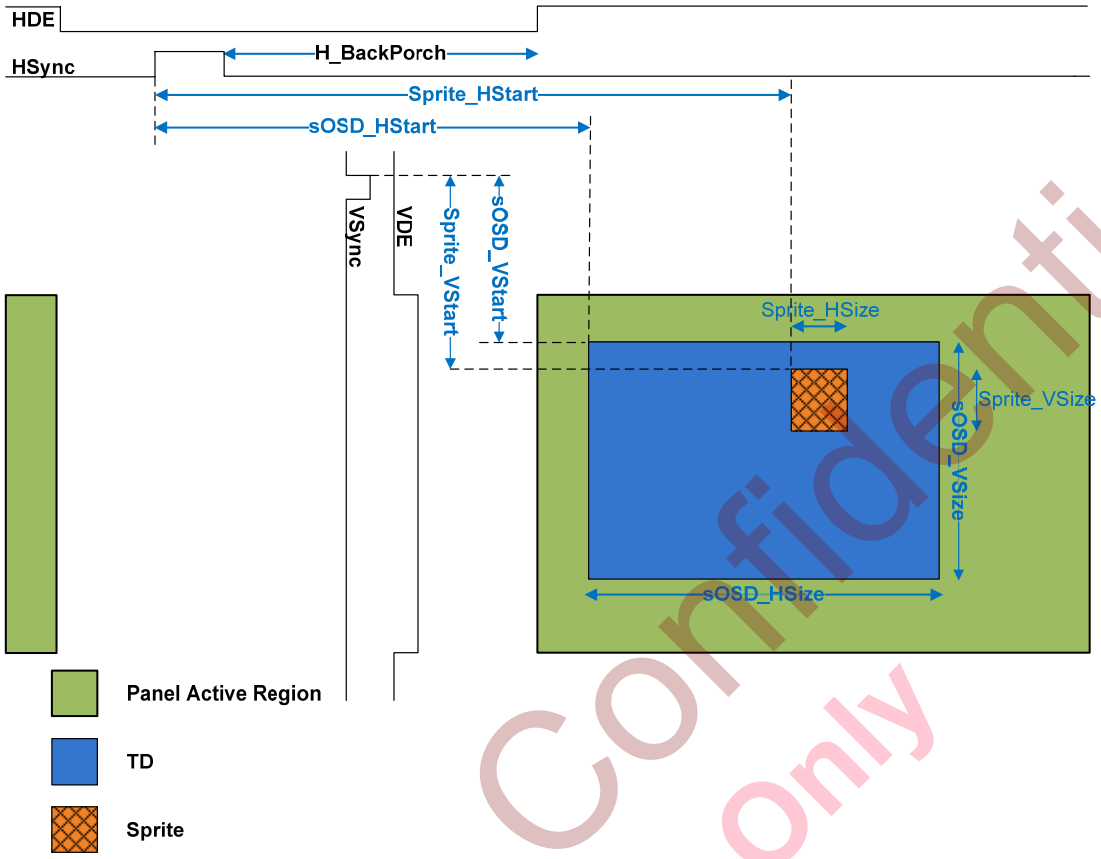
- Take image size of 800x480 for instance:
  - oSPI_ImageA (P3_96, P3_97, P3_98): the starting position of modulation bits in Flash memory
  - sOSD_LineJumpA (P3_9C, P3_9D): C8h = 200d (800 pixels * 2 (bits/pixel) / 8 (bits/byte) = 200 bytes) ;
  - TWBC_color_addr (P3_D1, P3_D2, P3_D3): the starting position of AB colors in Flash memory
  - TWBC_color_hsize (P3_D4, P3_D5): 328h = 808d ((800+8) pixels / 4 (x-way-pixels/block) * 32 (bits / block) / 8 (bits/byte) = 808 bytes)
- Limitation to the starting position:
  - Assume oSPI_ImageA_0 and TWBC_color_addr_0 for the origin (0,0) of the image.
  - Considering the starting position (x, y), where x and y must be multiples of 4:
    - oSPI_ImageA = oSPI_ImageA _0 + y * sOSD_LineJumpA + x / 4
    - TWBC_color_addr = TWBC_color_addr_0 + (y / 4) * TWBC_color_hsize + x

2.14.4.1 Display TWBC image



- Setting proper values to registers for the position and size of TWBC image
  - sOSD_HStart (P3_88, P3_89[3:0])
  - sOSD_VStart (P3_8A, P3_8B[2:0])
  - sOSD_HSize (P3_8C, P3_8D[2:0])
  - sOSD_VSize (P3_8E, P3_8F[2:0])
- Setting proper value to registers for accessing TWBC data in Flash memory
  - oSPI_ImageA (P3_96, P3_97, P3_98)
  - sOSD_LineJumpA (P3_9C, P3_9D)
  - TWBC_color_addr (P3_D1, P3_D2, P3_D3)
  - TWBC_color_hsize (P3_D4, P3_D5[2:0])
- Enable TWBC and trigger to load PsLUT
  - TWBC_enable (P3_D0[7])
  - sOSD_En (P3_9E[7])

2.14.4.2 Display TWBC image and Sprite image using SsLUT



- Setting proper values to registers for the position and size of TWBC image (same as 2.14.4.1)
- Setting proper value to registers for accessing TWBC data in Flash memory (same as 2.14.4.1)
- Setting proper values to registers for the position and size of Sprite image
  - Sprite_HStart (P3_E8, P3_E9[3:0])
  - Sprite_VStart (P3_EA, P3_EB[2:0])
  - Sprite_HSize (P3_EC)
  - Sprite_VSize (P3_ED, P3_EE[2:0])
- Setting proper value to registers for accessing Sprite data in Flash memory
  - oSPI_SsLUTA (P3_E0, P3_E1, P3_E2)
  - oSPI_SpriteA (P3_E3, P3_E4, P3_E5)
  - Sprite_LineJumpA (P3_E6, P3_E7)
- Enable TWBC and Sprite; trigger to load SsLUT
  - Sprite_En (P3_EF[7])
  - TWBC_enable (P3_D0[7])
  - TrigLoad_SsLUT (P3_9E[2])
  - sLUT_LoadOnce (P3_9E[4])
  - sOSD_En(P3_9E[7])

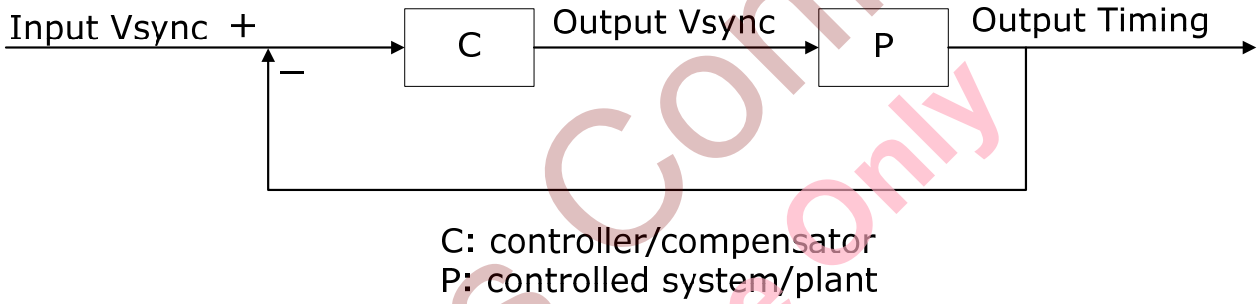
2.15 UART0

To use UART0, following pin function selection should be set for RX &TX:
RS232_sel = 1 (P1_FD[0] = 1'b1)
CPUINT_oeSel[1:0] = 2'b01 (P1_AC[1 :0] = 2'b01)
PD_TotalPad_ = 1'b1 (P0_E0[7] = 1'b1

2.16 UART1

UART1 can only be used with **hardware trapping SPI1_EN=1'b0**, and to use UART1, following pin function selection should be set for RX &TX:
RS232TX1_oeSel = 1'b1 (P1_AC[4] = 1'b1)
PD_TotalPad_ = 1'b1 (P0_E0[7] = 1'b1)
Using UART1 with flow control, pin function selection for RTS & CTS should also be set:
RLUD_oeSel = 2'b10 (P1_AC[3:2] = 2'b10

2.17 FPLL



The difference between input vsync and output vsync is checked and feedback to controller to tracking input vsync behavior. The quantity of difference represents if input vsync suddenly lost or changed to other input source.

3 Register Map

PAGE0 LOW NIBBLE OF SUBADDRESS																		
Addr		Function Block	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
PAGE0 HIGH NIBBLE OF SUBADDRESS	0h	ADC R/G/B	R/G/B LPF			APLL	Clamp	R/G/B Offset Tune		R/G/B GAIN Control				R/G/B Offset Adjust		Misc. Ctrl	Gain rbk	Power Down
	1h		Polarity	Mid clamp	slicer	Vsync Sep	Sync.	PLL Divider		VCO CP	ADC MUX	YCbCr Swap	AGC	Dither Diff	Blank	sel	ADC rbk	
	2h		Phase	HS/VS	Phase ATK			Res.	Boundary Detect									
	3h	Input sel/detect	Input setting	Input select	Res.	Missing det	1ms count	1ms timer		V miss count	H miss count		VSYN DLY	HSYN DLY	VD/656 Crop			
	4h		ADC Output Timing Fine Tune							ADC Capture Timing								
	5h	Input timing detection	ShortVS detect FrmXclk_sum					Input timing detection H/V/HS/VS										
	6h	Pixel Enhancement	DXTi	Peaking	DLTi / DCTi			Color Adjustment B/C/H/S					BLE/WLE					
	7h	Main Scaling Machine	Misc. & Coefficient		Scaling Ratio			H Aspect Ratio					Scaler Misc.					
	8h	Main LCD Output Timing Control	Res.	LB Timing									Border Mask					
	9h	Image Control	Gamma					Reserved			Int Pattern	Reserved			Internal Pattern			
	Ah	OSD	Contrast			Brightness					OSD2				Reserved			
	Bh	LCD Output Timing Control	Panel Output Window															
	Ch		Signal Timing										Output PLL					LVDS
	Dh		LVDS delay control							sRGB interlace	Main Fetch Start				Main Fetch Size			
	Eh	Misc	Power Management		Global Shadow	PDn_Bias_			PDn Bypas	Res.	PWM1	PWM4		656 enc	Res.	Res.		XCLK 2MC
	Fh	ID	I2C & IDs							Reserved							Pin Contol	PAGE

PAGE1 LOW NIBBLE OF SUBADDRESS																	
Addr		Function Block	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
PAGE1 HIGH NIBBLE OF SUBADDRESS	0h	ADC SOY	SOY Track								Reserved			SOY PreFilter				
	1h	ADCV	ADC V Control					Sync delay for CP		Free-run hs		Reserved						
	2h	TCON	TCON															
	3h	TCON	TCON							FpII Control								
	4h	IR1	IR Control								Reserved						WDT	
	5h	GPIOE DDC	GPIOE								SetClr	Reserved		DDC				
	6h	PWM2/3	PWM23 Limit		PWM2/PWM3							PWM range				PWM targe		
	7h	PWM pi control	GPIO clear					PWM2/PWM3 pi control										
	8h	GPIOA/GPIOB	GPIOA											GPIOB				
	9h	GPIOC/GPIOD	GPIOC											GPIOD				
	Ah	Pad Control	DS 0~27				PE 0~27				Reserved		PS 20~23		Res.	PinFunctionsel	Reserved	Scratch Reg.
	Bh	Main Color Space Convert	YUV To RGB Coef									YUV2 RGB 2	Reserved					
	Ch	ADC CP	ADC Color Range & Probing															
	Dh	ITU656 Decoder	Generate HSync / Vsync					ITU656 Input Capture Window					Ramp smooth	ITU656 Input Capture Window				
	Eh	Scratch	Scratch Register															
	Fh	Reserved	Reserved													I8051control		Page

PAGE2 LOW NIBBLE OF SUBADDRESS																		
Addr		Function Block	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
PAGE2 HIGH NIBBLE OF SUBADDRESS	0h	CVD	CVD Ctrl				HAGC	CVD Control			Contrast	Brightness	Saturation	Hue	CAGC	CKILL	CPeak	CVD Ctrl
	1h		Peak White	Gate Ctrl	AGC Gate				Lock Count	HLoop	CDTO			HDTO				
	2h		HSync Ctrl								H Backporch		H Blank		Burst Gate		HStart	H Width
	3h		VStart	V Width	VSync Ctrl								Status 1	Status 2	Status 3			Reset
	4h		Auto Mode	AM Status	MDET Line		V50 Bst		V60 Bst		Abs Phase1		Abs Phase2		Phase Inc3			
	5h		Phase Inc1				Phase Inc2				Ex Bst			AM Debug				
	6h		AM Debug						NR					Comb		Noise TH		
	7h		HDTO Status				CDTO Status				GAIN Status			CAGC Status				Noise Status
	8h		Luma Peak	CVD Misc												Reserved		
	9h	ADC Y/C																
	Ah	FeH_Core	FeH Control															
	Bh		FeH Gain															
	Ch		FeH_Step_Inc11~48															
	Dh		FeH_Step_Inc51~88															
	Eh	I2C Host	I2C Host													Reserved		
	Fh	Reserved	Reserved															

PAGE3 LOW NIBBLE OF SUBADDRESS																	
Addr		Function Block	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
PAGE3 HIGH NIBBLE OF SUBADDRESS	0h	Auto offset calibration	Auto offset calibration															
	1h	H/V Blur	Reserved											H/V Blur				
	2h	SAR0/SAR1/ Touch Panel	SAR0			SAR1			Res.	Touch Panel Control								
	3h		Reserved											Touch Panel Read Back				
	4h		TP Measure Contol	Touch Panel Read Back														
	5h		TP Bouncing Control						Reserved					SAR Value Step Check				
	6h	Vivid Color	Vivid Color		Reserved			Vivid Color						Reserved				
	7h	ACE	Reserved											Adaptive contrast enhancement				
	8h	SPI OSD	Force aB	Reserved					sOSD									
	9h	SPI OSD	Emu Base			PsLUT Base			Image Base			Misc. Contrl			Line Jump Addr		Emu Control	
	Ah	ICACHE to SPI Nor Mapping	ICACHE to SPI Nor Mapping													Reserved		
	Bh	ICACHE statistics	ICACHE statistics										Reserved					
	Ch	Command queue	Command queue control														Reserved	
	Dh	SPI OSD	TWBC Decompression										Reserved					
	Eh	SPI OSD	SsLUT Base			Sprite Base			Sprite Line Jump Addr	Sprite H/V Start/Size Control								Sprite aB
	Fh	BIST	BIST Enable/Done/Failed										Reserved					

PAGE4 LOW NIBBLE OF SUBADDRESS																	
Addr		Function Block	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
PAGE4 HIGH NIBBLE OF SUBADDRESS	0h	UART0																
	1h																	
	2h																	
	3h																	
	4h																	
	5h																	
	6h																	
	7h																	
	8h																	
	9h																	
	Ah																	
	Bh																	
	Ch																	
	Dh																	
	Eh																	
	Fh																	

PAGE5 LOW NIBBLE OF SUBADDRESS																	
Addr		Function Block	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
PAGE5 HIGH NIBBLE OF SUBADDRESS	0h	UART1																
	1h																	
	2h																	
	3h																	
	4h																	
	5h																	
	6h																	
	7h																	
	8h																	
	9h																	
	Ah																	
	Bh																	
	Ch																	
	Dh																	
	Eh																	
	Fh																	

PAGE6 LOW NIBBLE OF SUBADDRESS																	
Addr		Function Block	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
PAGE6 HIGH NIBBLE OF SUBADDRESS	0h	Reserved	Reserved															
	1h	Interrupt Status	Reserved		Interrupt Staturs							Reserved						
	2h	GPIOF	GPIOF									Reserved						
	3h	Sub Path Input sel/detect	Input setting	Input select	Sub select	Reserved				V miss count	H miss count	VSYN DLY	HSYN DLY	VD/656 Crop				
	4h	Sub path Input timing detection	ShortVS detect FrmXclk_sum				Sub path Input timing detection H/V/HS/VS											
	5h	LVDS TX test	LVDS TX test Patterns					Reserved										
	6h	SPI for i8051																
	7h	SPI for sOSD										Reserved						
	8h	SPI Arbitrator	SPI Arbitrator Control				Reserved											
	9h		Reserved															
	Ah		Reserved															
	Bh		Reserved															
	Ch		Reserved															
	Dh		Reserved															
	Eh		Reserved															
	Fh	Reserved	Reserved															

4 Register Description

4.1 ADC R/G/B/V Register Set

4.1.1 Channel R Clamp Voltage Selection Register

Address Offset: P0_00h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	LPF_EN	Enable 2nd-order sallen-key low pass filter 0: bypass
[6:4]	R/W	R_LPF_Sel[2:0]	Low-pass filter bandwidth selection for ADC0 000 : 200MHz 001 : 175 MHz 010 : 150 MHz 011 : 105 MHz 100 : 60 MHz 101 : 35 MHz 110 : 12 MHz 111 : 6.5MHz
[3]	RO	Reserved	
[2:0]	R/W	R_ClampVolt_Sel[2:0]	Channel Red (ADC0) clamp voltage selection

4.1.2 Channel G Clamp Voltage Selection Register

Address Offset: P0_01h Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:4]	R/W	G_LPF_Sel[2:0]	Low-pass filter bandwidth selection for ADC1 000 : 200MHz 001 : 175 MHz 010 : 150 MHz 011 : 105 MHz 100 : 60 MHz 101 : 35 MHz 110 : 12 MHz 111 : 6.5MHz
[3]	RO	Reserved	
[2:0]	R/W	G_ClampVolt_Sel[2:0]	Channel Green (ADC1) clamp voltage selection

4.1.3 Channel B Clamp Voltage Selection Register

Address Offset: P0_02h Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:4]	R/W	B_LPF_Sel[2:0]	Low-pass filter bandwidth selection for ADC2 000 : 200MHz 001 : 175 MHz 010 : 150 MHz 011 : 105 MHz 100 : 60 MHz 101 : 35 MHz 110 : 12 MHz 111 : 6.5MHz

[3]	RO	Reserved	
[2:0]	R/W	B_ClampVolt_Sel[2:0]	Channel Blue (ADC2) clamp voltage selection

4.1.4 APLL Setting / VCO select / Low Pass Filter Enable

Address Offset: P0_03h Default Value: 01h

Bit	Access	Symbol	Description
[7]	R/W	APLL_Coast_Leading	
[6]	RO	Reserved	
[5:4]	R/W	APLL_Test[1:0]	LPLL test control pin
[3:2]	RO	Reserved	
[1:0]	R/W	ADC_Discharge	Fine tune charge pump current

4.1.5 Sync Tip Clamp Register

Address Offset: P0_04h Default Value: 2Fh

Bit	Access	Symbol	Description
[7:5]	R/W	STip_ClampPlacement	Sync. tip clamp placement
[4:0]	R/W	STip_ClampDuration	Sync. tip clamp duration

4.1.6 Channel R Offset Tune Register

Address Offset: P0_05h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	DC_Cal_Blank	
[6]	R/W	B_Decrease	Channel blue decrease (1) or increase (0) by B_Offset_Tune[3:0]
[5]	R/W	G_Decrease	Channel green decrease (1) or increase (0) by G_Offset_Tune[3:0]
[4]	R/W	R_Decrease	Channel red decrease (1) or increase (0) by R_Offset_Tune[3:0]
[3:0]	R/W	R_Offset_Tune[3:0]	Channel red offset fine tune

4.1.7 Channel G, B Offset Tune Register

Address Offset: P0_06h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	B_Offset_Tune[3:0]	Channel blue offset fine tune
[3:0]	R/W	G_Offset_Tune[3:0]	Channel green offset fine tune

4.1.8 ADC Channel 0 Static Gain

Address Offset: P0_07h Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	ADC_RGAIN	This register can set a fixed gain for ADC channel 0 when static gain control is enabled

4.1.9 ADC Channel 1 Static Gain

Address Offset: P0_08h Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	ADC_GGAIN	This register can set a fixed gain for ADC channel 1 when static gain control is enabled

4.1.10 ADC Channel 2 Static Gain

Address Offset: P0_09h Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	ADC_BGAIN	This register can set a fixed gain for ADC channel 2 when static gain control is enabled

4.1.11 ADC Channel 0 Offset

Address Offset: P0_0Ah Default Value: 80h

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_Red_Offset	ADC Channel 0 DC Offset Control
[1:0]	RO	Reserved	

4.1.12 ADC Channel 1 Offset

Address Offset: P0_0Bh Default Value: 80h

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_Green_Offset	ADC Channel 1 DC Offset Control
[1:0]	RO	Reserved	

4.1.13 ADC Channel 2 Offset

Address Offset: P0_0Ch Default Value: 80h

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_Blue_Offset	ADC Channel 2 DC Offset Control
[1:0]	RO	Reserved	

4.1.14 ADC General Control Configuration Register

Address Offset: P0_0Dh Default Value: 20h

Bit	Access	Symbol	Description
[7:6]	R/W	CLPMD[1:0]	Clamping mode Mode: Type 0, 3: Fixed window 1, 2: Locked Window
[5]	R/W	DC_Clamp_En	DC Clamping Enable
[4]	R/W	Clamp_Source_Sel	Clamping Source Selection
[3]	R/W	VPeak_Video	vmode, 1: video mode, 0: RGB mode
[2]	RO	DC_Calib_Ready	DC Calibration Ready
[1]	R/W	DC_Calib_En	DC Calibration Enable
[0]	R/W	DC_Calib_mode	DC Calibration Mode Mode: Type 0: minimum 1: average

4.1.15 ADC Gain ReadBack

Address Offset: P0_0Eh Default Value: -

Bit	Access	Symbol	Description
[7:0]	R	adc_gain_readback[7:0]	ADC automatic gain control read back.

4.1.16 ADC Power Down Control

Address Offset: P0_0Fh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	PD_SOY_	1: Power up 0: Power down
[6]	R/W	PD_Ch2_ (B)	1: Power up 0: Power down
[5]	R/W	PD_Ch1_ (G)	1: Power up 0: Power down

[4]	R/W	PD_Ch0_ (R)	1: Power up 0: Power down
[3:2]	R/W	SOY_Hysteresis[1:0]	Hysteresis selection 00: 8mV, 01: 4mV, 10: 2mV, 11: 0mV
[1]	R/W	SOY_PreFilter	Enable SOY Prefilter
[0]	RO	Reserved	

4.1.17 ADC Polarity Control

Address Offset: P0_10h Default Value: E8h

Bit	Access	Symbol	Description
[7]	RO/WO	HSi_Polarity / HSi_Inv_	When Read: get input HSync polarity When writing, to invert (0) or non-invert (1) input HSync
[6]	RO/WO	VSi_Polarity / VSi_Inv_	When Read: get input VSync polarity When writing, to invert (0) or non-invert (1) input VSync
[5]	R/W	SOY_Inv_	Invert SOY inupt
[4]	R/W	Auto_Polarity	Set to 1 for enabling auto-adjusting HSync/VSync polarity.
[3]	R/W	Clamp_Polarity	Set to 1 for controlling Clamp positive polarity.
[2]	R/W	Clamp_Sel_GfbHS	Set to 1 to use PLL feedback HSync as clamp reference
[1]	R/W	Clamp_Leading	Set to 1 to use leading edge of HSync as clamp reference point.
[0]	R/W	Clamp_Sel_RGB	Clamp control by: 1: RGB/SOY logic, 0: VD logic.

4.1.18 ADC Clamping Control Register

Address Offset: P0_11h Default Value: 98h

Bit	Access	Symbol	Description
[7:5]	R/W	SOY_Threshold[2:0]	Voltage threshold for SOY slicing
[4:3]	R/W	SOY_Discharge[1:0]	SOY discharge option
[2]	R/W	BSCALE	ADC Channel 2 Clamping Mode 0: Clamp to Ground; 1: Clamp to mid-scale
[1]	R/W	GSCALE	ADC Channel 1 Clamping Mode 0: Clamp to Ground; 1: Clamp to mid-scale
[0]	R/W	RSCALE	ADC Channel 0 Clamping Mode 0: Clamp to Ground; 1: Clamp to mid-scale

4.1.19 SOY Status / Clamp Setting

Address Offset: P0_12h Default Value: 06h

Bit	Access	Symbol	Description
[7]	R/W	En/Done_Slicer_Status	When read：get flag of slicer status ready or not When write：to enable monitoring slicer status
[6:5]	R/W	Slicer_Status[1:0]	0：Slicer always low, 1：always high, 2：almost low, 3：almost high
[4]	R/W	SOY_Filter	Enable SOY low pass filter
[3:2]	R/W	SOY_Clamp_Placement	SOY Clamp Placement
[1:0]	R/W	SOY_Clamp_Duration	SOY Clamp Duration

4.1.20 VSync Separation Register

Address Offset: P0_13h Default Value: 08h

Bit	Access	Symbol	Description
[7]	RO	CSync_Detect_Done	flag of whether CSync Detection is done or not
[6]	RO	Fs_TooFast	Get 1 if CSync Detecting operation clock is too fast

[5]	R/W	En_CSync_Detect	Set to 1 for enabling CSync Detection function
[4]	R/W	Short_Frame	Reserved for chip testing, should set 0 for normal operation
[3]	R/W		Reserved for special case, set to 1 for normal conditions
[2]	R/W	ReSync_VsFP	Reserved for special case, set to 0 for normal conditions
[1:0]	R/W	Div_To14[1:0]	00b: power down or reset, 01b: XCLK/1, 10b:XCLK/2 (normal operation for XCLK=27MHz); 11b: XCLK/3

4.1.21 Sync Routine Control

Address Offset: P0_14h Default Value: D1h

Bit	Access	Symbol	Description
[7]	R/W	HS2PLL_Polarity	HRef polarity
[6]	R/W	Coast2PLL_Polarity	Coast polarity
[5]	R/W	ADC_is_RGB	ADC Color space select: Set 1 for RGB input, 0 for YPbPr input.
[4]	R/W	HSo_Sel_Fdbk	ADC HSo source from PLL when set to 1
[3]	R/W	HRef_Sel_SOY	PLL HRef from: 1: SOY Slicer (SOY); 0: HS input pin (SS/CS)
[2]	R/W	VS_Sel_Sep	ADC VSo from: 1: VSync Detect (SOY/CS); 0: VS input pin (SS)
[1]	R/W	Coast_Sel_Sep	PLL Coast from: 1: VSync Detect (SOY/CS); 0: Ground (SS)
[0]	R/W	En_Fake_HS	Should keep in “0”

4.1.22 Line Lock PLL Divider Register 1

Address Offset: P0_15h Default Value: 5Ah

Bit	Access	Symbol	Description
[7:0]	R/W	APLL_Div[7:0]	PLL divider LSB

4.1.23 Line Lock PLL Divider Register 2

Address Offset: P0_16h Default Value: 43h

Bit	Access	Symbol	Description
[7]	R/W	APLL_PwrDn_	1: power up, 0: power down
[6]	R/W	APLL_Sel_HighFreq	Reserved for testing, 1: high freq., 0: low freq.
[5]	R/W	APLL_Reset_	1: Normal operation for RGB and SOY inputs 0: Reset Line-lock PLL
[4]	RO	ADC_Clock_From	ADC clock source: 1: XCLK; 0:APLL output
[3:0]	R/W	APLL_Div[11:8]	PLL divider MSB

4.1.24 VCO & Charge Pump Register

Address Offset: P0_17h Default Value: 48h

Bit	Access	Symbol	Description
[7:6]	R/W	ADC_VCO[1:0]	VCO gain selection
[5:3]	R/W	ADC_ChargePump[2:0]	000：50μA 001：100μA 010：150μA 011：250μA 100：350μA 101：500μA 110：750μA 111：1500μA
[2:0]	RO	Reserved	

4.1.25 Analog Source MUX Selection

Address Offset: P0_18h Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:4]	R/W	AI_Ch2_Sel[1:0] (B)	Analog mux selection for ADC channel 2 0~3=ACB1/ACB0/ACB2/ACB2
[3:2]	R/W	AI_Ch1_Sel[1:0] (G)	Analog mux selection for ADC channel 1 0~3=AY1/AY0/AY2/AY2
[1:0]	R/W	AI_Ch0_Sel[1:0] (R)	Analog mux selection for ADC channel 0 0~3=ACR1/ACR0/ACR2/ACR2

4.1.26 Y/Cb/Cr Data Switching Control

Address Offset: P0_19h Default Value: 07h

Bit	Access	Symbol	Description
[7]	R/W	Y_in_Sel_V	Y channel selection for video decoder 1: ADCV is selected
[6]	RO	Reserved	
[5:4]	R/W	CBINSEL	The digitaized CB or B data can be taken from one of 3 ADCs: 00: ADC Ch0 01: ADC Ch1 1X: ADC Ch2
[3:2]	R/W	YINSEL	The digitaized Y or Composite or G data can be taken from one of 3 ADCs: 00: ADC Ch0 01: ADC Ch1 1X: ADC Ch2
[1:0]	R/W	CRINSEL	The digitaized CR or Chroma or R data can be taken from one of 3 ADCs: 00: ADC Ch0 01: ADC Ch1 1X: ADC Ch2

4.1.27 ADC Analog AGC Selection

Address Offset: P0_1Ah Default Value: 42h

Bit	Access	Symbol	Description
[7:6]	R/W	AGC_GAINMD	<table><tr><th>Mode</th><th>Type</th></tr><tr><td>0</td><td>Positive gain</td></tr><tr><td>1</td><td>Positive gain 1x~2x</td></tr><tr><td>2</td><td>Negative gain 1x~2x</td></tr><tr><td>3</td><td>Negative gain</td></tr></table>
[5]	R/W(WO)	AGC_FreeMM	1: release agc when no signal is present
[4]	RO	Reserved	
[3]	R/W	V_AGC_SEL	If 0, refer to ADCVSG (P1_11h): 0: Static gain; 1: Dynamic gain
[2]	R/W	CB_AGC_SEL	If 0, refer to ADCBSG (P0_09h): 0: Static gain; 1: Dynamic gain
[1]	R/W	Y_AGC_SEL	If 0, refer to ADCGSG (P0_08h) 0: Static gain; 1: Dynamic gain
[0]	R/W	CR_AGC_SEL	If 0, refer to ADCRSG (P0_07h) 0: Static gain; 1: Dynamic gain

4.1.28 ADC Analog Pseudo Differential Control

Address Offset: P0_1Bh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	R_diff_en	Enable pseudo differential for R channel
[6]	R/W	G_diff_en	Enable pseudo differential for G channel
[5]	R/W	B_diff_en	Enable pseudo differential for B channel
[4]	R/W	V_diff_en	Enable pseudo differential for V channel
[3:2]	RO	Reserved	
[1]	R/W	entrpy_en	
[0]	R/W	dither_en	

4.1.29 Blank Sync Level

Address Offset: P0_1Ch Default Value: F0h

Bit	Access	Symbol	Description
[7:0]	R/W	BLANK_SL	

4.1.30 ADC Read Back Selection

Address Offset: P0_1Dh Default Value: 00h

Bit	Access	Symbol	Description
[7:1]	RO	Reserved	
[0]	R/W	RBK_SEL	1: Read Max of ADC data 0: Read Min of ADC data or Average of ADC data

4.1.31 ADC Read-back LSB Data

Address Offset: P0_1Eh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	RBK_ADC[7:0]	

4.1.32 ADC Read-back MSB Data

Address Offset: P0_1Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:2]	R	RESERVED	
[1:0]	R	RBK_ADC[9:8]	

4.1.33 ADC Phase Setting Register

Address Offset: P0_20h Default Value: 80h

Bit	Access	Symbol	Description
[7:3]	R/W	ADC_Phase[4:0]	32 phases per clock
[2]	R/W	ADC_Clk_Div2	Clock divided by 2 if set to 1
[1]	R/W	ADC_Clk_Dly	Clock delay if set to 1
[0]	R/W	ADC_Clk_Inv	Clock inverted if set to 1

4.1.34 ADC Detection Register

Address Offset: P0_21h Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO/WO	Done_ATK / En_ATK	When read: get flag of Phases Tracking finish or not When write, to enable Phases Tracking

Bit	Access	Symbol	Description
[6:5]	R/W	ATK_Channel[1:0]	Select which channel to perform ATK: 00: R+G+B 01: R 10: G 11: B
[4:3]	RO	Reserved	
[2]	RO/WO	Done_Exist_ADC / En_Exist_ADC	When read: get flag of Checking ADC HS/VS finish or not When write, to enable Checking ADC HS/VS
[1]	RO	Exist_HSync	HSync input toggle when read 1
[0]	RO	Exist_VSync	HSync input toggle when read 1

4.1.35 ADC_Phase Tracking LSB Register

Address Offset: P0_22h Default Value: -

Bit	Access	Symbol	Description
[7:0]	RO	ATK_Accu[7:0]	Accumulated Phase Tracking Result

4.1.36 ADC Phase Tracking Middle Register

Address Offset: P0_23h Default Value: -

Bit	Access	Symbol	Description
[7:0]	RO	ATK_Accu[15:8]	Accumulated Phase Tracking Result

4.1.37 ADC Phase Tracking MSB Register

Address Offset: P0_24h Default Value: -

Bit	Access	Symbol	Description
[7:0]	RO	ATK_Accu[23:16]	Accumulated Phase Tracking Result

4.1.38 Boundary Control Register

Address Offset: P0_26h Default Value: 04h

Bit	Access	Symbol	Description
[7]	RO/WO	Done_Boundary / En_Boundary	When read: get flag of Boundary Detection finish or not When write, to enable Boundary Detection
[6]	R/W	Boundary_hDE	Check boundary when: 0: in all range 1: in HDE window
[5:3]	R/W	Boundary_Mask_HS_L	Set the do not care range near HSync leading edge
[2:0]	R/W	Boundary_Mask_HS_T	Set the do not care range near HSync trailing edge

4.1.39 Boundary Control Register

Address Offset: P0_27h Default Value: 40h

Bit	Access	Symbol	Description
[7:0]	R/W	Boundary_Threshold	Set the color threshold for boundary detection

4.1.40 Boundary Left LSB Register

Address Offset: P0_28h Default Value: -

Bit	Access	Symbol	Description
[7:0]	RO	Left_Bound[7:0]	Left Boundary Position

4.1.41 Boundary Left MSB Register

Address Offset: P0_29h Default Value: -

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	

Bit	Access	Symbol	Description
[3:0]	RO	Left_Bound[11:8]	Left Boundary Position

4.1.42 Boundary Right LSB Register

Address Offset: P0_2Ah Default Value: -

Bit	Access	Symbol	Description
[7:0]	RO	Right _Bound[7:0]	Right Boundary Position

4.1.43 Boundary Right MSB Register

Address Offset: P0_2Bh Default Value: -

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	RO	Right_Bound[11:8]	Right Boundary Position

4.1.44 Boundary Top LSB Register

Address Offset: P0_2Ch Default Value: -

Bit	Access	Symbol	Description
[7:0]	RO	Top _Bound[7:0]	Top Boundary Position

4.1.45 Boundary Top MSB Register

Address Offset: P0_2Dh Default Value: -

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	RO	Top _Bound[11:8]	Top Boundary Position

4.1.46 Boundary Bottom LSB Register

Address Offset: P0_2Eh Default Value: -

Bit	Access	Symbol	Description
[7:0]	RO	Bottom _Bound[7:0]	Bottom Boundary Position

4.1.47 Boundary Bottom MSB Register

Address Offset: P0_2Fh Default Value: -

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	RO	Bottom _Bound[11:8]	Bottom Boundary Position

4.1.48 Boundary Bottom MSB Register

Address Offset: P0_2Fh Default Value: -

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	RO	Bottom _Bound[11:8]	Bottom Boundary Position

4.1.49 ADC V channel Control Register

Address Offset: P1_10h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	PD_Ch3_ (V)	1: Power up 0: Power down

[6:4]	R/W	V_LPF_Sel[2:0]	Low-pass filter bandwidth selection for ADC3 000 : 200MHz 001 : 175 MHz 010 : 150 MHz 011 : 105 MHz 100 : 60 MHz 101 : 35 MHz 110 : 12 MHz 111 : 6.5MHz
[3]	RO	Reserved	
[2:0]	R/W	V_ClampVolt_Sel[2:0]	Channel V (ADC3) clamp voltage selection

4.1.50 ADC Channel 3 Static Gain

Address Offset: P1_11h Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	ADC_VGAIN	This register can set a fixed gain for ADC channel 3 when static gain control is enabled

4.1.51 ADC Channel 3 Offset

Address Offset: P1_12h Default Value: 80h

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_V_Offset	ADC Channel 3 DC Offset Control
[1:0]	RO	Reserved	

4.1.52 ADC Clamping Control Register

Address Offset: P1_13h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:1]	R/W	AI_Ch3_Sel[1:0] (V)	Analog mux selection for ADC channel 3 0~3=ACR0/AY0/ACB0/ACB0
[0]	R/W	VSCALE	ADC Channel 3 Clamping Mode 0: Clamp to Ground; 1: Clamp to mid-scale

4.1.53 Channel V Offset Tune Register

Address Offset: P1_14h Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6]	R/W	V_Decrease	Channel v decrease (1) or increase (0) by V_Offset_Tune[3:0]
[5:4]	RO	Reserved	
[3:0]	R/W	V_Offset_Tune[3:0]	Channel v offset fine tune

4.1.54 ADC Sync Offset Control Register

Address Offset: P0_40h Default Value: D0h

Bit	Access	Symbol	Description
[7]	R/W	En_HsOffset	Set to 1 for enabling ADC HSync Offset.
[6]	R/W	En_VsOffset	Set to 1 for enabling ADC VSync Offset.
[5]	R/W	En_VsOfs_Evn_P1	Set to 1 for enabling ADC VSync Offset delay 1 line for even field.
[4]	R/W	SOY_Odd_Inv_	Set to 0 for inverting SOY Odd field flag.
[3:2]	RO	Reserved	
[1]	R/W	RGB_PowerDown_	Set to 0 for power down RGB related logic. 1 for enabling RGB path.

Bit	Access	Symbol	Description
[0]	R/W	HS_in_SyncSel	Select the sampling edge of HSync pin. HSi_SyncSel: 0=posedge, 1=negedge

4.1.55 ADC HSync Offset LSB Register

Address Offset: P0_41h Default Value: 02h

Bit	Access	Symbol	Description
[7:0]	R/W	HsOffset[7:0]	Delay ADC HSync by # dots. HsOffset >= 1

4.1.56 ADC HSync Offset MSB Register

Address Offset: P0_42h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	HsOffset[10:8]	Delay ADC HSync by # dots.

4.1.57 ADC VSync Offset LSB Register

Address Offset: P0_43h Default Value: 01h

Bit	Access	Symbol	Description
[7:0]	R/W	VsOffset[7:0]	Delay ADC VSync by # lines. VsOffset >= 1

4.1.58 ADC VSync Offset MSB Register

Address Offset: P0_44h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	VsOffset[10:8]	Delay ADC VSync by # lines.

4.1.59 ADC HSync Offset Pulse Width Register

Address Offset: P0_45h Default Value: 10h

Bit	Access	Symbol	Description
[7:0]	R/W	HsPulseWidth[7:0]	Pulse width of the regenerated ADC HSync (# dots).

4.1.60 ADC VSync Offset Pulse Width Register

Address Offset: P0_46h Default Value: 01h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	VsPulseWidth[3:0]	Pulse width of the regenerated ADC VSync (# lines).

4.1.61 ADC Capture Control Register

Address Offset: P0_47h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	Mask_H_Left	Set to 1 for mask left portion when wrap.
[6]	R/W	Mask_H_Right	Set to 1 for mask right portion when wrap.
[5]	R/W	Mask_V_Top	Set to 1 for mask top portion when wrap.
[4]	R/W	Mask_V_Bottom	Set to 1 for mask bottom portion when wrap.
[3:1]	RO	Reserved	
[0]	R/W	Reserved	Reserved for chip test only

4.1.62 ADC Capture HSize LSB Register

Address Offset: P0_48h Default Value: D0h

Bit	Access	Symbol	Description

Bit	Access	Symbol	Description
[7:0]	WO	ADC_HSize[7:0]	ADC Capture window: Horizontal Size (# dots).

4.1.63 ADC Capture HSize MSB Register

Address Offset: P0_49h Default Value: 02h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	WO	ADC_HSize[10:8]	ADC Capture window: Horizontal Size (# dots).

4.1.64 ADC Capture VSize LSB Register

Address Offset: P0_4Ah Default Value: E0h

Bit	Access	Symbol	Description
[7:0]	WO	ADC_VSize[7:0]	ADC Capture window: Vertical Size (# lines).

4.1.65 ADC Capture VSize MSB Register

Address Offset: P0_4Bh Default Value: 01h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	WO	ADC_VSize[10:8]	ADC Capture window: Vertical Size (# lines).

4.1.66 ADC Capture HSync Back Porch LSB Register

Address Offset: P0_4Ch Default Value: 10h

Bit	Access	Symbol	Description
[7:0]	WO	ADC_HStart[7:0]	ADC Capture window: Horizontal Start Point (# dots).

4.1.67 ADC Capture HSync Back Porch MSB Register

Address Offset: P0_4Dh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	WO	ADC_HStart[10:8]	ADC Capture window: Horizontal Start Point (# dots).

4.1.68 ADC Capture VSync Back Porch LSB Register

Address Offset: P0_4Eh Default Value: 05h

Bit	Access	Symbol	Description
[7:0]	R/W	ADC_VStart[7:0]	ADC Capture window: Vertical Start Point (# linees).

4.1.69 ADC Capture VSync Back Porch MSB Register

Address Offset: P0_4Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	WO	ADC_VStart[10:8]	ADC Capture window: Vertical Start Point (# linees).

Address Offset: P2_9Ch Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	En_frn_hs	Enable free run
[6]	R/W	frn_hs_pol	Polarity of free run hsync
[3:0]	R/W	Reg_frn_htotal[11:8]	

4.2 ITU-656 Decoder Register Set

4.2.1 ITU-656 Decoder HS Delay Register

Address Offset: P1_D0h Default Value: 30h

Bit	Access	Symbol	Description
[7:2]	R/W	Reserved	
[1:0]	R/W	A656_HS_Delay[7:0]	Unit: cycles of half VCLK

4.2.2 ITU-656 Decoder HS Pulse Width Register

Address Offset: P1_D2h Default Value: 10h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:3]	R/W	A656_HS_Width[5:3]	Unit: Cycles of Half VCLK, HS_WIDTH656[2:0] = 000b, [7:6] = 00b
[2:0]	RO	Reserved	

4.2.3 ITU-656 Decoder VS Delay Register

Address Offset: P1_D3h Default Value: 01h

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4:0]	R/W	A656_VS_Delay[4:0]	Unit: HS, other [7:5] all zero

4.2.4 ITU-656 Decoder VS Pulse Width Register

Address Offset: P1_D4h Default Value: 01h

Bit	Access	Symbol	Description
[7]	R/W	VS_in_LineCnt	0: VSync Delay/Width in VCLK count (for those digital video inputs which have no HREF or its codeword during vertical blank) 1: VSync Delay/Width in Line count (for those digital video inputs which keeps sending HREF or its codeword during Vertical Blank)
[6]	R/W	VS_Ex1_Odd	Set to 1 for extra 1 line VSync Offset for Odd field
[5]	R/W	VS_Ex1_Evn	Set to 1 for extra 1 line VSync Offset for Even field
[4:2]	RO	Reserved	
[1:0]	R/W	A656_VS_Width[1:0]	Unit:HS

4.2.5 ITU-656 Decoder HDE Start LSB Register

Address Offset: P1_D5h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	A656_HStart[7:0]	Unit: Pixel

4.2.6 ITU-656 Decoder HDE Start MSB Register

Address Offset: P1_D6h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	A656_HStart[11:8]	Unit: Pixel

4.2.7 ITU-656 Decoder HDE Size LSB Register

Address Offset: P1_D7h Default Value: D0h

Bit	Access	Symbol	Description
[7:0]	R/W	A656_HSize[7:0]	Unit: Pixel, RO (if A656_Size_Det=1); else R/W

4.2.8 ITU-656 Decoder HDE Size MSB Register

Address Offset: P1_D8h Default Value: 02h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	A656_HSize[11:8]	Unit: Pixel, RO (if A656_Size_Det=1) ; else R/W

4.2.9 ITU-656 Decoder Odd Field VDE Start Register

Address Offset: P1_D9h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	A656_OVStart[7:0]	Odd Filed VDE Start, Unit: HS

4.2.10 ITU-656 Decoder Odd/Even Field VDE Start Register

Address Offset: P1_DAh Default Value: 10h

Bit	Access	Symbol	Description
[7]	R/W	A656_EVStart_P1	Even Filed VDE Start 1: EVSTART656=OVSTART + 1 0: EVSTART656=OVSTART
[6]	R/W	En_RampSmooth	set to 1 for enabling hardware smooth operation
[5:4]	R/W	RampGap[1:0]	Allow to smooth step when the gap between steps is under value 4/8/12/16 (corresponding to setting value of 0/1/2/3)
[3]	R/W	RampSmooth565	0: 666, 1:565
[2:0]	RO	Reserved	

4.2.11 ITU-656 Decoder VDE Size LSB Register

Address Offset: P1_DBh Default Value: F0h

Bit	Access	Symbol	Description
[7:0]	R/W	A656_VSize[7:0]	Unit: HS, RO (if A656_Size_Det=1) ; else R/W

4.2.12 ITU-656 Decoder VDE Size MSB Register

Address Offset: P1_DCh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	A656_VSize[10:8]	Unit: HS, RO (if A656_Size_Det=1) ; else R/W

4.2.13 ITU-656 Decoder Swap/Endian Control Register

Address Offset: P1_DDh Default Value: 00h

Bit	Access	Symbol	Description

[7:6]	RO	Reserved	
[5:3]	R/W	RGB_Swap[2:0]	RGB Channel Swapping: 000: RGB, 001: RBG, 010: GRB, 011: GRB, 1X0: BRG, 1X1: BGR; Note: RGB565 only support RGB/BGR
[2]	R/W	C_Sel	ITU601 16 bits chroma selection 0: LSB 8-bit of 16 bits to be chroma 1: MSB 8-bit of 16 bits to be chroma
[1]	R/W	Y_Sel	ITU601 16 bits luma selection 0: MSB 8-bit of 16 bits to be luma 1: LSB 8-bit of 16 bits to be luma
0]	R/W	En_BigEndian	Reverse input data [7:0] to [0:7] 0: Non-Inverted, Little Endian. 1: Inverted, Big Endian. Note: RGB565/RGB666 not support En_BigEndian

4.2.14 ITU-656 Decoder VCLK Tuning Register

Address Offset: P1_DEh Default Value: 02h

Bit	Access	Symbol	Description
[7]	R/W	One_DE_Only	
[6]	RO	Reserved	
[5]	R/W	LODD_Inv	Set to 1 for invert LODD/LVSYNC pin
[4]	R/W	LODD_is_VS	Set to 1 if LODD pin acts as VSYNC input
[3]	R/W	LHREF_Inv	to 1 for invert LHREF/LHSYNC pin
[2]	R/W	Lfield_in_HREF	Set to 1 for enabling extract Odd flag from LHREF pin
[1]	R/W	VCLK_Inv	VCLK skew: invert
[0]	R/W	VCLK_Dly	VCLK skew: delay

4.2.15 ITU-656 Decoder Format Control Register

Address Offset: P1_DFh Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6]	R/W	A656_OddF_Inv	Filed flag indicator 0: 1st field =0, 2nd field=1 1: 1st filed =1, 2nd field=0
[5]	R/W	A656_ReSync_OddF	Set to 1 for re-synchronizing Odd Flag
[4]	R/W	RGB_for_HDTV	Option different color space convert coefficient set
[3]	R/W	A656_V_Align	Chroma_V pixel alignment
[2]	R/W	A656_UV_Intrplt	Interpolate UV pixel values when 422 => 444 converting
[1]	R/W	A656_Size_Det	Read back Size of HDE and VDE 0:Disable 1:Enable
[0]	R/W	A656_DetUpdate_	Size detect result update allow, depends on: 0:Update current detection 1:Keep previous detection

4.3 Input Timing Register Set

4.3.1 De-Interlace Process & Vertical Shadow Control Register

Address Offset: P0_30h Default Value: 02h

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6]	R/W	En_RGB_Proc	
[5]	R/W	VS_time_ch_Sel_X	1:Vsync timing change determined by 8*# of XCLK 0:Vsync timing change determined by # of hsync (default) # can be assigned at Reg 0x3A
[4]	R/W	INT_EDGE	Interrupt polarity 1: positive 0: negative (default)
[3]	R/W	LBi_Size_Prog	This bit control capture size for Scaler. 1: Hsize and Vsize are assigned by 54h ~57h 0: sizes assigned by input sources. (default)
[2]	R/W	ENQKHS	Reserved for chip teset only, set to 0 for normal operation
[1]	R/W	ITLCPRO	Set 1 for interlaced video (default) Set 0 for non-interlaced video
[0]	R/W	ADC_Odd_in_HsVs	Set to 1 for enabling detecting Odd flag from HS/VS pins

4.3.2 Source Select Register

Address Offset: P0_31h Default Value: 04h

Bit	Access	Symbol	Description
[7]	RO	Interlace_Flag	Indicates incoming video signal is interlaced if get 1
[6:4]	R/W	VIP_Sel[2:0]	Select the digital input source (VIP: Video Input): 000: A656, Alternative ITU-656 001: ITU-656 010: L601_8bits 011: L601_16bits 100: Reserved 101: RGB565 110: RGB666 111: RGB888
[3:2]	R/W	InSource_Sel[1:0]	Select the input source: 00: Digital VIP input 01: select VD input (CVBS, S-Video, YPbPr) 10: Select ADC RGB, SOY(YPbPr) 11: Reserved
[1]	R/W	A656_601_8b	When VIP_Sel[2:0] = 3'b000 (A656) 0: A656 1: A601 8bits
[0]	RO	VBI_Field	Current VBI field information

4.3.3 1ms Timer LSB Register

Address Offset: P0_35h Default Value: BCh

Bit	Access	Symbol	Description
[7:0]	R/W	TM_1MS_L [7:0]	Lower byte of the number of XCLK's in half 1ms.

4.3.4 1ms Timer MSB Register

Address Offset: P0_36h Default Value: 34h

Bit	Access	Symbol	Description
[7:0]	R/W	TM_1MS_H [15:8]	Higher byte of the number of XCLK's in half 1ms.

4.3.5 VSYNC Missing Counter Register

Address Offset: P0_37h Default Value: 40h

Bit	Access	Symbol	Description
[7:0]	R/W	V_MISS_CNT[7:0]	When no VSync toggle during this value * 1ms, trigger interrupt

4.3.6 HSYNC Missing Counter LSB Register

Address Offset: P0_38h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	H_MISS_CNT_L[7:0]	When no HSync toggle during this value * XCLK, trigger interrupt

4.3.7 HSYNC Missing Counter MSB Register

Address Offset: P0_39h Default Value: 10h

Bit	Access	Symbol	Description
[7:0]	R/W	H_MISS_CNT_L[15:8]	

4.3.8 VSYNC Delta Difference Result Register

Address Offset: P0_3Ah Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	VSYNC_DLT[7:0]	When VSync period varies more than this value, trigger interrupt

4.3.9 HSYNC Delta Difference Result Register

Address Offset: P0_3Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	HSYNC_DLT[7:0]	When HSync period varies more than this value, trigger interrupt

4.3.10 VD/656 Left Border Crop Register

Address Offset: P0_3Ch Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	CROP_LEFTB	Remove noisy pixels appearing on left border. 1LSB =1 pixel

4.3.11 VD/656 VSync Offset Register

Address Offset: P0_3Dh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	VD_VsOfs_Mode	VD/656 VSync Offset mode: 0: Crop Top Border 1: VSync Offset, delay lines
[6]	R/W	En_VD_VsOfsEvn_P1	
[5:0]	R/W	VD_VsOffset	Remove noisy pixels appearing on top border or re-shape VSync 1LSB =1 line, value 0 means disable.

4.3.12 VD/656 Left Border Crop Register

Address Offset: P0_3Eh Default Value: 10h

Bit	Access	Symbol	Description
[7]	R/W	En_VD_VsOfs_P1	Enable VSync Offset add 1 line for even or odd field on VD path
[6]	R/W	VD_VsOfs_on_Odd	Set to 1 for selecting VD VSync Offset delay 1 line on Odd field; Set to 0 for Even field. This bit works only when En_VD_VsOfs_P1=1.

[5:0]	R/W	VD_VsBP	VD/656 VSync Back Proch (# lines)

4.3.13 Input Sync Signal Detection Register

Address Offset: P0_3Fh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	HSTLSPVS	1:use trailing edge of hsync to sample 0:use leading edge of hsync to sample
[6]	R/W	AUTOVSD6	When the edges of vsync and hsync are too close, input detection circuit can delay vsync 6 cycle of XCLK to avoid unstable detection 1:Automatically delay 6 cycles of XCLK if CFSEEDGE is true. 0:Dealy 6 cycles of XCLK if FCVSD6 is true
[5]	R/W	FCVSD6	AUTOVSD6 FCSVSD6T 1 x Automatically delay VSync 6 XCLK if CFSEEDGE is true 0 1 Force to delay VSync 6 XCLK 0 0 No Vsync Dealy
[4]	RO	HsVs_Edge_Confuse	VS and HS edges are too close.
[3]	RO	HS_Polarity	Detected HSync polarity (for Analog RGB raw input)
[2]	RO	VS_Polarity	Detected VSync polarity (for Analog RGB raw input)
[1]	R/W	VsHs_Sync_Edge	
[0]	R/W	VsHs_Sync_En	

4.3.14 VSYNC Timing Measure Register

Address Offset: P0_50h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	FreeRun_Sel_cd	1: Use cvd signal to enter FreeRun; 0: ShortVS
[6]	R/W	HsPeriod_dclki	Register 0x5c and 0x5d can be HS pulse width or HSync period 1: Period in # of pixel clock. 0: HSync pulse width in # of pixel clock.
[5]	RO	DONE_FRMXCLKCNT	When EN_FRAMEXCLKCNT is enabled, a whole frame time can be obtained through XCLK counting. See registers 0x51, 0x52 and 0x53. After this bit read back as 1, then clear EN_FRAMEXCLKCNT first before reading 0x51~0x53 values.
[4]	R/W	EN_FRAMEXCLKCNT	When input VSync changes, enable this bit to start measurement on VSync using XCLK.
[3]	R/W	Reserved	
[2]	RO	In_ShortVS_FreeRun	Status indicator of whether it is in Free-run which caused by short VS
[1]	R/W	VsPeriod_Rd_SetShort	Register 0x5A and 0x5B read back from: 1: Programmed threshold for VS period 0: VSync period in # of lines
[0]	R/W	ShortVS_Check_En	Set to 1for enabling monitoring VS period

4.3.15 VSYNC Period Measurement L Register

Address Offset: P0_51h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	FRMXCLK_SUM[7:0]	VSync Period, count by XCLK

4.3.16 VSYNC Period Measurement M Register

Address Offset: P0_52h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	FRMXCLK_SUM[15:8]	

4.3.17 VSYNC Period Measurement H Register

Address Offset: P0_53h Default Value: 00h

Bit	Access	Symbol	Description
[4:0]	RO	FRMXCLK_SUM[20:16]	

4.3.18 Input HSize LSB Register

Address Offset: P0_54h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO or R/W	Inp_HSize[7:0]	This register is: Read Only, when P0_30h<3>=0, showing input image HSize Read/Write, when P0_30h<3>=1, over-write HSize.

4.3.19 Input HSize MSB Register

Address Offset: P0_55h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	Reserved	
[3:0]	RO or R/W	Inp_HSize[11:8]	

4.3.20 Input VSize LSB Register

Address Offset: P0_56h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO or R/W	Inp_VSize[7:0]	This register is: Read Only, when P0_30h<3>=0, showing input image VSize Read/Write, when P0_30h<3>=1, over-write VSize.

4.3.21 Input VSize MSB Register

Address Offset: P0_57h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	Reserved	
[3:0]	RO or R/W	Inp_VSize[11:8]	

4.3.22 HSync Period LSB Register

Address Offset: P0_58h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	Hs_Period[7:0]	32x HSync period, counted by XCLK

4.3.23 HSync Period MSB Register

Address Offset: P0_59h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	Hs_Period[15:8]	32x HSync period, counted by XCLK

4.3.24 VSync Period LSB Register

Address Offset: P0_5Ah Default Value: FFh

Bit	Access	Symbol	Description
[7:0]	RO or R/W	VS_Period[7:0] / SetShortVs_Period[7:0]	This register is: RO, when P0_50h<2>=0, showing input VSync period (by lines) R/W, when P0_50h<2>=1, programmed ShortVS threshold

4.3.25 VSync Period MSB Register

Address Offset: P0_5Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	RO or R/W	Vs_Period[10:8]	

4.3.26 HSync Pulse Width LSB Register

Address Offset: P0_5Ch Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	HS_Period[7:0] / HS_Width[7:0]	HSYNC pulse width or period counted by dot clock See HSPMD (P0_50h<6>) for detail.

4.3.27 HSync Pulse Width MSB Register

Address Offset: P0_5Dh Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	RO	HS_Width[11:8]	HSYNC pulse width or period counted by dot clock

4.3.28 VSync Pulse Width LSB Register

Address Offset: P0_5Eh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	Vs_Width[7:0]	VSYNC pulse width counted by input HSYNC

4.3.29 VSync Pulse Width MSB Register

Address Offset: P0_5Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	RO	Vs_Width[10:8]	VSYNC pulse width counted by input HSYNC

4.4 Scaling Register Set

4.4.1 Scaling General Control Register

Address Offset: P0_70h Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5]	R/W	Inv_VideoF	Reverse input odd field control for intra-field scaling, only take action when ITLCPRO set to 1
[4]	R/W	Dclki_is_Faster	Software need to turn this bit on when the freq of input pixel clock is higher than output pixel clock
[3]	R/W	V_Half_En	Set to 1 if vertical downscale less than 1/2
[2]	R/W	LB_Clk_sel	Set to 1 to use pclk_pll (DPLL) to be LB_Clk, to avoid frequency of dclki and dclko_2x too close
[1]	RO	Reserved	
[0]	WO	Coef_Pointer_Reset	Write 1 to reset pointer, must be performed before programming scaling coefficients

4.4.2 Scaling Coefficient Data Port Register

Address Offset: P0_71h Default Value: 00h

Bit	Access	Symbol	Description

[7:0]	R/W	Coef_Data_Port	Coefficient Data Port, fill all coefficients of one set in one time

4.4.3 Horizontal Scale Step Register

Address Offset: P0_72h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	H_Scale_Step[7:0]	Horizontal scaling ratio

Address Offset: P0_73h Default Value: 20h

Bit	Access	Symbol	Description
[7:0]	R/W	H_Scale_Step[15:8]	Horizontal scaling ratio

4.4.4 Vertical Scale Step Register

Address Offset: P0_74h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	V_Scale_Step[7:0]	Vertical scaling ratio

Address Offset: P0_75h Default Value: 20h

Bit	Access	Symbol	Description
[7:0]	R/W	V_Scale_Step[15:8]	Vertical scaling ratio

4.4.5 Horizontal Aspect Ratio LSB Register

Address Offset: P0_76h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	H_Aspect[7:0]	Horizontal aspect ratio

4.4.6 Horizontal Aspect Ratio MSB Register

Address Offset: P0_77h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	H_Aspect_En	Horizontal aspect ratio enable
[6]	R/W	H_Center_Enlarge	Horizontalaspect adjusting effect: 0: center portion shrink 1: center portion enlarge
[5]	R/W	H_Aspect_16_Seg	Horizontal aspect with 16 segments 0: 8 segments 1:16 segments
[4]	RO	Reserved	
[3:0]	R/W	H_Aspect[11:8]	

4.4.7 Low Pass Filter Register

Address Offset: P0_78h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	En_Half_Input	Enable low pass filter
[6]	RO	Reserved	
[5:4]	R/W	LP_Average[1:0]	Shift average level
[3]	R/W	LP_Boundary_Dup	Duplicate the first dot or not 0: blank shift 1: duplicate first/last dot
[2]	RO	Reserved	
[1:0]	R/W	LP_ShiftDot[1:0]	Shift dot count

4.4.8 High Boost Filter Register

Address Offset: P0_79h Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	R/W	HighBoost_Mode[1:0]	Delta >= values * 8
[5:4]	R/W	HighBoost_Coef_C[1:0]	Chroma coef. For High Boost scaling
[3:0]	R/W	HighBoost_Coef_Y[3:0]	Luma coef. For High Boost scaling

Address Offset: P0_7Ah Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	HiBst_Corner_En	
[6]	R/W	HiBst_MaskBlack	
[5:0]	RO	Reserved	

4.4.9 Motion Register

Address Offset: P0_7Ch Default Value: 08h

Bit	Access	Symbol	Description
[7]	R/W	Motion_En	1: enable motion detection
[6:4]	RO	Reserved	
[3:2]	R/W	H_Continue[1:0]	Qualified thin line: 0~3: 4/8/12/16 dots
[1:0]	R/W	Init_VPhase_Sel[1:0]	2D DI shift option: 00b: 1/2; 01b:1/4; 10b:1/8; 11b:0 lines

4.4.10 Frame Color in Scaler Register

Address Offset: P0_7Dh Default Value: 10h

Bit	Access	Symbol	Description
[7:0]	R/W	Scale_Frame_Y[7:0]	Background(Frame) Y color of Scaler

Address Offset: P0_7Eh Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	Scale_Frame_U[7:0]	Background(Frame) U color of Scaler

Address Offset: P0_7Fh Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	Scale_Frame_V[7:0]	Background(Frame) V color of Scaler

4.5 LVDS TX Register Set

4.5.1 LVDS TX Power Down Control Register

Address Offset: P0_CFh Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	R/W	LVDS_Swing[1:0]	Output swing control bit 00: 200mV, 01: 250mV, 10:350mV, 11:450mV
[5]	R/W	LVDS_Inv	LVDS data polarity
[4]	R/W	LVDS_DE6	Set the value of undefined dummy bit
[3]	RO	Reserved	
[2]	R/W	LVDS_TD_PwnDn_	0:6-bit LVDS output; 1:8-bit LVDS output
[1]	R/W	LVDS_T1_PwnDn_	Set 1 to Power on LVDS channel 1

[0]	R/W	LVDS_T0_PwnDn_	Set 1 to Power on LVDS channel 0

4.5.2 LVDS TX Port0 Channel A/B Delay Control Register

Address Offset: P0_D0h Default Value: 44h

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:4]	R/W	LTxB0_dlyctl[2:0]	Delay control for port0 channel B
[3]	RO	Reserved	
[2:0]	R/W	LTxA0_dlyctl[2:0]	Delay control for port0 channel A

4.5.3 LVDS TX Port0 Channel A/B Delay Control Register

Address Offset: P0_D1h Default Value: 44h

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:4]	R/W	LTxD0_dlyctl[2:0]	Delay control for port0 channel D
[3]	RO	Reserved	
[2:0]	R/W	LTxC0_dlyctl[2:0]	Delay control for port0 channel C

4.5.4 LVDS TX Port0 Channel CLK Delay Control Register

Address Offset: P0_D2h Default Value: 04h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	LTxCK0_dlyctl[2:0]	Delay control for port0 channel C

4.5.5 LVDS TX Port1 Channel A/B Delay Control Register

Address Offset: P0_D3h Default Value: 44h

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:4]	R/W	LTxB1_dlyctl[2:0]	Delay control for port1 channel B
[3]	RO	Reserved	
[2:0]	R/W	LTxA1_dlyctl[2:0]	Delay control for port1 channel A

4.5.6 LVDS TX Port1 Channel C/D Delay Control Register

Address Offset: P0_D4h Default Value: 44h

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:4]	R/W	LTxD1_dlyctl[2:0]	Delay control for port1 channel D
[3]	RO	Reserved	
[2:0]	R/W	LTxC1_dlyctl[2:0]	Delay control for port1 channel C

4.5.7 LVDS TX Port1 Channel C/D CLK Control Register

Address Offset: P0_D5h Default Value: 04h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	LTxCK1_dlyctl[2:0]	Delay control for port1 channel CLK

4.5.8 LVDS TX Testing Register

Address Offset: P6_50h Default Value: 00h

Bit	Access	Symbol	Description
[7:1]	RO	Reserved	

[0]	R/W	EnLTx_Pat	

Address Offset: P6_51h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	LTx0_PatANeg	
[6:0]	R/W	LTx0_PatA	

Address Offset: P6_52h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	LTx0_PatBNeg	
[6:0]	R/W	LTx0_PatB	

Address Offset: P6_53h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	LTx0_PatCNeg	
[6:0]	R/W	LTx0_PatC	

Address Offset: P6_54h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	LTx0_PatDNeg	
[6:0]	R/W	LTx0_PatD	

4.6 TCON Register Set

4.6.1 Timing Controller (TCON) Control Register

Address Offset: P1_20h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	GScanInt	Enable interlaced scanning Mode: Type 0: Processive 1: Interlacing
[6]	R/W	DDR_GDRV	Enable DDR gate driver Mode: Type 0: 1 line/GCLK 1: 2 lines/GLK
[5]	R/W	GTOE	Enable gate driver output Mode: Type 0: Shutdown output 1: Enable
[4]	R/W	DbScan_Edge	Clock edge of STV When DbScan_STV_1p is enabled, DbScan_Edge can control STV alignment with the falling edge o rising edge of GCLK Mode: Type 0: Falling edge of GCLK 1: Rising edge of GCLK

[3]	R/W	DbScan_STV_1p5	STV 1.5 lines wide Mode: Type 0: 1 line wide 1: 1.5 lines wide
[2]	R/W	DbScan_En	Gate driver Scanning control Mode: Type 0: 1 GCLK/line 1: 2 GCLKs/line
[1]	R/W	Q1HPL	Q1H polarity Mode: Type 0: Negative 1: Positive
[0]	R/W	PNINV	Enable line-inverted function.

4.6.2 Timing Protocol & Polarity Control Register

Address Offset: P1_21h Default Value: FFh

Bit	Access	Symbol	Description
[7]	RW	DRVRSTPL	This bit may control Source Drive Reset polarity When P0_E1h<7:6> is not 11b, pin STV2 becomes the rese of source driver
[6]	R/W	GTOEPL	This bit may control GOE polarity Mode: Type 0: Low-active 1: Highactive
[5]	R/W	STVPL	Row Driver start pulse polarity Mode: Type 0: Negative 1: Positive
[4]	R/W	CLKVPL	Data Inversion Polarity Mode: Type 0: Negative 1: Positive
[3]	R/W	FLD1PL	Video Field Polarity Mode: Type 0: Inverted field flag 1: Non-inverted field flag
[2]	R/W	POLPL	Column Driver POL inversion polarity Mode: Type 0: Negative 1: Positive
[1]	R/W	LPPL	Column Driver Latch Pulse polarity Mode: Type 0: Negative 1: Positive
[0]	R/W	STHPL	Column Driver Start Pulse polarity Mode: Type 0: Negative 1: Positive

4.6.3 Column Driver Latch Pulse Placement Register

Address Offset: P1_22h Default Value: 03h

Bit	Access	Symbol	Description
[7:0]	R/W	CDLPPLM[7:0]	This register allows LP to place between 2 DE pulses counted by LLCK dot clock The reference point is the rising edge of DE

Address Offset: P1_23h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	CDLPPLM[10:8]	This register allows LP to place between 2 DE pulses counted by LLCK dot clock The reference point is the rising edge of DE

4.6.4 Column Driver Latch Pulse Duration Control Register

Address Offset: P1_24h Default Value: 21h

Bit	Access	Symbol	Description
[7:0]	R/W	CDLPDU[7:0]	This register allows LP duration programmable counted by LLCK dot clock

4.6.5 POL Placement Register

Address Offset: P1_25h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	POLPLM[7:0]	The reference point is the leading edge of DE

Address Offset: P1_26h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	POLPLM[10:8]	The reference point is the leading edge of DE

4.6.6 CLKV Placement Register

Address Offset: P1_27h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	CLKVPLM[7:0]	The reference point is the leading edge of DE

Address Offset: P1_28h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	CLKVPLM[10:8]	The reference point is the leading edge of DE

4.6.7 CLKV Duration Register

Address Offset: P1_29h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	CLKVDU[7:0]	The reference point is leading edge of DE

Address Offset: P1_2Ah Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	CLKVDU[10:8]	The reference point is the leading edge of DE

4.6.8 STH Position Placement Register

Address Offset: P1_2Bh Default Value: 01h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	STHPLM[2:0]	STH timing related to HDE. -2 to 5 CLKHs

4.6.9 Gate Driver Pre-Driving Register

Address Offset: P1_2Dh Default Value: 03h

Bit	Access	Symbol	Description
[7:0]	R/W	GTVLTC	STV2 Duration

4.6.10 Double Scan CLKV Placement Register

Address Offset: P1_2Eh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	DbS_CLKVPLM[7:0]	

Address Offset: P1_2Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	DbS_CLKVPLM[10:8]	

4.6.11 Row Driver Configuration Register

Address Offset: P1_30h Default Value: 00h

Bit	Access	Symbol	Description
[7:1]	RO	Reserved	
[0]	R/W	ESTVOFFSET	Enable STV Offset

4.6.12 Gate Driver OE Pulse Position Placement Register

Address Offset: P1_31h Default Value: 0Fh

Bit	Access	Symbol	Description
[7:0]	R/W	GOEPL[7:0]	

Address Offset: P1_32h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	GOEPL[10:8]	

4.6.13 Gate Driver OE Pulse Duration Register

Address Offset: P1_33h Default Value: 0Fh

Bit	Access	Symbol	Description
[7:0]	R/W	GOEDU[7:0]	

Address Offset: P1_34h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	GOEDU[10:8]	

4.6.14 STV Offset Register

Address Offset: P1_35h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	STVOFF[7:0]	

4.7 I-Cache Register Set

4.7.1 Offset[23:0] of 1st 16KB range

Address Offset: P3_A0h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Bank0_Offset	Offset[7:0] of 1st 16KB range

4.7.2

Address Offset: P3_A1h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Bank0_Offset	Offset[15:8] of 1st 16KB range

4.7.3

Address Offset: P3_A2h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Bank0_Offset	Offset[23:16] of 1st 16KB range

4.7.4 Offset[23:0] of 2nd 16KB range

Address Offset: P3_A3h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Bank0_Offset	Offset[7:0] of 2nd 16KB range

4.7.5

Address Offset: P3_A4h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Bank0_Offset	Offset[15:8] of 2nd 16KB range

4.7.6

Address Offset: P3_A5h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Bank0_Offset	Offset[23:16] of 2nd 16KB range

4.7.7 Offset[23:0] of 3rd 16KB range

Address Offset: P3_A6h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Bank0_Offset	Offset[7:0] of 3rd 16KB range

4.7.8

Address Offset: P3_A7h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Bank0_Offset	Offset[15:8] of 3rd 16KB range

4.7.9

Address Offset: P3_A8h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Bank0_Offset	Offset[23:16] of 3rd 16KB range

4.7.10 Offset[23:0] of 4th 16KB range

Address Offset: P3_A9h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Bank0_Offset	Offset[7:0] of 4th 16KB range

4.7.11

Address Offset: P3_AAh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Bank0_Offset	Offset[15:8] of 4th 16KB range

4.7.12

Address Offset: P3_ABh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Bank0_Offset	Offset[23:16] of 4th 16KB range

4.7.13

Address Offset: P3_ACh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	1'b0	Exec_Done
[6]	R/W	Exec_Pass	Execution pass for simulation purpose
[5:0]	RO	Reserved	

4.7.14 Instruction count [31:0] for statistics

Address Offset: P3_B0h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	nst_Cnt	Instruction count [7:0] for statistics

4.7.15

Address Offset: P3_B1h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	nst_Cnt	Instruction count [15:8] for statistics

4.7.16

Address Offset: P3_B2h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	nst_Cnt	Instruction count [23:16] for statistics

4.7.17

Address Offset: P3_B3h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	nst_Cnt	Instruction count [31:24] for statistics

4.7.18 Instruction miss count [31:0] for statistics

Address Offset: P3_B4h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	nst_Miss_Cnt	Instruction miss count [31:0] for statistics

4.7.19

Address Offset: P3_B5h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	nst_Miss_Cnt	Instruction miss count [31:0] for statistics

4.7.20

Address Offset: P3_B6h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	nst_Miss_Cnt	Instruction miss count [31:0] for statistics

4.7.21

Address Offset: P3_B7h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	nst_Miss_Cnt	Instruction miss count [31:0] for statistics

4.7.22

Address Offset: P3_B8h Default Value: 00h

Bit	Access	Symbol	Description
[7]	WO	Cpature_Statistics	Write 1 to capture statistics into registers
[6]	WO	Reset_Statistics	Write 1 to reset statistics
[5:0]	RO	Rserved	

4.8 OSD Register Set

4.8.1 OSD Configuration Index Port Register

Address Offset: P0_A8h Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	WO	OSD_CFG_INDEX	OSD Configuration Address Port

4.8.2 OSD Configuration Data Port Register

Address Offset: P0_A9h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	OSD_CFG_DATA	OSD Configuration Data Port

4.8.3 OSD RAM Address Port Register

Address Offset: P0_AAh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	WO	OSD_RAM_A	OSD RAM Address Port, LSB [7:0] firs, then MSB[15:8]
[7:3]	RO	Reserved	
[2]	RO	Grab_Ready	Triggered OSD RAM 16 bytes data is ready for reading out
[1]	RO	OSD_RAM_Ready	OSD RAM is ready for next programming
[0]	RO	OSD_Cfg_Ready	OSD configuration is ready for next programming

4.8.4 OSD RAM Data Port Register

Address Offset: P0_ABh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	WO	OSD_RAM_D	OSD RAM Data Port
[7:0]	RO	OSD_RAM_D/ TrigRd_Data	NonTrigRd_Mode (OSD_48h<3>) =1, OSD RAM Data Port NonTrigRd_Mode (OSD_48h<3>) =0 OSD RAM 16 bytes Data Port

4.8.5 OSD2 Configuration Register

4.8.5.1 OSD2 Enable/Blinking Register

Address Offset: OSD2_00h Default Value: 0Ah

Bit	Access	Symbol	Description
[7]	R/W	OSD2_En	Set to 1 for globally enabling OSD2 function.
[6]	R/W	Color_1_Half	Set to 1 for allowing shadow effect when color value is 1
[5:4]	R/W	CRAM_ByteAccess[1:0]	Byte Access mode when programming character of menu: 0Xb: Word access (LSB first, then MSB byte) 10b: LSB only (not affect font index >= 256) 11b: MSB only (character BG/FG colors, Blinking, and Index bit 8)
[3:2]	R/W	BlinkFreq[1:0]	Blinking Frequency Select (internal 4x BCLK for Blinking State Machine). Set 00b for Refresh Rate /16; 01b for 1/32; 10b for 1/64; 11b for 1/128.

[1:0]	R/W	BlinkDuty[1:0]	For adjusting the blinking duty cycle, Set: 00b for Global Blink Off, i.e., 0% Background, 100% OSD2. 01b for 25% Background, 75% OSD2. 10b for 50% Background, 50% OSD2. 11b for 75% Background, 25% OSD2.

4.8.5.2 OSD2 Font Size Register

Address Offset: OSD2_01h Default Value: 12h

Bit	Access	Symbol	Description
[7]	R/W	vDE_from_VS	Shift OSD1 more up
[6]	R/W	hDE_from_HS	Shift OSD1 more left
[5]	R/W	FontW16	Set Font Width: 0b: Font Width = 12 1b: Font Width = 16
[4:0]	R/W	FontHeight[4:0]	Font Height, valid value between 1 and 24

4.8.5.3 OSD2 Char2BP Font Index Base Register

Address Offset: OSD2_02h Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	Font_Index_2BP[8:1]	Defines the Char2BP font index base (offset). When character index small than this value*2 will be decoded as Char1BP (mono char). And if the character index greater than or equal to this value*2 will be decoded as Char2BP (<= Font_Index_4BP * 2).

4.8.5.4 OSD2 Char4BP Font Index Base Register

Address Offset: OSD2_03h Default Value: C0h

Bit	Access	Symbol	Description
[7:0]	R/W	Font_Index_4BP[8:1]	Defines the Char4BP font index base (offset). When character index small than this value*2 will be decoded as Char1BP (mono char) or Char2BP; else, Char4BP.

4.8.5.5 OSD2 Char2BP Font Memory Base Address LSB Register

Address Offset: OSD2_04h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Font_BaseA_2BP[7:0]	Defines the Char2BP font in memory, start with this base address (offset).

4.8.5.6 OSD2 Char2BP Font Memory Base Address MSB Register

Address Offset: OSD2_05h Default Value: 0Ch

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	Font_BaseA_2BP[13:8]	Defines the Char2BP font in memory, start with this base address (offset).

4.8.5.7 OSD2 Char4BP Font Memory Base Address LSB Register

Address Offset: OSD2_06h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Font_BaseA_4BP[7:0]	Defines the Char4BP font in memory, start with this base address (offset).

4.8.5.8 OSD2 Char4BP Font Memory Base Address MSB Register

Address Offset: OSD2_07h Default Value: 0Fh

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	Font_BaseA_4BP[13:8]	Defines the Char4BP font in memory, start with this base address (offset).

4.8.5.9 OSD2 LUT Address Register

Address Offset: OSD2_08h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	WO	LUT_A[8:1]	Assign access pointer of Color LUT. When assigning, LUT_A[0] always = 0. LUT[0..255] are main color LUT (16-bits); LUT[256..271] are Char2BP remap LUT (24-bits); LUT[272..273]are BMP remap LUT (24-bits).

4.8.5.10 OSD2 LUT Data Port Register

Address Offset: OSD2_09h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	WO	LUT_D[7:0]	Data written to this port will overwrite OSD2 LUT.

4.8.5.11 OSD2 Window Shadow Width/Height Register

Address Offset: OSD2_0Ah Default Value: 46h

Bit	Access	Symbol	Description
[7:4]	R/W	Wx_ShadowWidth[3:0]	Defines the shadow width (count in 2 dots).
[3:0]	R/W	Wx_ShadowHeight[3:0]	Defines the shadow height (count in 2 lines).

4.8.5.12 OSD2 Global Alpha-Blending Control Register

Address Offset: OSD2_0Bh Default Value: 1Ah

Bit	Access	Symbol	Description
[7]	R/W	Global_aB_Control	Set to 1 for all the alpha-blending behavior of Menu-1, Menu-2 and BMP are control by this register; Set to 0 for separate controls.
[6]	R/W	aB_via_RGBA	1: Alpha-Blending control from the “A” byte iin main RGBA8888 LUT 0: Alpha-Blending control from legacy settings.
[5:4]	R/W	Global_FG_aB_Mode[1:0]	Defines global alpha-blending for foreground when BG already alpha-Blended: 00b: All FG need alpha-Blended if BG is alpha-Blended; 01b: All FG no need alpha-Blended; 10b: All FG no need alpha-Blended, except their color is LUT[1]; 11b: All FG no need alpha-Blended, except their color is LUT[1..3];
[3:0]	R/W	Global_aB_SourcePercen [3:0]	Defines the percentage of source image/video for mixed with OSD2 menu.

4.8.5.13 OSD2 Char1BP Color High bits Register

Address Offset: OSD2_0Ch Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	FGC_1BP_Color[7:4]	Defines the Char1BP FG color [7:4]

4.8.5.14 OSD2 FontROM Index Base Register

Address Offset: OSD2_0Dh Default Value: 40h

Bit	Access	Symbol	Description
[7:0]	R/W	FontROM_IndexBase [8:1]	For font index value less than this value is mono character (Char1BP) RAM font segment; For font index >= this value but less than Char2BP_IndexBase is mono character (Char1BP) ROM font segment.

4.8.5.15 OSD2 LUT Control Register

Address Offset: OSD2_0Eh Default Value: 03h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3]	R/W	Color_0_Half	1: Color 0 treat as half dark color likes in shadow effect, and won't refer to LUT[0] 0: Color 0 refer LUT[0]
[2]	R/W	LUT_WrapIn256	1: LUT only use lower 256 entries 0: LUT wrap over 256 (100h~11Fh) when set to lower 32 entries for non-Char8BP characters
[1]	R/W	ChromaKey_100h	1: Change to transparent when dot color is LUT's 100h 0: No replace LUT color when LUT's input color index is 100h
[0]	R/W	ChromaKey_000h	1: Change to transparent when dot color is LUT's 000h 0: No replace LUT color when LUT's input color index is 000h

4.8.5.16 OSD2 Revision ID Register

Address Offset: OSD2_0Fh Default Value: C0h

Bit	Access	Symbol	Description
[7:0]	RO	Revision_ID[7:0]	

4.8.5.17 OSD2 Menu-1 Enable Register

Address Offset: OSD2_10h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	M1_En	Set to 1 enable Menu-1 thread to display
[6:0]	RO	Reserved	

4.8.5.18 OSD2 Menu-1 Start Address LSB Register

Address Offset: OSD2_11h Default Value: 00

Bit	Access	Symbol	Description
[7:0]	R/W	M1_Menu_SA[7:0]	Point to the 1st row attribute of Menu-1 in OSD2 RAM.

4.8.5.19 OSD2 Menu-1 Start Address MSB Register

Address Offset: OSD2_12h Default Value: 10h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	M1_Menu_SA[13:8]	Point to the 1st row attribute of Menu-1 in OSD2 RAM.

4.8.5.20 OSD2 Menu-1 End Address LSB Register

Address Offset: OSD2_13h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	M1_Menu_EA[7:0]	Point to the end of Menu-1 in OSD2 RAM.

4.8.5.21 OSD2 Menu-1 End Address MSB Register

Address Offset: OSD2_14h Default Value: 14h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	M1_Menu_EA[13:8]	Point to the end of Menu-1 in OSD2 RAM.

4.8.5.22 OSD2 FontROM Base Address LSB Register

Address Offset: OSD2_16h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Font_BaseA_ROM[7:0]	Point to the start address in ROM, i.e., point to the 1st Font in ROM.

4.8.5.23 OSD2 FontROM Base Address MSB Register

Address Offset: OSD2_17h Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	Font_BaseA_ROM[13:8]	Point to the start address in ROM, i.e., point to the 1st Font in ROM.

4.8.5.24 OSD2 Menu-2 Enable Register

Address Offset: OSD2_18h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	M2_En	Set to 1 enable Menu-2 thread to display
[6:0]	RO	Reserved	

4.8.5.25 OSD2 Menu-2 Start Address LSB Register

Address Offset: OSD2_19h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	M2_Menu_SA[7:0]	Point to the 1st row attribute of Menu-2 in OSD2 RAM.

4.8.5.26 OSD2 Menu-2 Start Address MSB Register

Address Offset: OSD2_1Ah Default Value: 15h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	M2_Menu_SA[13:8]	Point to the 1st row attribute of Menu-2 in OSD2 RAM.

4.8.5.27 OSD2 Menu-2 End Address LSB Register

Address Offset: OSD2_1Bh Default Value: 00h

Bit	Access	Symbol	Description

[7:0]	R/W	M2_Menu_EA[7:0]	Point to the end of Menu-2 in OSD2 RAM.

4.8.5.28 OSD2 Menu-2 End Address MSB Register

Address Offset: OSD2_1Ch Default Value: 16h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	M2_Menu_EA[13:8]	Point to the end of Menu-2 in OSD2 RAM.

4.8.5.29 OSD2 Memory BIST result Register

Address Offset: OSD2_1Fh Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO	ORAMh_Fail	After OSD BIST done, get 1 in this bit shows the upper 8Kx16 of OSD2 Font/Menu RAM is failed.
[6]	RO	ORAM_Fail	After OSD BIST done, get 1 in this bit shows the lower 8Kx16 of OSD2 Font/Menu RAM is failed.
[5]	RO	PRAM_Fail	After OSD BIST done, get 1 in this bit shows the OSD2 PatternFill RAM is failed.
[4]	RO	FontROM_Fail	After OSD BIST done, get 1 in this bit shows the OSD2 Font ROM is failed.
[3]	RO	LRAM_Fail	After OSD BIST done, get 1 in this bit shows the OSD2 LUT RAM is failed.
[2:0]	RO	Reserved	

4.8.5.30 OSD2 BMP Control Register

Address Offset: OSD2_20h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	BMP_En	Set to 1 enable BMP to display
[6:4]	R/W	BMP_Nbpp	Defines current BMP for displaying is N bits per pixel. 000b: Reserved 001b: 1 bit/pixel 010b: 2 bits/pixel 011b: 3 bits/pixel 100b: 4 bits/pixel 101b: 5 bits/pixel 11Xb: 5 bits/pixel
[3:2]	R/W	BMP_Extra_Height[1:0]	BMP enlarge ratio in vertical direction: x1, x2, x3, x4 lines
[1:0]	R/W	BMP_Extra_Width[1:0]	BMP enlarge ratio in horizontal direction: x1, x2, x3, x4 dots

4.8.5.31 OSD2 BMP Start Address LSB Register

Address Offset: OSD2_21h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_SA[7:0]	Point to the top-left dot of BMP for displaying in OSD2 RAM.

4.8.5.32 OSD2 BMP Start Address MSB Register

Address Offset: OSD2_22h Default Value: 0Bh

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	

[5:0]	R/W	BMP_SA[13:8]	Point to the top-left dot of BMP for displaying in OSD2 RAM.

4.8.5.33 OSD2 BMP Alpha-Blending Control Register

Address Offset: OSD2_23h Default Value: 1Ah

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:4]	R/W	BMP_FG_aB_Mode[1:0]	Defines BMP alpha-blending for foreground when BG already alpha-Blended: 00b: All FG need alpha-Blended if BG is alpha-Blended; 01b: All FG no need alpha-Blended; 10b: All FG no need alpha-Blended, except their color is LUT[1]; 11b: All FG no need alpha-Blended, except their color is LUT[1..3];
[3:0]	R/W	BMP_aB_SourcePercent[3:0]	Defines the percentage of source image/video for mixed with OSD2 BMP.

4.8.5.34 OSD2 BMP Horizontal Size LSB Register

Address Offset: OSD2_24h Default Value: 40h

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_HSize[7:0]	Defines the horizontal size of BMP for displaying in OSD2 RAM. Unit is how manys word (16-bits) count (before enlarged).

4.8.5.35 OSD2 BMP Horizontal Size MSB Register

Address Offset: OSD2_25h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	BMP_HSize[10:8]	Defines the horizontal size of BMP for displaying in OSD2 RAM.

4.8.5.36 OSD2 BMP Vertical Size LSB Register

Address Offset: OSD2_26h Default Value: 60h

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_HSize[7:0]	Defines the vertical size of BMP for displaying in OSD2 RAM. Unit is how many lines count (before enlarged).

4.8.5.37 OSD2 BMP Vertical Size MSB Register

Address Offset: OSD2_27h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	BMP_HSize[10:8]	Defines the vertical size of BMP for displaying in OSD2 RAM.

4.8.5.38 OSD2 BMP Horizontal Start Position LSB Register

Address Offset: OSD2_28h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_HStart[7:0]	Defines the left boundary position of BMP for displaying, count in display clocks.

4.8.5.39 OSD2 BMP Horizontal Start Position MSB Register

Address Offset: OSD2_29h Default Value: 01h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	BMP_HStart[10:8]	Defines the left boundary position of BMP for displaying.

4.8.5.40 OSD2 BMP Vertical Start Position LSB Register

Address Offset: OSD2_2Ah Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_VStart[7:0]	Defines the top boundary position of BMP for displaying, count in lines.

4.8.5.41 OSD2 BMP Vertical Start Position MSB Register

Address Offset: OSD2_2Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	BMP_VStart[10:8]	Defines the top boundary position of BMP for displaying.

4.8.5.42 OSD2 BMP LUT Base Address Register

Address Offset: OSD2_2Ch Default Value: 80h

Bit	Access	Symbol	Description
[7:1]	R/W	BMP_LUT_BaseA[7:1]	Defines the LUT offset. For N-BPP BMP, its LUT segment starts with {BMP_LUT_BaseA[7:N], N'b0};
[0]	RO	Reserved	

4.8.5.43 OSD2 BMP Background Color Register

Address Offset: OSD2_2Dh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_BG_Color[7:0]	Defines the address of one LUT as BMP background color.

4.8.5.44 OSD2 Pattern_Fill Control Register

Address Offset: OSD2_30h Default Value: 48h

Bit	Access	Symbol	Description
[7]	R/W	Patt_En	Set to 1 enable Pattern_Fill to display
[6:4]	R/W	Patt_ColorDepth[2:0]	Defines nBP color: 000b: 8BPP 001b: 1BPP 010b: 2BPP 011b: 3BPP 100b: 4BPP 101b: 5BPP 110b: 6BPP 111b: 7BPP

[3:2]	R/W	Patt_RAM_Bit[1:0]	Defines the usage in Pattern RAM: 00b: 1 bit/pixel 01b: 2 bits/pixel 10b: 4 bits/pixel 11b: 8 bits/pixel
[1]	R/W	Patt_Independ_AB	Set to 1 for independent Alpha-Blending setting for Pattern_Fill; set to 0 for by OSD2_0B
[0]	WO	Reset_PRAM_Pointer	Write 1 to reset the Pattern RAM pointer for loading pattern data

4.8.5.45 OSD2 Pattern_Fill LUT Base Address Register

Address Offset: OSD2_31h Default Value: 80h

Bit	Access	Symbol	Description
[7:7]	R/W	Patt_LUT_BaseA[7:0]	Defines the MSB color in LUT for PatternFill color. Bit 0 is not used.

4.8.5.46 OSD2 Pattern_Fill Pattern Horizontal Size Register

Address Offset: OSD2_32h Default Value: 10h

Bit	Access	Symbol	Description
[7:0]	R/W	Patt_HSize[7:0]	For repeated pattern, this defines its width in the unit: Byte.

4.8.5.47 OSD2 Pattern_Fill Pattern Vertical Size Register

Address Offset: OSD2_33h Default Value: 10h

Bit	Access	Symbol	Description
[7:0]	R/W	Patt_VSize[7:0]	For repeated pattern, this defines its height in the unit: line.

4.8.5.48 OSD2 Pattern_Fill Pattern Row Shift Register

Address Offset: OSD2_34h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Patt_Row_Shift[7:0]	For repeated pattern, this defines horizontal shift in the unit: Byte, to build a delta-type pattern.

4.8.5.49 OSD2 Pattern_Fill Color High Bits Register

Address Offset: OSD2_35h Default Value: 05h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	Patt_aB_SourcePencent[3:0]	Alpha Blending percentage (n/16) for Filled patterns only. If set 0000b, alpha blending is disabled (0/16 * Original Video Source + 8/8 * PatternFill display); If set 0001b, blending as 1/16 * Original Video Source + 15/16 * PatternFill display; . . . If set N, blending as N/16 * Original Video Source + (16-N)/16 * PatternFill display;

4.8.5.50 OSD2 Pattern Enlarge Register

Address Offset: OSD2_36h Default Value: 00h

Bit	Access	Symbol	Description

[7:4]	RO	Reserved	
[3:2]	R/W	Patt_V_Enlarge[1:0]	For each repeated pattern, enlarge it in verical direction
[1:0]	R/W	Patt_H_Enlarge[1:0]	For each repeated pattern, enlarge it in horizontal direction

4.8.5.51 OSD2 Pattern_Fill Pattern RAM Write Port Register

Address Offset: OSD2_37h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	WO	PRAM_WrD_Port[10:8]	For building pattern, need to load via writing pattern to PRAM (Pattern RAM). After reset PRAM pointer, the PRAM pointer will increase after each burst write.

4.8.5.52 OSD2 Pattern_Fill Position, Horizontal Start LSB Register

Address Offset: OSD2_38h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Patt_HStart[7:0]	Allowable pattern display region: horizontal start

4.8.5.53 OSD2 Pattern_Fill Position, Horizontal Start MSB Register

Address Offset: OSD2_39h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	Patt_HStart[10:8]	Allowable pattern display region: horizontal start

4.8.5.54 OSD2 Pattern_Fill Position, Vertical Start LSB Register

Address Offset: OSD2_3Ah Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Patt_VStart[7:0]	Allowable pattern display region: vertical start

4.8.5.55 OSD2 Pattern_Fill Position, Vertical Start MSB Register

Address Offset: OSD2_3Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	Patt_VStart[10:8]	Allowable pattern display region: vertical start

4.8.5.56 OSD2 Pattern_Fill Position, Horizontal End LSB Register

Address Offset: OSD2_3Ch Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Patt_HEnd[7:0]	Allowable pattern display region: horizontal End

4.8.5.57 OSD2 Pattern_Fill Position, Horizontal End MSB Register

Address Offset: OSD2_3Dh Default Value: 01h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	Patt_HEnd[10:8]	Allowable pattern display region: horizontal End

4.8.5.58 OSD2 Pattern_Fill Position, Vertical End LSB Register

Address Offset: OSD2_3Eh Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	Patt_VEnd[7:0]	Allowable pattern display region: vertical End

4.8.5.59 OSD2 Pattern_Fill Position, Vertical End MSB Register

Address Offset: OSD2_3Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	Patt_VEnd[10:8]	Allowable pattern display region: vertical End

4.8.5.60 OSD2 Block Write Data LSB Register

Address Offset: OSD2_40h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	OSD2_BlockWr_D[7:0]	LSB Data to be block fill

4.8.5.61 OSD2 Block Write Data MSB Register

Address Offset: OSD2_41h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	OSD2_BlockWr_D[15:8]	MSB Data to be block fill

4.8.5.62 OSD2 Block Write Starting Address LSB Register

Address Offset: OSD2_42h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	OSD2_BlockWr_SA[7:0]	Starting Address of block fill

4.8.5.63 OSD2 Block Write Starting Address MSB Register

Address Offset: OSD2_43h Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	OSD2_BlockWr_SA[13:8]	Starting Address of block fill

4.8.5.64 OSD2 Block Write Length Register

Address Offset: OSD2_44h Default Value: 10h

Bit	Access	Symbol	Description
[7:0]	R/W	OSD2_BlockWr_L[7:0]	Block fill length (count)

4.8.5.65 OSD2 Block Write Control Register

Address Offset: OSD2_45h Default Value: 00h

Bit	Access	Symbol	Description

[7]	WO/ RO	OSD2_BlockWr_Trig OSD2_BlockWr_Done	Set to 1 to trigger block fill operation Get 1 means the block fill operation is done
[6]	R/W	OSD2_BlockWr_mode	
[5:0]	R/W	OSD2_BlockWr_L[13:8]	Block fill length (count)

4.8.5.66 OSD2 Trigger Read Control Register

Address Offset: OSD2_48h Default Value: 00h

Bit	Access	Symbol	Description
[7]	WO	Trig_ORAM_Rd	Set to 1 to trigger 8 words burst read from OSR2 Font/Menu RAM; Before trigger, please programming ORAM address first. And after set trigger, please wait the finish status: Page0_AAh<2> Grab_Ready
[6]	R/W	TrigRd_ExtraLn	Trigger Rd execution starts from next horizontal line if this bit set to 1; otherwise from the current line.
[5:4]	RO	Reserved	
[3]	R/W	NonTrigRd_Mode	0: ORAM read back data always from Trigger Read Option 1: ORAM read back from random read command
[2:0]	RO	Reserved	

4.8.5.67 ORAM Misc. Control Register

Address Offset: OSD2_4Fh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	ORAM_NoStop	0: ORAM power save mode 1: ORAM power steady mode
[6:0]	RO	Reserved	

4.8.5.68 OSD2 Char4BP Font Index Base Register

Address Offset: OSD2_50 Default Value: F0h

Bit	Access	Symbol	Description
[7:0]	R/W	Font_Index_8BP[8:1]	Defines the Char8BP font index base (offset). When character index small than this value*2 will be decoded as Char1BP (mono char) / Char3BP or Char2BP or Char4BP; else, Char8BP.

4.8.5.69 OSD2 Char8BP Font Memory Base Address LSB Register

Address Offset: OSD2_51h Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	Font_BaseA_8BP[7:0]	Defines the Char8BP font in memory, start with this base address (offset).

4.8.5.70 OSD2 Char8BP Font Memory Base Address MSB Register

Address Offset: OSD2_52h Default Value: 10h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	Font_BaseA_8BP[13:8]	Defines the Char8BP font in memory, start with this base address (offset).

4.8.5.71 Char3BP (Tw-SubFont) Control Register

Address Offset: OSD2_54h Default Value: 08h

Bit	Access	Symbol	Description
[7]	R/W	Char3BP_En	0: Char1BP mono Char 1: Char3BP mono Char
[6:5]	RO	Reserved	
[4:0]	R/W	Char3BP_Center[4:0]	Center sub-pixel sharpness coefficient (values 0~16, must be even number) Note: The summation of “Far*2 + Near*2 + Center” must be 16

4.8.5.72 Char3BP (Tw-SubFont) Coefficient Register

Address Offset: OSD2_55h Default Value: 13h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:4]	R/W	Char3BP_Far[1:0]	Far sub-pixel sharpness coefficient (values: 0~3) Note: The summation of “Far*2 + Near*2 + Center” must be 16
[3]	RO	Reserved	
[2:0]	R/W	Char3BP_Near[2:0]	Near sub-pixel sharpness coefficient (values: 0~7) Note: The summation of “Far*2 + Near*2 + Center” must be 16

4.8.5.73 OSD2 Char3BP Font Memory Base Address LSB Register

Address Offset: OSD2_56h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Font_BaseA_3BP[7:0]	Defines the Char3BP font in memory, start with this base address (offset).

4.8.5.74 OSD2 Char3BP Font Memory Base Address MSB Register

Address Offset: OSD2_57h Default Value: 18h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	Font_BaseA_3BP[13:8]	Defines the Char3BP font in memory, start with this base address (offset).

4.8.5.75 Reserved for OSD2 Char3BP Font ROM Base Address LSB Register

Address Offset: OSD2_58h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FontROM_BaseA_3BP [7:0]	Defines the Char3BP font in ROM, start with this base address (offset).

4.8.5.76 Reserved for OSD2 Char3BP Font ROM Base Address MSB Register

Address Offset: OSD2_59h Default Value: 02h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	FontROM_BaseA_3BP [13:8]	Defines the Char3BP font in ROM, start with this base address (offset).

4.9 LCD Output Control Register Set

4.9.1. Configuration Ready Status Register

Address Offset: P0_80h Default Value: 00h

Bit	Access	Symbol	Description
[7:1]	RO	Reserved	
[0]	RO	Cfg_Ready_8BCD	Configuration Ready Status of Page0 8X ~ DX

4.9.2. Input VSync Leading Edge to DE Time Counter Register

Address Offset: P0_81h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	VBi_Xclk[7:0]	Timing counter can be used to measure the time interval between leading edge of input vsync and first valid input pixel (# XCLK)

Address Offset: P0_82h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	VBi_Xclk[15:8]	

Address Offset: P0_83h Default Value: 00h

Bit	Access	Symbol	Description
[7:2]	RO	Reserved	
[1:0]	RO	VBi_Xclk[17:16]	

4.9.3. Line Buffer Configuration Register

Address Offset: P0_84h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	LB_PreFill_Xclk[7:0]	A delay time counted in XCLK between the leading edge of input Vsync and leading edge of output Vsync

Address Offset: P0_85h Default Value: 10h

Bit	Access	Symbol	Description
[7:0]	R/W	LB_PreFill_Xclk[15:8]	

4.9.4. Output VSync Front Porch Remapping Register

Address Offset: P0_87h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	HsFP_Remap[7:0]	Output HSync remap amount in vertical front porch period

4.9.5. Left Display Border Configuration LSB Register

Address Offset: P0_88h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	HLDSPLB[7:0]	When the index of output pixel is less than HLDSPLB, the value of output pixel is assigned as left display border with Frame color: {FMCLRRED, FMCLRGRN , FMCLRBLU} ({P0_9D, P0_9E, P0_9F})

Address Offset: P0_89h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	HDSPLB_INV	Horizontal border is on if HDSPLB_INV is set as follows 1: HLDSPLB < Horizontal border < HRDSPLB 0: Horizontal border < HLDSPLB or it > HRDSPLB
[6]	R/w	VDSPLB_INV	Vertical border is on if VDSPLB_INV is set as follows 1: VTDSPLB < < VBDSPLB 0: Vertical border < VTDSPLB or it > VBDSPLB
[5]	R/W	HDSPLB_STY	Horizontal Border style 1: mesh 0: solid
[4]	R/W	VDSPLB_STY	Vertical Border style 1: mesh 0: solid
[3]	RO	Reserved	
[2:0]	R/W	HLDSPLB[10:8]	

4.9.6. Right Display Border Configuration Register

Address Offset: P0_8Ah Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	HRDSPLB[7:0]	When the index of output pixel is greater than HRDSPLB, the value of output pixel is assigned as right display border with Frame color

Address Offset: P0_8Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	HRDSPLB[10:8]	

4.9.7. Top Display Border Configuration Register

Address Offset: P0_8Ch Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	HTDSPLB[7:0]	

Address Offset: P0_8Dh Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	R/W	HDSPLB_GRID[1:0]	H grip precision, 00b: 1 pixel 01b: 4 pixels 10b: 16 pixels 11b: 32 pixels
[5:4]	R/W	VDSPLB_GRID[1:0]	V grip precision 00b: 1 line 01b: 4 lines 10b: 16 lines 11b: 32 lines
[3]	RO	Reserved	
[2:0]	R/W	VTDSPLB[10:8]	

4.9.8. Bottom Display Border Configuration Register

Address Offset: P0_8Eh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	HBDSPLB[7:0]	

Address Offset: P0_8Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	VBDSPLB[10:8]	

4.9.9. Display Window Horizontal Start Register

Address Offset: P0_B0h Default Value: 20h

Bit	Access	Symbol	Description
[7:0]	R/W	DWHS_L[7:0]	Horizontal back porch

4.9.10. Display Window Vertical Start Register

Address Offset: P0_B2h Default Value: 10h

Bit	Access	Symbol	Description
[7:0]	R/W	DWVS_L[7:0]	Vertical back porch

4.9.11. Display Window Horizontal Width LSB Register

Address Offset: P0_B4h Default Value: E0h

Bit	Access	Symbol	Description
[7:0]	R/W	DWHSZ[7:0]	Horizontal active size

4.9.12. Display Window Horizontal Width MSB Register

Address Offset: P0_B5h Default Value: 01h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	DWHSZ[11:8]	Horizontal active size

4.9.13. Display Window Vertical Width LSB Register

Address Offset: P0_B6h Default Value: EAh

Bit	Access	Symbol	Description
[7:0]	R/W	DWVSZ[7:0]	Vertical active size

4.9.14. Display Window Vertical Width MSB Register

Address Offset: P0_B7h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	DWVSZ[10:8]	Vertical active size

4.9.15. Display Panel Horizontal Total Dots Per Scan Line LSB Register

Address Offset: P0_B8h Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	PH_TOT[7:0]	Output horizontal total dots

4.9.16. Display Panel Horizontal Total Dots Per Scan Line MSB Register

Address Offset: P0_B9h Default Value: 03h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	PH_TOT[11:8]	

4.9.17. Display Panel Vertical Total Lines Per Frame LSB Register

Address Offset: P0_BAh Default Value: 58h

Bit	Access	Symbol	Description
[7:0]	R/W	PV_TOT[7:0]	Output vertical total lines

4.9.18. Display Panel Vertical Total Lines Per Frame MSB Register

Address Offset: P0_BBh Default Value: 02h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	PH_TOT[10:8]	

4.9.19. Display Panel HSYNC Width Register

Address Offset: P0_BCh Default Value: 10h

Bit	Access	Symbol	Description
[7:0]	R/W	PH_PW[7:0]	The Hsync width of display panel

4.9.20. Display Panel VSYNC Width Register

Address Offset: P0_BEh Default Value: 02h

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4:0]	R/W	PV_PW[10:8]	The Vsync width of display panel

4.9.21. Panel Output Signal Control 1 Register

Address Offset: P0_C0h Default Value: 01h

Bit	Access	Symbol	Description
[7]	R/W	DAC_3_Phases	Enable DAC data separated by 1/3 clock phases. 0: Same clock phase, all RGB data are aligned to skew of CPH1 rising edge 1: 3 phases, each RGB data are aligned to different CPH1~3 (considered RGB swap by line)
[6]	R/W	sRGB_ITLC	Enable serial RGB interlace mode
[5]	R/W	En_sPanel	Enable Serial RGB (sPanel) output 0: for Analog panel (DAC output with TCON) 1: for Serial RGB panel (sD[7:0] + DCLKO + HS/VS/HDE)
[4]	R/W	sPanel_Dot	Select output RGB components when Serial RGB (sPanel) output 0: RGB from different cell position, consider swap 1: RGB from same dot position, no matter swap or not

[3]	R/W	Data_Neg	Reverse RGB output. 0: No reverse 1: RGB reverse.
[2]	R/W	PHSync_Polarity	PHSYNC Polarity. Default=0. 0: Active Low 1: Active High
[1]	R/W	PVSync_Polarity	PVSYNC Polarity. Default=0. 0: Active Low 1: Active High
[0]	R/W	PHDE_Polarity	PDE polarity. Default=1. 0: Active Low 1: Active High

4.9.22. Panel Output Signal Control 2 Register

Address Offset: P0_C1h Default Value: 10h

Bit	Access	Symbol	Description
[7:5]	R/W	STH_Width[2:0]	Programmable STH output width = (value + 1) clocks
[4]	R/W	STH_NegEdge	Output STH aligned to: 0: the rising edge internal panel clock 1: the falling edge internal panel clock
[3]	R/W	DCLK_INV	CLKO Polarity. Default=0. 0: Non-Invert, CLKO rising aligns to Data transition 1: Inverted, CLKO falling aligns to Data transition
[2:1]	R/W	LVDS_Mode[1:0]	LVDS Output data order: 00b:No rotate 01b:Rotate left 1Xb: Rotate right
[0]	R/W	Half_CPHn	Half CPHn frequency when set to 1

4.9.23. Panel VSYNC Frame Delay Control Register

Address Offset: P0_C2h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	En_psync_str_swt	Enable
[6:5]	R/W	Hso_2_Vso_Delay[1:0]	Adjust VSO Transition Edge
[4]	R/W	psyn_str	For Frame lock, input VSync (if exist) will trigger output VSync 0: Allow input vsync to trigger output vsync 1: Block input vsync triggering on output vsync
[3]	R/W	ELastPHs	Last HSync Line length option: 0: Short line, i.e., last hsync is less than 1.0 line 1: Long line , i.e.,last hsync is greater than 1.0 line
[2]	R/W	En_VSo_mode	Enable
[1]	R/W	Ignore_VSYNC	Ignore the input VSYNC. This can be used for output free run when input VSYN is not available
[0]	R/W	pout_dual	Enable dual LVDS

4.9.24. Panel VSYNC Frame Delay Line Count LSB Register

Address Offset: P0_C3h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	PV_Delay[7:0]	Delay last stage VSync output, in the unit of output HSync leading edge

4.9.25. Panel VSYNC Frame Delay Line Count MSB Register

Address Offset: P0_C4h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	En_RGB_To_YCBCR	Enable RGB convert to YCbCr
[6]	R/W	Daclk_inv	When encode 656 is enable to control CLKO Polarity. 0: Non-Invert, CLKO rising aligns to Data transition 1: Inverted, CLKO falling aligns to Data transition
[5]	R/W	dPLL_sOSD_2x	1: SPI_OSD clock is twice the speed of display clock 0: SPI_OSD clock is equal to display clock
[4]	R/W	En_VSo_mode_fph	
[3]	RO	Reserved	
[2:0]	R/W	PV_Delay[10:8]	

4.9.26. Serial RGB HSync Delay Register

Address Offset: P0_C5h Default Value: 60h

Bit	Access	Symbol	Description
[7:0]	R/W	sPanel_HS_Delay[7:0]	Delay output HSync for sPanel. (count in 3x panel clock) Value must >= 02h. This register is used to shift sPanel_HS, and align correct RGB color in sequence, for some sPanel do not have HDE input

4.9.27. Serial RGB HSync Width Register

Address Offset: P0_C6h Default Value: 85h

Bit	Access	Symbol	Description
[7]	R/W	sPanel_VsHs_Align	Enable output VSync align to HSync for sPanel 0: VSync not aligned to HSync 1: VSync aligned to the leading clock of HSync pulse.
[6]	R/W	sPanel_Vs_1T	Set output VSync width for sPanel 0: VSync width set by P0_BE (lines) 1: VSync 1T pulse only
[5:0]	R/W	sPanel_HS_Width[5:0]	Set output HSync width for sPanel. (count in 3x panel clock) Value must >= 01h

4.9.28. Output RGB Reordering Register

Address Offset: P0_C7h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	Pout_dual_ex	Enable lvds even/odd channel swap
[6:4]	R/W	Reserved	For test only {LnSwap_Sel, LnSwap_Inv, LnSwap_En}
[3]	R/W	BigEndian_E	Reverse bit [7:0] of RGB: 0: Non-Inverted, Little Endian. 1: Inverted, Big Endian.
[2:0]	R/W	RGB_Swap_E	RGB Channel Swapping: 000: RGB, 001: RBG, 010: GRB, 011: GRB, 1X0: BRG, 1X1: BGR;

4.9.29. Output PLL Divider 1 Register

Address Offset: P0_C8h Default Value: 15h

Bit	Access	Symbol	Description

[7]	R/W	VCO_SEL	'1' : VCO range 30MHz ~ 75MHz (better SSC performance) '0' : VCO range 150MHz ~ 300MHz (lower clock jitter)
[6:0]	R/W	DPLLDiv_F[6:0]	PLL feedback divider

4.9.30. Output PLL Divider 2 Register

Address Offset: P0_C9h Default Value: 02h

Bit	Access	Symbol	Description
[7]	R/W	SS_Clock_En	Enable Spread Spectrum clock output
[6:5]	R/W	SS_Clock_Deviation[1:0]	Spread Spectrum clock deviation selection
[4:0]	R/W	DPLLDIV_I[4:0]	PLL Input Divider

4.9.31. Output PLL Divider 3 Register

Address Offset: P0_CAh Default Value: 03h

Bit	Access	Symbol	Description
[7:6]	R/W	DPLL_mx[1:0]	PLL MUX Function Select PLLMX / Mode 2'b00 PLLCLK 2'b01 Keep High 2'b10 Bypass PLL (CKPLLIN/(2^(PLLDIV_O+PLL_DIV2))) 2'b11 Bypass PLL (~CKPLLIN)
[5]	R/W	DPLL_PowerDown_	Display PLL power down Control: 1: Display PLL power on 0: Display PLL power down
[4]	R/W	DPLL_xDiv2	Display PLL analog divider, set 1 to half frequency output
[3:2]	R/W	DPLL_ExDiv[1:0]	PLL additional divider 0: no divider 1: divided by 2 2: divided by 4 3: divided by 8
[1:0]	R/W	DPLLDIV_O	PLL Output Divider. output_freq = 27Mhz*(DLLDIV_F+2)/(2*(PLLDIV_I+2)) / (2^(PLLDIV_O+PLL_DIV2))

4.9.32. LLCK Clock Register

Address Offset: P0_CBh Default Value: 10h

Bit	Access	Symbol	Description
[7:4]	R/W	LLCK1_Phase[3:0]	CPH1 (LLCK1) phase, 1<= value <= LLCK_DivideN[3:0]
[3:0]	R/W	LLCK_DivideN[3:0]	LLCK pre-divider. 0/1 for no divide

4.9.33. Output LLCK Control Register

Address Offset: P0_CDh Default Value: 80h

Bit	Access	Symbol	Description
[7:4]	R/W	DACLK_Delay	
[3:2]	R/W	CPH_Shift[1:0]	0/1/2/3: shift by 0/3, 1/3, 2/3, 2/3 phases
[1]	R/W	Same_CPH	Output all 3 CPH1~CPH3 with same phases
[0]	R/W	Speed_3X	Enable Cell-Base Scaling

4.9.34. Delta Type Panel Control Register

Address Offset: P0_CEh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	Delta_L2_Drop	For Delta-type panel, drop cell or not in even Line
[6:4]	R/W	Delta_L2_Swap[2:0]	For Delta-type panel, RGB swap in even Line
[3]	R/W	Delta_L1_Drop	For Delta-type panel, drop cell or not in odd Line
[2:0]	R/W	Delta_L1_Swap[2:0]	For Delta-type panel, RGB swap in odd Line

4.9.35. Current VSync Count Register

Address Offset: P0_D0h Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO	Reserved	For test only, VSync Count

4.9.36. Serial RGB Sync Interlace Register

Address Offset: P0_D7h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	Fld2_fp_half	Field2 front porch with N.5
[6:4]	R/W	Fld2Align	Field2 is odd filed
[3]	R/W	InpFld_inv	Reverse field id
[4]	RO	Reserved	
[3:2]	R/W	InpFld_lockmd[1:0]	Input field lock mode
[1]	R/W	sRGB_No_Vpht	
[0]	RO	Reserved	

4.9.37. Display Window Horizontal Start Register

Address Offset: P0_D8h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Main_H_Start[7:0]	Horizontal start of display window

4.9.38. Display Window Vertical Start Register

Address Offset: P0_DAh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Main_V_Start[7:0]	Vertical start of display window

4.9.39. Display Window Horizontal Size LSB Register

Address Offset: P0_DCh Default Value: E0h

Bit	Access	Symbol	Description
[7:0]	R/W	Main_H_Size[7:0]	Horizontal size of display window

4.9.40. Display Window Horizontal Size MSB Register

Address Offset: P0_DDh Default Value: 01h

Bit	Access	Symbol	Description
[7:3]	RO	Reseved	
[2:0]	R/W	Main_H_Size[10:8]	

4.9.41. Display Window Vertical Size LSB Register

Address Offset: P0_DEh Default Value: EAh

Bit	Access	Symbol	Description
[7:0]	R/W	Main_V_Size[7:0]	Vertical size of display window

4.9.42. Display Window Vertical Size MSB Register

Address Offset: P0_DFh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reseved	
[2:0]	R/W	Main_V_Size[10:8]	

4.10 CVD Register Set

4.10.1. VD CONTROL

Address Offset: P2_00h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	hv_delay	This bit emulates the HV-delay mode found on Sony studio monitors. 0 = disabled (default) 1 = enabled
[6:5]	R/W	hpixel	These bits select the output display format. Standard pixels/line bit-setting NTSC, PAL(M) 858 00 (default) PAL(B,D,G,H,I,N,CN),SECAM 864 01 NTSC Square Pixel, PAL(M) Square Pixel 780 10 PAL(B,D,G,H,I,N) Square Pixel 944 11 When aconfig_en set 1, this register will be accessed as ready only and auto updated by mode detection.
[4]	R/W	vline_625	This bit selects the number of scan lines per frame. 0 = 525 (default) 1 = 625 When aconfig_en set 1, this register will be accessed as ready only and auto updated by mode detection.
[3:1]	R/W	colour_mode	These bits select video colour standard. 000 = NTSC (default) 001 = PAL (I,B,G,H,D,N) 010 = PAL (M) 011 = PAL (CN) 100 = SECAM When amode_en set 1, this register will be accessed as ready only and report the detected colour standard.
[0]	R/W	yc_src	This bit selects input video format. 0 = composite (default) 1 = S-Video (separated Y/C)

Address Offset: P2_01h Default Value: 01h

Bit	Access	Symbol	Description
[7]	R/W	cv_inv	This bit inverts the select signal for the analog input multiplexer during component video mode. 0 = not inverted (default) 1 = inverted
[6]	R/W	cv_src	This bit enables the component video input format. 0 = Disable the component video input (default) 1 = Component-Video (Y,Pb,Pr)
[5:4]	R/W	luma_notch_bw	These bits select luma notch width 00 = none (default) 01 = narrow 10 = medium 11 = wide

[3:2]	R/W	chroma_bw_lo	This bit set the chroma low pass filter to wide or narrow 0 = narrow (default) 1 = wide 2 = extra wide
[1]	R/W	chroma_burst5or10	This bit selects the burst gate width 0 = 5 subcarrier clock cycles (default) 1 = 10 subcarrier clock cycles
[0]	R/W	ped	This bit enables black level correction for 7.5 blank-to-black setup (pedestal). 0 = no pedestal subtraction 1 = pedestal subtraction (default)

Address Offset: P2_02h Default Value: 4Bh

Bit	Access	Symbol	Description
[7]	R/W	hagc_field	When this bit is “0” (the default), then the gain is updated once per line, after DC clamping. When this bit is set, then the gain is only updated once per field, at the start of vertical blank. 0 = off (default) 1 = on
[6]	R/W	mv_hagc	This bit, when set, automatically reduces the gain (set in register 4) by 25% when macro-vision encoded signals are detected 0 = off 1 = on (default)
[5:4]	R/W	dc_clamp_mode	This bit sets the mode for the analog front end DC clamping 00 = auto (default) 01 = backporch only 10 = synctip only 11 = off
[3]	R/W	dagc_en	This bit, when set, enables the digital AGC. The digital AGC is used in series with the analog gain. 0 = off 1 = on (default)
[2]	R/W	agc_half_en	This bit, when set, enables the half gain mode, when unlocked, for the analog front end. 0 = off 1 = on (default)
[1]	R/W	cagc_en	This bit when set enables the chroma AGC. If disabled, then the AGC target is used to drive directly the AGC gain. 0 = off 1 = on (default)
[0]	R/W	hagc_en	This bit when set enables the luma/composite AGC. If disabled, then the AGC target (register 04h) is used to drive directly the AGC gain. 0 = off 1 = on (default)

4.10.2. VD YC-SEPARATION CONTROL

Address Offset: P2_03h Default Value: 08h

Bit	Access	Symbol	Description
[7]	R/W	ntsc443	Enable NTSC443 mode When aconfig_en set 1, this register will be accessed as ready only and auto updated by mode detection.
[6]	R/W	tgain_en	Enable auto gain value for wide range ADC
[5]	R/W	color_bar	Select the color_bar as the fill pattern.
[4]	R/W	cbcr_avg	Enable low pass filter for analog input when component input.
[3]	R/W	colour_trap	This bit enables the notch-filter at the luma path after the comb filter. This filter can be turned on or off irrespective of the adaptive mode setting. 0 = Disabled (default) 1 = Enabled

[2:0]	R/W	adaptive_mode	These bits select modes for the composite signal's luma (Y) and chroma (C) separation before colour demodulation. 000 = fully adaptive comb (2-D adaptive comb) (default) 001 = vertical adaptive comb (1-D adaptive comb, vertical comb only) 010 = 5-Tap comb filter mode (PAL Mode only) 011 = basic luma notch filter mode (for very noisy and unstable pictures) 100 = simple 2-tap comb 101 = simple 3-tap comb 110 = 5-Tap hybrid comb filter (PAL Mode only) 111 = *Reserved* When aconfig_en set 1, this register will be accessed as ready only and auto updated by mode detection.

4.10.3. VD LUMA AGC VALUE

Address Offset: P2_04h Default Value: DDh

Bit	Access	Symbol	Description
[7:0]	R/W	hagc	These bits specify the luma AGC target value. The gain of the AGC is modified until the horizontal sync height is equal to this value. Note that if a MacroVision signal is detected and "mv_hagc_mode" (02.6h) is set, then this value is automatically reduced by 25%. Standard — Programming Value NTSC M — DDh (221d) (default) NTSC J — CDh (205d) PAL B,D,G,H,I, COMB N, SECAM — DCh (220d) PAL M,N — DDh (221d) NTSC M (MACROVISIOIN) — A6h (166d) PAL B,D,G,H,I, COMB N (MACROVISION) — AEh (174d) If "hagc_en" (register 02.0h) is "0", then "hagc" is used to directly drive the analog gain. In this case, a value of 64 represents a unity gain, 32 represents a one-half gain, and 128 denotes a double gain.

4.10.4. VD NOISE_THRESHOLD

Address Offset: P2_05h Default Value: 32h

Bit	Access	Symbol	Description
[7:0]	R/W	noise_thresh	This value sets the noise value at which the circuit considers a signal noisy. The detected noise value may be read back through register 9Fh ("status_noise"). If the detected noise value is greater than "noise_thresh", then register bit 3C.3h ("noisy") is set. Larger values of "status_noise" indicate noisier signals, so larger values of "noise_thresh" decreases the likelihood of "noisy" being set while smaller values of "noise_thresh" increases the likelihood of "noisy" being set. Default = 50

4.10.5. VD AGC_GATE_THRESHOLD

Address Offset: P2_06h Default Value: 0Ah

Bit	Access	Symbol	Description
[7]	R/W	adc_updn_swap	This bit swaps the DC clamp up/down controls to the analog front-end. 0 = Disabled (default) 1 = Enabled
[6]	R/W	adc_input_swap	This bit swaps the MSBs and LSBs from the analog front-end's ADC 0 = Disabled (default) 1 = Enabled

[5]	R/W	adc_cbcr_pump_swap	This bit swaps the Pb/Pr charge pump pairs to the analog front-end 0 = Disabled (default) 1 = Enabled
[4:0]	R/W	agc_gate_thresh	This specifies the threshold at which the rough gate generator creates a sync gate. Default = 10.

4.10.6. VD YC DELAY ADJUSTMENT

Address Offset: P2_07h Default Value: A0h

Bit	Access	Symbol	Description
[7]	R/W	blue_color	This bit set the fill pattern as blue color. 0 = Disabled (default) 1 = Enabled
[6]	R/W	cbcr_swap	This bit swaps Cb/Cr outputs. 0 = don't swap Cb/Cr (default) 1 = swap Cb/Cr
[5:4]	R/W	blue_mode	This bit controls the blue screen mode. 00 = Disabled 01 = Enabled 10 = Auto (Default) 11 = reserved
[3:0]	R/W	yc_delay	This 2's complement number controls the output delay between luma and chroma. Negative values shift luma outputs to the left while positive values shift luma values to the right. The range is [-5,7]. Default = 0 When aconfig_en set 1, this register will be accessed as ready only and auto updated by mode detection.

4.10.7. VD C/B/H/S ADJUSTMENT

Address Offset: P2_08h Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	contrast	These bits control the adjustable gain to the luma output path (default = 128).

Address Offset: P2_09h Default Value: 20h

Bit	Access	Symbol	Description
[7:0]	R/W	brightness	These bits control the adjustable brightness level to the luma output path. This value is offset by -32, i.e., a value of 32 (the default) implies a brightness level of 0, and a value of 0 implies a brightness level of -32.

Address Offset: P2_0Ah Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	saturation	These bits adjust the colour saturation (default = 128).

Address Offset: P2_0Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	hue	This 2's complement number adjusts the hue phase offset (default = 0).

4.10.8. VD CHROMA AGC

Address Offset: P2_0Ch Default Value: 8Ah

Bit	Access	Symbol	Description
[7:0]	R/W	cagc	These bits set the chroma AGC target (default = 138)

4.10.9. VD CHROMA KILL

Address Offset: P2_0Dh Default Value: 07h

Bit	Access	Symbol	Description
[7:6]	R/W	user_ckill_mode	Mode 0 uses auto hardware chroma kill, Mode 1 forces chroma kill on and Mode 2 forces chroma kill off (default=0)
[5]	R/W	vbi_ckill	When set, chroma is killed during VBI (default = 0)
[4]	R/W	hlock_ckill	When set, chroma is killed whenever horizontal lock is lost (default = 0)
[3:0]	R/W	chroma_kill	These bits set the chroma kill level (default = 7)

4.10.10. VD CHROMA PEAKING

Address Offset: P2_0Eh Default Value: 77h

Bit	Access	Symbol	Description
[7:5]	R/W	chroma_cor_val	Chroma coring value
[4]	R/W	chroma_cor_en	Enable chroma coring function.
[3]	R/W	cpeak_cor	Coring for high frequency chroma when cpeaking
[2:1]	R/W	cpeak_gain	Gain setting of chroma peaking.
[0]	R/W	cpeak_en	Enable chroma peaking function.

4.10.11. VD CHROMA AUTOPOSITION

Address Offset: P2_0Fh Default Value: 4Ch

Bit	Access	Symbol	Description
[7]	R/W	cpeak_bw	Cpeaking bandwidth selection.
[6]	R/W	cpress_en	Enable chroma compress when low level luma The level is adjusted by cpree_level
[5]	R/W	fixed_burstgate	When set, this bit disables the burst gate autoposition. The manual burstgate window position is defined by the burst_gate_start(0x2c) and burst_gate_end(0x2d) register. (default = 1)
[4:0]	R/W	cautopos	These bits set the chroma burst gate position relative to the auto centre position. (default = 12)

4.10.12. VD AGC PEAK NOMINAL

Address Offset: P2_10h Default Value: 0Ah

Bit	Access	Symbol	Description
[7]	R/W	reserved	
[6:0]	R/W	agc_peak_nominal	These bits set the luma peak white detection's AGC nominal peak white value. This value is added to 128 and then the result is multiplied by 4 (default = 10)

4.10.13. VD AGC PEAK AND GATE CONTROLS

Address Offset: P2_11h Default Value: B9h

Bit	Access	Symbol	Description
[7]	R/W	agc_gate_vsync_coarse	This bit forces coarse sync-tip and backporch gates to be used during vsync when VCRs are detected (default = 1).
[6]	R/W	agc_gate_vsync_stip	This bit forces sync-tip clamping during vsync (default = 0).
[5:4]	R/W	agc_gate_kill_mode	These bits determine the method that sync-tip and backporch gates are suppressed: 00 = off 01 = enabled – if sync-tip gate is killed, kill backporch gate 10 = enabled – if sync-tip gate is killed, kill backporch gate, except during vsync 11 = enabled – if sync-tip gate is killed, do not kill backporch gate (default)

[3]	R/W	agc_peak_en	This bit enables the AGC peak white detector (default = 1)
[2:0]	R/W	agc_peak_cntl	These bits set the time constant for the AGC peak white detector (default = 1)

4.10.14. VD AGC GATE WINDOW

Address Offset: P2_12h Default Value: 06h

Bit	Access	Symbol	Description
[7:3]	R/W	reserved	
[2:0]	R/W	agc_gate_start[10:8]	These high-order bits set the delay from the detected hsync for the rough gate generator

Address Offset: P2_13h Default Value: 82h

Bit	Access	Symbol	Description
[7:0]	R/W	agc_gate_start[7:0]	These low-order bits set the delay from the detected hsync for the rough gate generator. Default = 1666

Address Offset: P2_14h Default Value: 40h

Bit	Access	Symbol	Description
[7]	R/W	reserved	
[6:0]	R/W	agc_gate_width	These bits sets the width of the rough gates. Default = 64

4.10.15. VD AGC_BP_DELAY

Address Offset: P2_15h Default Value: 64h

Bit	Access	Symbol	Description
[7:0]	R/W	agc_bp_delay	These bits set the time delay from the sync tip gate to the backporch gate for the rough gate generator. Default = 100

4.10.16. VD LOCK COUNT

Address Offset: P2_16h Default Value: 74h

Bit	Access	Symbol	Description
[7:4]	R/W	locked_count_noisy_max	These bits set the max value of the hlock sensor for noisy signals. 8 is added to this value. (default = 7 ->15)
[3:0]	R/W	locked_count_clean_max	These bits set the max value of the hlock sensor for clean signals. 8 is added to this value. (default = 4 ->12)

4.10.17. VD H LOOP MAXSTATE

Address Offset: P2_17h Default Value: CBh

Bit	Access	Symbol	Description
[7:6]	R/W	hlock_vsync_mode	These bits control hsync locking during vsync: 00 = disabled 01 = enabled 10 = enabled except for noisy signals 11 = enabled only for VCR signals (default)
[5]	R/W	hstate_fixed	This bit when set forces the state machine to remain in the state set in “hstate_max” (default = 0)
[4]	R/W	disable_hfine	This bit, when set, disables the fine mode of the HPLL phase comparator. (default = 0)
[3]	R/W	hstate_unlocked	This bit sets the state when unlocked (default = 1)
[2:0]	R/W	hstate_max	These bits set the maximum state for the horizontal PLL state machine. The range of this register is 0 to 5, inclusive. Higher states have a finer PLL control. Values of “0” and “1” should not programmed into this register. If “hstate_fixed” is set, then this register is used to force the state. (default = 3).

4.10.18. VD CHROMA DTO INCREMENT

Address Offset: P2_18h Default Value: 21h

Bit	Access	Symbol	Description
[7]	R/W	cdto_fixed	This bit, when set, fixes the chroma DTO at its centre frequency (default = 0)
[7]	R/W	reserved	
[5:0]	R/W	cdto_inc[29:24]	These bits contain bits 29:24 of the 30-bit-wide chroma DTO increment. When aconfig_en set 1, this register will be accessed as ready only and auto updated by mode detection.

Address Offset: P2_19h Default Value: F0h

Bit	Access	Symbol	Description
[7:0]	R/W	cdto_inc[23:16]	These bits contain bits 23:16 of the 30-bit-wide chroma DTO increment. When aconfig_en set 1, this register will be accessed as ready only and auto updated by mode detection.

Address Offset: P2_1Ah Default Value: 7Ch

Bit	Access	Symbol	Description
[7:0]	R/W	cdto_inc[15:8]	These bits contain bits 15:8 of the 30-bit-wide chroma DTO increment. When aconfig_en set 1, this register will be accessed as ready only and auto updated by mode detection.

Address Offset: P2_1Bh Default Value: 1Fh

Bit	Access	Symbol	Description
[7:0]	R/W	cdto_inc[7:0]	These bits contain bits 7:0 of the 30-bit-wide chroma DTO increment. When aconfig_en set 1, this register will be accessed as ready only and auto updated by mode detection.

4.10.19. VD HORIZONTAL SYNC DTO INCREMENT

Address Offset: P2_1Ch Default Value: 20h

Bit	Access	Symbol	Description
[7]	R/W	hdto_fixed	This bit, when set, fixes the horizontal sync DTO at its centre frequency (default = 0)
[6]	R/W	reserved	
[5:0]	R/W	hdto_inc[29:24]	These bits contain bits 29:24 value of the 30-bit-wide horizontal sync DTO increment.

Address Offset: P2_1Dh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	hdto_inc[23:16]	These bits contain bits 23:16 value of the 30-bit-wide horizontal sync DTO increment.

Address Offset: P2_1Eh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	hdto_inc[15:8]	These bits contain bits 15:8 value of the 30-bit-wide horizontal sync DTO increment.

Address Offset: P2_1Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	hdto_inc[7:0]	These bits contain bits 7:0 value of the 30-bit-wide horizontal sync DTO increment.

4.10.20. VD HORIZONTAL SYNC RISING-EDGE OCCURRENCE TIME

Address Offset: P2_20h Default Value: 3Eh

Bit	Access	Symbol	Description
[7:0]	R/W	hsync_rising	These bits set the position of the expected hsync rising edge. It is used by the fine hsync detector. The fine detector uses this time position to sample the video signal for the rising edge of the hsync. Default = 62

4.10.21. VD HORIZONTAL SYNC PHASE OFFSET

Address Offset: 41h Default Value: 3Eh

Bit	Access	Symbol	Description
[7:0]	R/W	hsync_phase_offset	This register sets the offset value between the coarse hsync detector and the fine hsync detector. Nominally set to 62. The course detector actually finds the middle of the hsync so we need to subtract the nominal hsync width to find the beginning of the hsync. Default = 62

4.10.22. VD HORIZONTAL SYNC DETECT WINDOW

Address Offset: P2_22h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	hsync_gate_start	These bits control the PLL horizontal sync detect window for coarse sync detection. This specifies the beginning of the window. Default = 0

Address Offset: P2_23h Default Value: 40h

Bit	Access	Symbol	Description
[7:0]	R/W	hsync_gate_end	These bits control the PLL horizontal sync detect window for coarse sync detection. This specifies the end of the window. Default = 128

4.10.23. VD HORIZONTAL SYNC TIP DETECT WINDOW

Address Offset: P2_24h Default Value: E9h

Bit	Access	Symbol	Description
[7:0]	R/W	hsync_tip_start	These bits control the PLL horizontal sync tip detect window used for AGC control. This specifies the beginning of the window. Default = -23

Address Offset: P2_25h Default Value: 0Fh

Bit	Access	Symbol	Description
[7:0]	R/W	hsync_tip_end	These bits control the PLL horizontal sync tip detect window used for AGC control. This specifies the end of the window. Default = 15

4.10.24. VD HORIZONTAL SYNC RISING-EDGE DETECT WINDOW

Address Offset: P2_26h Default Value: 2Dh

Bit	Access	Symbol	Description
[7:0]	R/W	hsync_rising_start	These bits provide a programmable start time of the window that looks for the rising edge of the hsync. This is used by the coarse hsync detector. Default = 45

Address Offset: P2_27h Default Value: 50h

Bit	Access	Symbol	Description
[7:0]	R/W	hsync_rising_end	These bits provide a programmable end time for the window which spans across the rising-edge of the horizontal sync pulse. Default = 80

4.10.25. VD BACKPORCH INTERVAL

Address Offset: P2_28h Default Value: 22h

Bit	Access	Symbol	Description
[7:0]	R/W	backporch_start	These bits control the backporch detect window. This specifies the beginning of the window. Default = 34

Address Offset: P2_29h Default Value: 4Eh

Bit	Access	Symbol	Description
[7:0]	R/W	backporch_end	These bits control the backporch detect window. This specifies the end of the window. Default = 78

4.10.26. VD HSYNC FILTER GATE POSITION

Address Offset: P2_2Ah Default Value: D6h

Bit	Access	Symbol	Description
[7:0]	R/W	hblank_start	These bits specify the beginning of the horizontal-blank-interval window. Default = -42

Address Offset: P2_2Bh Default Value: 4Eh

Bit	Access	Symbol	Description
[7:0]	R/W	hblank_end	These bits specify the end of the horizontal-blank-interval window. Default = 78

4.10.27. VD CHROMA BURST GATE POSITION

Address Offset: P2_2Ch Default Value: 23h

Bit	Access	Symbol	Description
[7:0]	R/W	burst_gate_start	This specifies the beginning of the burst gate window. Note that this window is set to be bigger than the burst. The automatic burst position tracker finds the burst within this window. Default = 50

Address Offset: P2_2Dh Default Value: 64h

Bit	Access	Symbol	Description
[7:0]	R/W	burst_gate_end	These bits specifies the end of the burst gate window. Default = 70

4.10.28. VD ACTIVE VIDEO HORIZONTAL WINDOW

Address Offset: P2_2Eh Default Value: 82h

Bit	Access	Symbol	Description
[7:0]	R/W	hactive_start	These bits control the active video line time interval. This specifies the beginning of active line. This register is used to centre the horizontal position, and should *not* be used to crop the image to a smaller size. (default = 130) When aconfig_en set 1, this register will be accessed as ready only and auto updated by mode detection.

Address Offset: P2_2Fh Default Value: 50h

Bit	Access	Symbol	Description
[7:0]	R/W	hactive_width	These bits control the active video line time interval. This register specifies the width of the active line, and should *not* be used to crop the image to a smaller size. The value 640 is added to this register. (default = 80 ，640+80=720)

4.10.29. VD ACTIVE VIDEO VERTICAL WINDOW

Address Offset: P2_30h Default Value: 22h

Bit	Access	Symbol	Description
[7:0]	R/W	vactive_start	These bits control the first active video line in a field. This specifies the number of half lines from the start of a field. Default = 34. When aconfig_en set 1, this register will be accessed as ready only and auto updated by mode detection.

Address Offset: P2_31h Default Value: 61h

Bit	Access	Symbol	Description
[7:0]	R/W	vactive_height	These bits control the active video height. This specifies the height by the number of half lines. The value 384 is added to this register. (default = 97 . 394+97=481 half lines) When aconfig_en set 1, this register will be accessed as ready only and auto updated by mode detection.

4.10.30. VD VSYNC H LOCKOUT

Address Offset: P2_32h Default Value: 70h

Bit	Access	Symbol	Description
[7]	R/W	reserved	
[6:0]	R/W	vsync_h_min	This register defines the number of half-lines before the vsync that the hsync detector circuit is disabled. This is to make sure that the HPLL is not confused by the equalization pulses and the broad pulses. Also in VCR trick modes the VSYNC is just one 3 line wide pulse with no hsync structure so it must be ignored. Default = -16

Address Offset: P2_33h Default Value: 0Eh

Bit	Access	Symbol	Description
[7]	R/W	reserved	
[6:0]	R/W	vsync_h_max	This register defines the number of half-lines after the vsync that the hsync detector circuit is re-enabled. Default = 14

4.10.31. VD VSYNC AGC LOCKOUT

Address Offset: P2_34h Default Value: 6Ch

Bit	Access	Symbol	Description
[7]	R/W	reserved	
[6:0]	R/W	vsync_agc_min	This register defines the number of half-lines before the vsync that the AGC, SYNCTIP, and BACKPORCH gates are disabled. Default = -20

Address Offset: P2_35h Default Value: 90h

Bit	Access	Symbol	Description
[7:6]	R/W	vsync_clamp_mode	These bits control DC clamping during the vertical blanking interval. 00 = disabled 01 = enabled 10 = enabled except for noisy signals (default) 11 = enabled except for noisy signals and VCRs
[5:0]	R/W	vsync_agc_max	This register defines the number of half-lines after the vsync that the AGC, SYNCTIP, and BACKPORCH gates are re-enabled. Default = 16

4.10.32. VD VSYNC_CNTL

Address Offset: P2_38h Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	R/W	vsync_cntl	These bits set the vsync output mode 00 = output the vertical PLL vsync when the signal is noisy; otherwise use directly derived vsync (default) 01 = output the directly detected vsync 10 = output the vertical PLL derived vsync 11 = output the PLL vsync in alternate mode
[5:0]	R/W	vsync_thresh	This register specifies a relative threshold to add to the slice level for the purpose of vsync detection. Default = 0 (2's complement value)

Address Offset: P2_39h Default Value: 0Ah

Bit	Access	Symbol	Description
[7]	R/W	field_polarity	This bit sets the output field polarity. 0 . field=1 for odd fields, field=0 for even fields (default) 1 . field=0 for odd fields, field=1 for even fields
[6]	R/W	flip_field	This bit flips even/odd fields
[5]	R/W	veven_delayed	This bit delays detection of even fields by 1 vertical line (default = 0)
[4]	R/W	vodd_delayed	This bit delays detection of odd fields by 1 vertical line (default = 0)
[3:2]	R/W	field_detect_mode	These bits control the field detection logic. (default = 2)
[1:0]	R/W	vloop_tc	These bits set the vertical PLL time constant 0 = fast. Only useful if the vloop_cntl register is not 11. Internal values are 2 and 1. 1 = moderate. Internal values are 1 and ¼. 2 = slow. Internal values are ½ and 1/16 (default) 3 = very slow. Most useful for noisy signals. Internal values are ¼ and ½

4.10.33. VD STATUS REGISTER

Address Offset: P2_3Ah Default Value: 00h

Bit	Access	Symbol	Description
[7:5]	RO	mv_colourstripes	Macrovision colour stripes detected. The number indicates the number of colour stripe lines in each group
[4]	RO	mv_vbi_detected	MacroVision VBI pseudo-sync pulses detection 1 = Detected 0 = Undetected
[3]	RO	chromalock	Chroma PLL locked to colour burst 1 = Locked 0 = Unlocked
[2]	RO	vlock	Vertical lock 1 = Locked 0 = Unlocked
[1]	RO	hlock	Horizontal line locked 1 = Locked 0 = Unlocked
[0]	RO	no_signal	No signal detection 1 = No Signal Detected 0 = Signal Detected

Address Offset: P2_3Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:1]	RO	reserved	
[0]	RO	proscan_detected	Progressive Scan Detected

Address Offset: P2_3Ch Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO	vcr_rew	VCR Rewind Detected
[6]	RO	vcr_ff	VCR Fast-Forward Detected
[5]	RO	vcr_trick	VCR Trick-Mode Detected
[4]	RO	vcr	VCR Detected
[3]	RO	noisy	Noisy Signal Detected. This bit is set when the detected noise value (status register 7Fh) is greater than the value programmed into the "noise_thresh" register (05h).
[2]	RO	625lines_detected	625 Scan Lines Detected
[1]	RO	SECAM_detected	SECAM Colour Mode Detected
[0]	RO	PAL_detected	PAL Colour Mode Detected

4.10.34. VD CPRESS LEVEL

Address Offset: P2_3Eh Default Value: 07h

Bit	Access	Symbol	Description
[7:0]	R/W	cpress_level	Luma level for chroma compress

4.10.35. VD RESET REGISTER

Address Offset: P2_3Fh Default Value: 01h

Bit	Access	Symbol	Description
[7:1]	R/W	reserved	
[0]	R/W	soft_rst	Soft Reset

4.10.36. VD AUTO_MODE CONTROL1

Address Offset: P2_40h Default Value: 1Ch

Bit	Access	Symbol	Description
[7]	R/W	Capture	Debug usage: enable capture mode
[6:5]	R/W	Cap_Sel	Debug usage: capture data selection.
[4]	R/W	Dis_amode_rst	Debug usage:
[3]	R/W	Amode_blue	Enable blue screen when mode change transition.
[2]	R/W	Reserved	
[1]	R/W	Aconfig_en	Enable Auto Configuration for all TV standard. Note: When Aconfig_en is set to 1 then some registers' definition will be changed: reset to 0 and fine tuned as signed number. 1. Address x27[3:0] yc_delay 2. Address x4E hde_hstart 3. Address x50 vde_vstart 4. Address x51 vde_vheight
[0]	R/W	Amode_en	Enable Auto Mode Detection

4.10.37. VD AUTO_MODE STATUS

Address Offset: P2_41h Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO	Hold_fsc_det	The flag which detect the disappear of subcarrier
[6]	RO	Fsc3_present	Status of fsc3 detected flag
[5]	RO	fsc2_present	Status of fsc2 (4.43 Mhz) detected flag.
[4]	RO	fsc1_present	Status of fsc1 (3.58MHz) detected flag.
[3]	RO	amode_ready	The detection status (ready) of amode mode 1: det_colour_mode is stable 0: det_colour_mode is not ready

[2:0]	RO	det_colour_mode	Status of color mode by auto mode detection

4.10.38. VD AUTO_MODE VERTICAL DETECTION WINDOW

Address Offset: P2_42h Default Value: 10h

Bit	Access	Symbol	Description
[7:0]	R/W	mdet_line_start	Start of line setting for auto mode detection.

Address Offset: P2_43h Default Value: 28h

Bit	Access	Symbol	Description
[7:0]	R/W	mdet_line_end	End of line setting for auto mode detection

4.10.39. VD AUTO_MODE BURST POSITION1

Address Offset: 64h Default Value: 28h

Bit	Access	Symbol	Description
[7:0]	R/W	v50_bst_start	Start position of line setting for fsc2 detection

Address Offset: P2_45h Default Value: 40h

Bit	Access	Symbol	Description
[7:0]	R/W	v50_bst_end	End position of line setting for fsc2 detection

Address Offset: P2_46h Default Value: 20h

Bit	Access	Symbol	Description
[7:0]	R/W	v60_bst_start	Start position of line setting for fsc1 detection

Address Offset: P2_47h Default Value: 40h

Bit	Access	Symbol	Description
[7:0]	R/W	v60_bst_end	End position of line setting for fsc1 detection

4.10.40. VD AUTO_MODE PHASE VALUE

Address Offset: P2_48h Default Value: 40h

Bit	Access	Symbol	Description
[7:0]	R/W	phase1_abs[7:0]	Threshold of fsc1 absolute phase

Address Offset: P2_49h Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	phase2_abs[7:0]	Threshold of fsc2 absolute phase

4.10.41. VD AUTO_MODE CONTROL2

Address Offset: P2_4Ah Default Value: 33h

Bit	Access	Symbol	Description
[7]	R/W	Fix_level	Enable fixed subcarrier detection theshold.
[6:4]	R/W	F443_inc	The time constant for f443 detection.
[3]	R/W	Amode_sv	Enable auto no color detection for S-Video.
[2:0]	R/W	F443_dec	The time constant for f443 detection.

Address Offset: P2_4Bh Default Value: 37h

Bit	Access	Symbol	Description
[7]	R/W	Hold_det_en	Enable the auto detection hold on for noisy or weak input signals.
[6:4]	R/W	Phalt_inc	The time constant for phase detection.
[3]	R/W	Hold_noisy	When input signal is noisy, disable auto mode change.

[2:0]	R/W	Phalt_dec	The time constant for phase detection.

4.10.42. VD AUTO_MODE PHASE INC1

Address Offset: P2_50h Default Value: 87h

Bit	Access	Symbol	Description
[7:0]	R/W	sc_pa_pal[31:24]	Subcarrier Phase Increment of fsc1 (3.58MHz) detection

Address Offset: P2_51h Default Value: C1h

Bit	Access	Symbol	Description
[7:0]	R/W	sc_pa_pal [23:16]	Subcarrier Phase Increment of fsc1 (3.58MHz) detection

Address Offset: P2_52h Default Value: F0h

Bit	Access	Symbol	Description
[7:0]	R/W	Sc_pa_pal [15:8]	Subcarrier Phase Increment of fsc1 (3.58MHz) detection

Address Offset: P2_53h Default Value: 7Ch

Bit	Access	Symbol	Description
[7:0]	R/W	sc_pa_ntsc [7:0]	Subcarrier Phase Increment of fsc1 (3.58MHz) detection

4.10.43. VD AUTO_MODE PHASE INC2

Address Offset: P2_54h Default Value: A8h

Bit	Access	Symbol	Description
[7:0]	R/W	sc_pa_pal[31:24]	Subcarrier Phase Increment of fsc2 (4.43MHz) detection

Address Offset: P2_55h Default Value: 26h

Bit	Access	Symbol	Description
[7:0]	R/W	sc_pa_pal [23:16]	Subcarrier Phase Increment of fsc2 (4.43MHz) detection

Address Offset: P2_56h Default Value: 2Bh

Bit	Access	Symbol	Description
[7:0]	R/W	sc_pa_pal [15:8]	Subcarrier Phase Increment of fsc2 (4.43MHz) detection

Address Offset: P2_57h Default Value: 2Ch

Bit	Access	Symbol	Description
[7:0]	R/W	sc_pa_pal [7:0]	Subcarrier Phase Increment of fsc2 (4.43MHz) detection

4.10.44. VD AUTO_MODE HOLD CMAG

Address Offset: P2_5Ah Default Value: 08h

Bit	Access	Symbol	Description
[7:0]	R/W	Hold_cmag	The chroma magnitude threshold setting to hold mode change.

4.10.45. VD AUTO_MODE HOLD GAIN

Address Offset: P2_5Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Hold_gain	The gain threshold setting to hold mode change.

4.10.46. VD AUTO443_CDTO

Address Offset: P2_5Ch Default Value: 09h

Bit	Access	Symbol	Description

[7:0]	R/W	A443_CDTO	Programmable 2'nd Byte cdto value for auto config when NTSC443

4.10.47. VD NOISE REDUCTION CONTROL

Address Offset: P2_67h Default Value: 0Ah

Bit	Access	Symbol	Description
[7:4]	R/W	Reserved	
[3]	R/W	Auto_cavg	Automatic enable line average for chroma.
[2]	R/W	Manu_cavg	Manual force line average for chroma.
[1]	R/W	Osel_UV	Output YUV444 data to scaler
[0]	R/W	En_uv2cbcr	Enable uv2cbcr transfer for color domain.

Address Offset: P2_68h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	422_Swap_UV	Swap U/V for 444 to 422 conversion in NR
[6]	R/W	422_C_Ave	Enable chrom average filter on 444 to 422 conversion
[5]	R/W	444_C_Ave	Enable chrom average filter on 422 to 444 conversion
[4:0]	R/W	444_ignore_hcnt	Delay HDE in NR

Address Offset: P2_69h Default Value: 10h

Bit	Access	Symbol	Description
[7]	R/W	Reserved	
[6]	R/W	Nr_usignc	Treat chroma as unsigned value in NR block.
[5]	R/W	Nr_algm	Nr algorithm selection.
[4]	R/W	Nr_rnd	Enable Nr data rounding.
[3]	R/W	Nr_y_recur	Enable recursive noise reduction for luma
[2]	R/W	Nr_y_en	Enable noise reduction on luma path. Nr_y_en = 0: disable. Nr_y_en = 1: enable. (default)
[1]	R/W	Nr_c_recur	Enable recursive noise reduction for chroma
[0]	R/W	Nr_c_en	Enable noise reduction on chroma path. Nr_c_en = 0: disable. Nr_c_en = 1: enable. (default)

Address Offset: P2_6Ah Default Value: 88h

Bit	Access	Symbol	Description
[7:4]	R/W	Noise_threshold_y	Noise threshold for luma path
[3:0]	R/W	Noise_threshold_c	Noise threshold for chroma path

4.10.48. VD COMB FILTER CONTROL

Address Offset: P2_6Bh Default Value: 82h

Bit	Access	Symbol	Description
[7:2]	R/W	reserved	
[1]	R/W	sv_bf	Enable the bandpass filter on chroma path
[0]	R/W	noise_th_en	This bit enable the use of the noise detector value as the threshold value used to determine the best set of adaptive coefficients to be used . Default = 0

Address Offset: P2_6Ch Default Value: 00h

Bit	Access	Symbol	Description
[6:4]	R/W	Notch_Gain	Weighting for luma data from notch filter in adaptive yc separation.
[2:0]	R/W	Comb_Gain	Weighting for luma data from comb filter in adaptive yc separation.

Address Offset: P2_6Dh Default Value: 0Ah

Bit	Access	Symbol	Description
[6:0]	R/W	noise_th	These register bits specified the noise threshold used to determine the set of adaptive coefficients to be used. If the noise_th_en bit is disabled, this value is directly used as the threshold value. If the nosie_th_en bit is enable, this value is added to the value from the noise detector before it is used. Default = 10

4.10.49. VD HORIZONTAL SYNC DTO INCREMENT STATUS

Address Offset: P2_70h Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	RO	reserved	
[5:0]	RO	status_hdto_inc[29:24]	These bits contain status bits 29:24 of the 30-bit-wide horizontal sync DTO increment.

Address Offset: P2_71h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	status_hdto_inc[23:16]	These bits contain status bits 23:16 of the 30-bit-wide horizontal sync DTO increment.

Address Offset: P2_72h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	status_hdto_inc[15:8]	These bits contain status bits 15:8 of the 30-bit-wide horizontal sync DTO increment.

Address Offset: P2_73h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	status_hdto_inc[7:0]	These bits contain status bits 7:0 of the 30-bit-wide horizontal sync DTO increment.

4.10.50. VD CHROMA SYNC DTO INCREMENT STATUS

Address Offset: P2_74h Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	RO	reserved	
[5:0]	RO	status_cdto_inc[29:24]	These bits contain status bits 29:24 of the 30-bit-wide chroma sync DTO increment.

Address Offset: P2_75h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	status_cdto_inc[23:16]	These bits contain status bits 23:16 of the 30-bit-wide chroma sync DTO increment.

Address Offset: P2_76h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	status_cdto_inc[15:8]	These bits contain status bits 15:8 of the 30-bit-wide chroma sync DTO increment.

Address Offset: P2_77h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	status_cdto_inc[7:0]	These bits contain status bits 7:0 of the 30-bit-wide chroma sync DTO increment.

4.10.51. VD AGC STATUS

Address Offset: P2_78h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	status_agc_again	These bits contain the analog AGC gain value.

Address Offset: P2_79h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	status_agc_dgain	These bits contain the digital AGC gain value.

Address Offset: P2_7Ah Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	status_cmag	These bits contain the chroma magnitude.

Address Offset: P2_7Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	RO	reserved	
[5:0]	RO	status_cgain[13:8]	These bits contain the high order bits of the chroma gain.

Address Offset: P2_7Ch Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	status_cgain[7:0]	These bits contain the low-order bits of the chroma gain.

4.10.52. VD CORDIC FREQUENCY STATUS

Address Offset: P2_7Dh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	status_cordic_frerq	These bits contain the SECAM cordic frequency.

4.10.53. VD NOISE STATUS

Address Offset: P2_7Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	status_noise	This registers indicates how noisy the signal is. Larger values indicate noisier signals. This register is used in conjunction with programmable register 05h, “noise_thresh” and status bit 3C.3h, “noisy”.

4.10.54. VD LUMA Peaking

Address Offset: P2_80h Default Value: 04h

Bit	Access	Symbol	Description
[7]	R/W	Reserved	
[6]	R/W	Y_clamp_en	
[5:4]	R/W	peak_range	These bits set the range of peak_gain. Setting peak_range value 00 1 (default) 01 2 10 4 11 8 Ypeak = Y + YH *(peak_gain/peak_range) where Y is the luma and YH is the high frequency luma only
[3:1]	R/W	peak_gain	These bits set the gain for the luma horizontal peaking control. This allows adjustable gain to the luma around the colour subcarrier frequency (default = 2).

[0]	R/W	peak_en	This bit enables the luma horizontal peaking control around the colour subcarrier frequency 0 = Disabled (default) 1 = Enabled

4.10.55. VD MISC

Address Offset: P2_81h Default Value: 08h

Bit	Access	Symbol	Description
[7:4]	R/W	reserved	
[3]	R/W	Sync_uvflag	Synchronus uv flag for each line.
[2]	R/W	Woc_Sts_En	Enable lock stauts as write one clear flag.
[1]	R/W	Prompt_nos	Speed up the detection of no_signal flag and prompt blue screen.
[0]	R/W	Prompt_nov	Speed up the detection of no_vsync flag and prompt blue screen.

4.10.56. VD CHROMA_LOCK_CONFIG

Address Offset: P2_83h Default Value: 6Fh

Bit	Access	Symbol	Description
[7:4]	R/W	lose_chromalock_count	This register is used to tune the chromakill, higher values are more sensitive to losing lock (default = 6).
[3:1]	R/W	lose_chromalock_level	Set the level for chromakill (default = 7).
[0]	R/W	lose_chromalock_ckill	When set, chroma is killed whenever chromlock is lost (default = 1).

4.10.57. VD SYNC_LEVEL

Address Offset: P2_84h Default Value: 26h

Bit	Access	Symbol	Description
[7:0]	RO	SYNC_LEVEL[7:0]	Sync-tip level status

Address Offset: P2_85h Default Value: 26h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	RO	SYNC_LEVEL[10:8]	Sync-tip level status

4.10.58. VD BLANK_LEVEL

Address Offset: P2_86h Default Value: 26h

Bit	Access	Symbol	Description
[7:0]	RO	BLANK_LEVEL[7:0]	Blank level status

Address Offset: P2_87h Default Value: 26h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	RO	BLANK_LEVEL[10:8]	Blank level status

4.10.59. VD TGAIN RANGE

Address Offset: P2_88h Default Value: 26h

Bit	Access	Symbol	Description
[7:0]	R/W	AGC_VL	Lower Limit of ADC Input Signal for Tgain calculation

Address Offset: P2_89h Default Value: 55h

Bit	Access	Symbol	Description
[7:0]	R/W	AGC_VT_VL	Input Range Limit of ADC Input for Tgain calculation

4.10.60. VD CHROMA LOOPFILTER STATE

Address Offset: P2_8Ah Default Value: 0Ah

Bit	Access	Symbol	Description
[7:4]	R/W	reserved	
[3:1]	R/W	cstate	This register sets the chroma loopfilter bandwidth state, larger state has a slower response (default = 5)
[0]	R/W	fixed_cstate	This register fixes the state of chroma loopfilter to cstate. (default=0)

4.11 Image Enhancement Register Set

4.11.1. Vivid color Management

Address Offset: P3_60h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]			reserved
[3]	R/W	VVC_SRAM_PDn	When Disable Vivid Color, shut down SRAM for power saving.
[2]	R/W	VVC_prg_mode	1: Fast Mode Programming ; 0: Slow Mode Programming
[1:0]	R/W	VVC_En	11: Enable Vivid Color; 00: Disable Vivid Color

Address Offset: P3_61h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	W	Fast_ LUT _DATA	

Address Offset: P3_85h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	W	Slow_ LUT _DATA1	

Address Offset: P3_66h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	W	Slow_ LUT _DATA2	

Address Offset: P3_67h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	W	Slow_ LUT _DATA3	

Address Offset: P3_68h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	W	Slow_ LUT _DATA4	

Address Offset: P3_69h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	W	Slow_LUT_DATA5	

4.11.2. Ramp Smooth

Address Offset: P1_DAh Default Value: 10h

Bit	Access	Symbol	Description
[6]	R/W	En_RampSmooth	set to 1 for enabling hardware smooth operation
[5:4]	R/W	RampGap[1:0]	Allow to smooth step when the gap between steps is under value 4/8/12/16 (corresponding to setting value of 0/1/2/3)
[3]	R/W	RampSmooth565	0: 666, 1:565

4.11.3. Dithering

Address Offset: P0 _90h Default Value: 04h

Bit	Access	Symbol	Description
[7:6]	R/W	GATS[1:0]	Gamma Table Select. Default=2'b00. 00b: All R/G/B Gamma tables 01b: B Gamma table 10b: G Gamma table 11b: R Gamma table
[5]	R/W	Reserved	
[4]	R/W	Tp_dith_en	
[3]	R/W	Sp_dith_2b	
[2]	R/W	ShortVS_Black	
[1]	R/W	Gamma_en	Enable Gamma correction
[0]	R/W	Dither_en	Enable Dithering: 0: Disable Dithering, output full 8 bit 1: 6 bits Dithering

4.11.4. Gamma Correction

4.11.4.1 Built-in Pattern Generator Control Register

Address Offset: P0 _91h Default Value: 0Ch

Bit	Access	Symbol	Description
[7]	R/W	EFMCLR	Enable Frame background color Turn on this bit may disable Scaler's color and show user-defined color on LCD panel. See 0x9D, 0x9E and 0x9F for user-defined frame color.
[6]	R/W	ESLDSW	This bit may enable pattern generator shows 9 patterns sequentially. EFMCLR, ESLDSW — Output 2'b0X — Normal Color 2'b10 — Still pattern 2'b11 — Motion patterns
[5]	R/W	EVBAR	Enable Vertical Bar Patterns
[4]	R/W	PLBIT	1: indicate 8-bit patterns 0:indicate 6-bit patterns
[3]	R/W	REVERSED	
[2:0]	R/W	PTN	Show nth pattern on LCD panel when EFMCLR is enabled When Both EFMCLR and ESLDSW are enabled, pattern generator may show 0, 1 ,2 …up to PTNth.

4.11.4.2 Color Bar Width

Address Offset: P0 _92h Default Value: 3Bh

Bit	Access	Symbol	Description
[7:0]	R/W	CBAR_WIDTH[7:0]	

4.11.4.3 GAMMA Table Address Port Register

Address Offset: P0 _93h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	GAMMA_ADR	Gamma coefficient table address. The Index range is 00h~FFh

4.11.4.4 GAMMA Table Write Data Port Register

Address Offset: P0 _94h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	WO	GAMMA_WR_D	Gamma coefficient write data port.

4.11.5. DCTi/DLTi Control Register

Address Offset: P0_60h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2]	R/W	DCTi_Dist_Sel	DCTI distance selection: 1 for longer distance
[1]	RO	Reserved	
[0]	R/W	DLTi_Dist_Sel	DLTI distance selection: 1 for longer distance

4.11.6. Peaking Register

Address Offset: P0_61h Default Value: 08h

Bit	Access	Symbol	Description
[7]	R/W	Peaking_En	Enable Peaking function
[6]	R/W	Peaking_LR_Disable	Peaking boundary mode
[5:0]	R/W	Peaking_Coring	

4.11.7. Peaking Band-Pass Coefficient Register

Address Offset: P0_62h Default Value: 04h

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4:0]	R/W	BandPass_Coef[4:0]	

4.11.8. Peaking High-Pass Coefficient Register

Address Offset: P0_63h Default Value: 04h

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4:0]	R/W	HighPass_Coef[4:0]	

4.11.9. Peaking Low-Pass Coefficient Register

Address Offset: P0_64h Default Value: 02h

Bit	Access	Symbol	Description
[7:4]	R/W	WLE_Gain[3:0]	
[3]	RO	Reserved	
[2:0]	R/W	Peaking_LP_Coef	

4.11.10. DCTi_0 Gain and Coring Register

Address Offset: P0_65h Default Value: 08h

Bit	Access	Symbol	Description
[7:5]	R/W	DLTI_Gain_0	DLTI Gain Register
[4:0]	R/W	DLTI_Coring_0	DLTI Coring Register

4.11.11. DCTi_1 Gain and Coring Register

Address Offset: P0_66h Default Value: 08h

Bit	Access	Symbol	Description
[7:5]	R/W	DLTI_Gain_1	DLTI Gain Register
[4:0]	R/W	DLTI_Coring_1	DLTI Coring Register

4.11.12. Cb/Cr Delay Register

Address Offset: P0_67h Default Value: 1Eh

Bit	Access	Symbol	Description
[7]	R/W	U_delay	Cb signal delay control. 0: no delay (default) 1: 1 pixel delay
[6:5]	R/W	V_delay	Cr signal delay control. 00: no delay (default) 01: 1 pixel delay 10: 2 pixel delay 11: 3 pixel delay
[4:0]	R/W	DCTI_Threshold	DCTI performing Threshold Limit

4.11.13. Contrast Adjust Register

Address Offset: P0_68h Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	Contrast[7:0]	

4.11.14. Contrast Adjust Register

Address Offset: P0_69h Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	LumaBRIBrightness[7:0]	

4.11.15. Hue Sin Adjust Register

Address Offset: P0_6Ah Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	HueSin	

4.11.16. Hue Cos Adjust Register

Address Offset: P0_6Bh Default Value: 7Fh

Bit	Access	Symbol	Description
[7:0]	R/W	HueCos	

4.11.17. Chroma Satureation Adjust Register

Address Offset: P0_6Ch Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	reg_Saturation[7:0]	

4.11.18. White Level Expansion Threshold Register

Address Offset: P0_6Dh Default Value: EBh

Bit	Access	Symbol	Description
[7:0]	R/W	WLE_TH[7:0]	White Level Expansion Threshold

4.11.19. Black Level Expansion Threshold Register

Address Offset: P0_6Eh Default Value: 10h

Bit	Access	Symbol	Description
[7:0]	R/W	BLE_TH[7:0]	Black Level Expansion Threshold

4.11.20. VIP Black Level Expansion Gain/Offset Control Register

Address Offset: P0_6Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	BLE_GAIN	Black Level Expansion Gain
[3:2]	R/W	WLE_OFFSET	White Level Expansion Offset
[1:0]	R/W	BLE_OFFSET	Black Level Expansion Offset

4.12 Adaptive Contrast Enhancement Register Set

4.12.1 ACE_VMASK_START

Address Offset: P3_77h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	ace_vmask_start[7:0]	

Address Offset: P3_78h Default Value: 00h

Bit	Access	Symbol	Description
[7:2]	R/W	reserved	
[1:0]	R/W	ace_vmask_start[9:8]	

4.12.2 ACE_VMASK_WIDTH

Address Offset: P3_79h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	ace_vmask_width[7:0]	

Address Offset: P3_7Ah Default Value: 00h

Bit	Access	Symbol	Description
[7:2]	R/W	reserved	
[1:0]	R/W	ace_vmask_width[9:8]	

4.12.3 ACE_LPF_SEL

Address Offset: P3_7Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:5]	R/W	reserved	
[4:2]	R/W	ace_lpf_select	Low pass filter for normal distribution gain result.
[1]	R/W	Shape_coef_sel	Disable shape limitation adjustment.
[0]	R/W	Film_coef_sel	Disable Film mode coefficient gain.

4.12.4 ACE_GAIN

Address Offset: P3_7Ch Default Value: E0h

Bit	Access	Symbol	Description
[7:0]	R/W	ace_gain	Adaptive Contrast Gain ratio.

4.12.5 ACE_RATE

Address Offset: P3_7Dh Default Value: 03h

Bit	Access	Symbol	Description
[7]	R/W	ACE_soft_reset	Software reset for ACE block.
[6]	RO	Reserved	
[5]	R/W	ACE_vmdt	Debug mode to mask data as black in ace vmask window.
[4]	R/W	ACE_vmon	Enable VMask for ACE with adjustable window
[3:2]	RO	Reserved	
[1:0]	R/W	LPFrate	Adjustable time constant for adaptive histogram calculation.

4.12.6 ACE_DDB_GAIN

Address Offset: P3_7Eh Default Value: 84h

Bit	Access	Symbol	Description
[7:4]	R/W	deep_darkbright_gain	
[3:0]	R/W	deep_chroma_gain	

4.12.7 ACE_CTRL

Address Offset: P3_7Fh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	ace_enable	Enable Adaptive Contrast Enhancement
[6]	R/W	deep_gain_en	Eanble Deep Dark and Bright Enhancement
[5]	R/W	NDG_gain_en	Enable Normal Distribution Gain for Color Compensation
[4:0]	R/W	Reversed	
[0]	R/W	Byp_ACE	Bypass Adaptive Contrast Enhancement block.

4.13 Auto Offset Calibration Register Set

4.13.1. Auto Offset Calibrate Setting

Address Offset: P3_00h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	atOffset_Done	Auto Offset Calibration Done flag
[6:4]	R/W	reserved	
[3]	R/W	atOffset_tne_pol	Calibration increase/decrease polarity, 0: if result lower than target then INCREASE base register 1: if result lower than target then DECREASE base register
[2]	R/W	reserved	
[1]	R/W	atO_srst_b_s	Auto offset calibration soft ware reset, write 1 reset
[0]	R/W	atOffset_en	Auto offset enable. Write 1:enable

4.13.2. Offset Low Limit

Address Offset: P3_01h Default Value: 60h

Bit	Access	Symbol	Description
[7:0]	R/W	atOffset_L_lmt	Offset Low Limit Value for Updating Offset register

4.13.3. Offset High Limit

Address Offset: P3_02h Default Value: 90h

Bit	Access	Symbol	Description
[7:0]	R/W	atOffset_H_lmi	Offset High Limit Value for Updating Offset register

4.13.4. Auto Offset Calibration Threshold

Address Offset: P3_03h Default Value: 90h

Bit	Access	Symbol	Description
[7:0]	R/W	atOffset_Th	Chroma Summary Threshold, if | Summary – atOffset_ref_val | > atOffset_Th, then auto change Offset Register Value

4.13.5. Auto Offset Reference Value

Address Offset: P3_04h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	atOffset_ref_val[7:0]	Chroma summary reference Value Low byte

Address Offset: P3_05h Default Value: 20h

Bit	Access	Symbol	Description
[7:0]	R/W	atOffset_ref_val[15:8]	Chroma summary reference Value High byte

4.13.6. Auto Offset Tune Step

Address Offset: P3_06h Default Value: 04h

Bit	Access	Symbol	Description
[7:5]	R/W	reserved	
[4:0]	R/W	atOffset_setp	Offset change Step value while write to Offset Register

4.13.7. Auto Offset Calculation Scan Mode

Address Offset: P3_07h Default Value: 01h

Bit	Access	Symbol	Description
[7]	R/W	atOffset_Vscan	1: Chroma Calculation per frame
[6:3]	R/W	reserved	
[2:0]	R/W	atOffset_scan_sel	If Vscan=0, 000/001/010/011 : Chroma Calculation per 1/4/8/16 line 100/101/110/111 : Chroma Calculation per 32/64/128/256 line

4.13.8. Auto Offset Chroma Register Setting

Address Offset: P3_07h Default Value: 05h

Bit	Access	Symbol	Description
[7:6]	R/W	atOffset_R_src	Cr Offset Value source register, 1X/01/00 : G_in/B_in/R_in
[5:4]	R/W	atOffset_R_wrsel	Cr target register to write updated value, 1X/01/00 : P0_0B/P0_0C/P0_0A
[7:6]	R/W	atOffset_B_src	Cb Offset Value source register, 1X/01/00 : G_in/B_in/R_in
[5:4]	R/W	atOffset_B_wrsel	Cb target register to write updated value, 1X/01/00 : P0_0B/P0_0C/P0_0A

Relative Register P0_0A/P0_0B/P0_0C (ADC Offset) ; P0_C0, P0_CA~P0_CC (Color Range Probing)

4.14 FeH Core Register Set

4.14.1. FeH Control Register

Address Offset: P2_A0h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	PDn_FeH	
[6]	R/W	Reserved	
[5:4]	R/W	fPLL_Extra_Div_Fe	
[3]	R/W	Reserved	
[2]	R/W	Nap_Sel	
[1]	R/W	FeH_Debug	
[0]	R/W	En_FeH	

4.14.2. FeH DTO

Address Offset: P2_A1h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FeH_DTO[7:0]	

Address Offset: P2_A2h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FeH_DTO[15:8]	

4.14.3. Fe Step

Address Offset: P2_A3h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FeH_Step[7:0]	

Address Offset: P2_A4h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FeH_Step[15:8]	

4.14.4. Fe Sign

Address Offset: P2_A5h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FeH_Sign[7:0]	

4.14.5. Fe HBP

Address Offset: P2_A6h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Fe_HBP[7:0]	

4.14.6. Fe Hsize

Address Offset: P2_A7h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Fe_HSize[7:0]	

Address Offset: P2_A8h Default Value: 00h

Bit	Access	Symbol	Description
[7:5]	R/W	Reserved	
[4]	R/W	Fe_HBP[8]	
[3]	R/W	Reserved	
[2:0]	R/W	Fe_HSize[10:8]	

4.14.7. Fe VSize

Address Offset: P2_A9h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Fe_VSize[7:0]	

Address Offset: P2_AAh efault Value: 00h

Bit	Access	Symbol	Description
[7:2]	R/W	Reserved	
[1:0]	R/W	Fe_VSize[9:8]	

4.14.8. FeH Gain

Address Offset: P2_B8h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FeH_Gain01	

Address Offset: P2_B9h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FeH_Gain02	

Address Offset: P2_BAh Default Value: 00h

Bit	Access	Symbol	Description

[7:0]	R/W	FeH_Gain03	

Address Offset: P2_BBh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FeH_Gain04	

Address Offset: P2_BCh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FeH_Gain05	

Address Offset: P2_BDh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FeH_Gain06	

Address Offset: P2_BEh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FeH_Gain07	

Address Offset: P2_BFh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FeH_Gain08	

4.14.9. FeH_Step_Inc

Address Offset: P2_C0/D0h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc11/51	
[3:0]	R/W	FeH_Step_Inc12/52	

Address Offset: P2_C1/D1h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc13/53	
[3:0]	R/W	FeH_Step_Inc14/54	

Address Offset: P2_C2/D2h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc15/55	
[3:0]	R/W	FeH_Step_Inc16/56	

Address Offset: P2_C3/D3h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc17/57	
[3:0]	R/W	FeH_Step_Inc18/58	

Address Offset: P2_C4/D4h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc21/61	
[3:0]	R/W	FeH_Step_Inc22/62	

Address Offset: P2_C5/D5h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc23/63	

[3:0]	R/W	FeH_Step_Inc24/64	

Address Offset: P2_C6/D6h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc25/65	
[3:0]	R/W	FeH_Step_Inc26/66	

Address Offset: P2_C7/D7h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc27/67	
[3:0]	R/W	FeH_Step_Inc28/68	

Address Offset: P2_C8/D8h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc31/71	
[3:0]	R/W	FeH_Step_Inc32/72	

Address Offset: P2_C9/D9h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc33/73	
[3:0]	R/W	FeH_Step_Inc34/74	

Address Offset: P2_CA/DAh Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc35/75	
[3:0]	R/W	FeH_Step_Inc36/76	

Address Offset: P2_CB/DBh Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc37/77	
[3:0]	R/W	FeH_Step_Inc38/78	

Address Offset: P2_CC/DCh Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc41/81	
[3:0]	R/W	FeH_Step_Inc42/82	

Address Offset: P2_CD/DDh Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc43/83	
[3:0]	R/W	FeH_Step_Inc44/84	

Address Offset: P2_CE/DEh Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc45/85	
[3:0]	R/W	FeH_Step_Inc46/86	

Address Offset: P2_CF/DFh Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	FeH_Step_Inc47/87	
[3:0]	R/W	FeH_Step_Inc48/88	

4.15 Color Space Convert Register Set

4.15.1 YUV To RGB Convert Register – 1

Address Offset: P1 _B0h Default Value: 95h

Bit	Access	Symbol	Description
[7:0]	R/W	YCoef_R	CSC Red Coef of Y 1.7-bit fixed point

4.15.2 YUV To RGB Convert Register – 2

Address Offset: P1 _B1h Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5]	R/W	CbCoef_R_Sign	Cb To R Coefficient, Sign bit
[4:0]	R/W	CbCoef_R[4:0]	Cb To R Coefficient

4.15.3 YUV To RGB Convert Register – 3

Address Offset: P1 _B2h Default Value: CCh

Bit	Access	Symbol	Description
[7:0]	R/W	CrCoef_R	CSC Red Coef of Cr 1.7-bit fixed point

4.15.4 YUV To RGB Convert Register – 4

Address Offset: P1 _B3h Default Value: 95h

Bit	Access	Symbol	Description
[7:0]	R/W	YCoef_G	CSC Green Coef of Y 1.7-bit fixed point

4.15.5 YUV To RGB Convert Register – 5

Address Offset: P1 _B4h Default Value: 32h

Bit	Access	Symbol	Description
[7:0]	R/W	CbCoef_G	CSC Green Coef of Cb 1.7-bit fixed point

4.15.6 YUV To RGB Convert Register – 6

Address Offset: P1 _B5h Default Value: 68h

Bit	Access	Symbol	Description
[7:0]	R/W	CrCoef_G	CSC Green Coef of Cr 1.7-bit fixed point

4.15.7 YUV To RGB Convert Register – 7

Address Offset: P1 _B6h Default Value: 95h

Bit	Access	Symbol	Description
[7:0]	R/W	YCoef_B	CSC Blue Coef of Y 0.8-bit fixed point

4.15.8 YUV To RGB Convert Register – 8

Address Offset: P1 _B7h Default Value: 81h

Bit	Access	Symbol	Description
[7:0]	R/W	CbCoef_B	CSC Blue Coef of Cb 0.8-bit fixed point

4.15.9 YUV To RGB Convert Register – 9

Address Offset: P1 _B8h Default Value: C0h

Bit	Access	Symbol	Description
[7]	R/W	En_YCbCr2RGB	Set to 1 for enabling YUV (YCbCr) Color space converting to RGB
[6]	R/W	Y_Sub16	Set to 1 for Luma offset 16; 0 for offset 0;
[5]	R/W	CrCoef_B_Sign	Cr To B Coefficient, Sign bit
[4:0]	R/W	CrCoef_B	CSC Blue Coef of Cr 2.6-bit fixed point

4.16 Command Queue Register Set

4.16.1 CQ general setting

Address Offset: P3_C0h Default Value: 00h

Bit	Access	Symbol	Description
[7]	W1 Trig	soft_reset	Write '1' to assert software reset to all the registers in this module
[6:2]		Reserved	
[1]	R/W	debug_mode	Set '1' to read SRAM data from data port.
[0]	R/W	CQ_locked	Lock command queue not to be issued

4.16.2 CQ interrupt

Address Offset: P3_C1h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]		Reserved	
[3]	R/W	IM_overflow	Interrupt mask of command queue overflow
[2]	R/W	IM_timeout	Interrupt mask of wait trigger signal time-out
[1]	R/W	IM_CQ_invalid	Interrupt mask of invalid command
[0]	R/W	IM_CQ_done	Interrupt mask of command queue done

Address Offset: P3_C2h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]		Reserved	
[3]	R/W1C	IS_overflow	Interrupt status of command queue overflow
[2]	R/W1C	IS_timeout	Interrupt status of wait trigger signal time-out
[1]	R/W1C	IS_CQ_invalid	Interrupt status of invalid command
[0]	R/W1C	IS_CQ_done	Interrupt status of command queue done

4.16.3 CQ trigger control

Address Offset: P3_C3h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	CQ_issue	Issue command queue (de-asserted when done)
[6]	RO	CQ_action	If (CQ_locked==0) CQ_action <= CQ_issue; Else (CQ_issue==0) CQ_action <= 0;
[5:2]		Reserved	
[1:0]	R/W	trigger_source	00b: software trigger 01b: vsync rising 10b: vde falling

4.16.4 CQ Port Register

Address Offset: P3_C5h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Data Port	Data port to SRAM **(read for debug mode only)**

4.16.5 CQ time-out control

Address Offset: P3_C6h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	timeout_threshold	Time out threshold in WAIT TRIGGER state. If the timer tick (1ms) is counted to this threshold, command queue will start programming sequence and then issue a time-out interrupt. Set 0 to disable this feature.

4.16.6 CQ queue pointer

Address Offset: P3_C7h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Queue Pointer	When debug mode, the SRAM address will be override by this queue pointer, and the corresponding data can be read from data port.

4.16.7

Address Offset: P3_C8h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	line_count_record[7:0]	The line number when command queue is done.

Address Offset: P3_C9h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]		Reserved	
[3:0]	RO	line_count_record[11:8]	The line number when command queue is done.

4.16.8

Address Offset: P3_CAh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	delay_amount[7:0]	

Address Offset: P3_CBh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	delay_enable	Used to delay command queue programming sequence after triggered.
[6]	R/W	delay_unit	0: clock cycle; 1: line (hsync rising)
[5:2]		Reserved	
[1:0]	R/W	delay_amount [9:8]	

4.16.9

Address Offset: P3_C8h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	line_count_freerun[7:0]	The line number.

Address Offset: P3_C9h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]		Reserved	
[3:0]	RO	line_count_freerun[11:8]	The line number.

4.17 New Clamp Placement Register Set

4.17.1. New Clamp Placement Enable

Address Offset: P3_0Eh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	Stip_CLPL_new	Clamp Placement select new register, 1: select new register
[6:0]	R/W	reserved	

4.17.2. New Clamp Placement Value

Address Offset: P3_0Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	STip_CLPL_MSB	Clamp Placement Value, P3_0E[0] = 1/0 : CLPL[7:0] / {CLPL[7:3],P0_04[7:5]}

4.18 Color Probing Read Back Pixel Low 2 bits Register Set

Address Offset: P3_0Ah Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	RO	Rbk_pix_lsb	ADC Read back data, high to low bit sequence: R_in[1:0], G_in[1:0], B}_in[1:0]

4.19 GPIO Register Set

4.19.1 GPE Output Enable Register

Address Offset: P1_50h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oe_GPE[7:0]	Set to 1 for GPE[7:0] output enable, else acts as input.

4.19.2 GPE Output Register

Address Offset: P1_51h Default Value: FFh

Bit	Access	Symbol	Description
[7:0]	R/W	o_GPE[7:0]	GPE [7:0] Output Value

4.19.3 GPE Status Register

Address Offset: P1_52h Default Value: 00h

Bit	Access	Symbol	Description

[7:0]	RO	i_GPE[7:0]	Report GPE [7:0] Pins current status

4.19.4 GPE Interrupt Register

Address Offset: P1_53h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO/W1C	Int_GPE[7:0] / Clr_Int_GPE[7:0]	Read to get interrupt status triggered by GPE[7:0] transition. Write 1 to clear.

4.19.5 GPE Interrupt Trigger Register

Address Offset: P1_54h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_Rise_GPE[7:0]	Enable GPE[7:0] rising edge to trigger interrupt.

4.19.6 GPE Interrupt Trigger Register

Address Offset: P1_55h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_Fall_GPE[7:0]	Enable GPE[7:0] falling edge to trigger interrupt.

4.19.7 GPE Open Drain Control Register

Address Offset: P1_56h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	OD_GPE[7:0]	Set to 1 for GPIO[n] as Open Drain output, else as Drive output.

4.19.8 GPE Debounce Control Register

Address Offset: P1_57h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_DeBnc_GPE[7:0]	Enable GPE[7:0] inputs de-bounce function.

4.19.9 GPE Debounce Control Register

Address Offset: P1_58h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	GPF_sgl_set_clr	1: Enable GPF set and clear control for per single bit
[6]	R/W	GPE_sgl_set_clr	1: Enable GPE set and clear control for per single bit
[5]	R/W	GPD_sgl_set_clr	1: Enable GPD set and clear control for per single bit
[4]	R/W	GPC_sgl_set_clr	1: Enable GPC set and clear control for per single bit
[3]	R/W	GPB_sgl_set_clr	1: Enable GPB set and clear control for per single bit
[2]	R/W	GPA_sgl_set_clr	1: Enable GPA set and clear control for per single bit
[1:0]	R/W	Debounce_sel[1:0]	Debounce selection

4.19.10 GPA Clear Register

Address Offset: P1_70h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	WO	GPA_Clr[7:0]	

4.19.11 GPB Clear Register

Address Offset: P1_71h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	WO	GPB_Clr[7:0]	

4.19.12 GPC Clear Register

Address Offset: P1_72h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	WO	GPC_Clr[7:0]	

4.19.13 GPD Clear Register

Address Offset: P1_73h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	WO	GPD_Clr[7:0]	

4.19.14 GPE Clear Register

Address Offset: P1_74h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	WO	GPE_Clr[7:0]	

4.19.15 GPA Output Enable Register

Address Offset: P1_80h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oe_GPA[7:0]	Set to 1 for GPA[7:0] output enable, else acts as input.

4.19.16 GPA Output Register

Address Offset: P1_81h Default Value: FFh

Bit	Access	Symbol	Description
[7:0]	R/W	o_GPA[7:0]	GPA[7:0] Output Value

4.19.17 GPA Status Register

Address Offset: P1_82h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	i_GPA[7:0]	Report GPA[7:0] Pins current status

4.19.18 GPA Interrupt Register

Address Offset: P1_83h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO/W1C	Int_GPA[7:0] / Clr_Int_GPA[7:0]	Read to get interrupt status triggered by GPA[7:0] transition. Write 1 to clear.

4.19.19 GPA Interrupt Trigger Register

Address Offset: P1_84h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_Rise_GPA[7:0]	Enable GPA[7:0] rising edge to trigger interrupt.

4.19.20 GPA Interrupt Trigger Register

Address Offset: P1_85h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_Fall_GPA[7:0]	Enable GPA[7:0] falling edge to trigger interrupt.

4.19.21 GPA Open Drain Control Register

Address Offset: P1_86h Default Value: 00h

Bit	Access	Symbol	Description

[7:0]	R/W	OD_GPA[7:0]	Set to 1 for GPIO[n] as Open Drain output, else as Drive output.

4.19.22 GPA Debounce Control Register

Address Offset: P1_87h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_DeBnc_GPA[7:0]	Enable GPA[7:0] inputs de-bounce function.

4.19.23 GPB Output Enable Register

Address Offset: P1_88h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oe_GPB[7:0]	Set to 1 for GPB[7:0] output enable, else acts as input.

4.19.24 GPB Output Register

Address Offset: P1_89h Default Value: FFh

Bit	Access	Symbol	Description
[7:0]	R/W	o_GPB[7:0]	GPB[7:0] Output Value

4.19.25 GPB Status Register

Address Offset: P1_8Ah Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	i_GPB[7:0]	Report GPB[7:0] Pins current status

4.19.26 GPB Interrupt Register

Address Offset: P1_8Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO/W1C	Int_GPB[7:0] / Clr_Int_GPB[7:0]	Read to get interrupt status triggered by GPB[7:0] transition. Write 1 to clear.

4.19.27 GPB Interrupt Trigger Register

Address Offset: P1_8Ch Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_Rise_GPB[7:0]	Enable GPB[7:0] rising edge to trigger interrupt.

4.19.28 GPB Interrupt Trigger Register

Address Offset: P1_8Dh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_Fall_GPB[7:0]	Enable GPB[7:0] falling edge to trigger interrupt.

4.19.29 GPB Open Drain Control Register

Address Offset: P1_8Eh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	OD_GPB[7:0]	Set to 1 for GPIO[n] as Open Drain output, else as Drive output.

4.19.30 GPB Debounce Control Register

Address Offset: P1_8Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_DeBnc_GPB[7:0]	Enable GPB[7:0] inputs de-bounce function.

4.19.31 GPC Output Enable Register

Address Offset: P1_90h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oe_GPC[7:0]	Set to 1 for GPC[7:0] output enable, else acts as input.

4.19.32 GPC Output Register

Address Offset: P1_91h Default Value: FFh

Bit	Access	Symbol	Description
[7:0]	R/W	o_GPC[7:0]	GPC[7:0] Output Value

4.19.33 GPC Status Register

Address Offset: P1_92h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	i_GPC[7:0]	Report GPC[7:0] Pins current status

4.19.34 GPC Interrupt Register

Address Offset: P1_93h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO/W1C	Int_GPC[7:0] / Clr_Int_GPC[7:0]	Read to get interrupt status triggered by GPC[7:0] transition. Write 1 to clear.

4.19.35 GPC Interrupt Trigger Register

Address Offset: P1_94h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_Rise_GPC[7:0]	Enable GPC[7:0] rising edge to trigger interrupt.

4.19.36 GPC Interrupt Trigger Register

Address Offset: P1_95h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_Fall_GPC[7:0]	Enable GPC[7:0] falling edge to trigger interrupt.

4.19.37 GPC Open Drain Control Register

Address Offset: P1_96h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	OD_GPC[7:0]	Set to 1 for GPIO[n] as Open Drain output, else as Drive output.

4.19.38 GPC Debounce Control Register

Address Offset: P1_97h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_DeBnc_GPC[7:0]	Enable GPC[7:0] inputs de-bounce function.

4.19.39 GPD Output Enable Register

Address Offset: P1_98h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oe_GPD[7:0]	Set to 1 for GPD[7:0] output enable, else acts as input.

4.19.40 GPD Output Register

Address Offset: P1_99h Default Value: FFh

Bit	Access	Symbol	Description
[7:0]	R/W	o_GPD[7:0]	GPD[7:0] Output Value

4.19.41 GPD Status Register

Address Offset: P1_9Ah Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	i_GPD[7:0]	Report GPD[7:0] Pins current status

4.19.42 GPD Interrupt Register

Address Offset: P1_9Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO/W1C	Int_GPD[7:0] / Clr_Int_GPD[7:0]	Read to get interrupt status triggered by GPD[7:0] transition. Write 1 to clear.

4.19.43 GPD Interrupt Trigger Register

Address Offset: P1_9Ch Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_Rise_GPD[7:0]	Enable GPD[7:0] rising edge to trigger interrupt.

4.19.44 GPD Interrupt Trigger Register

Address Offset: P1_9Dh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_Fall_GPD[7:0]	Enable GPD[7:0] falling edge to trigger interrupt.

4.19.45 GPD Open Drain Control Register

Address Offset: P1_9Eh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	OD_GPD[7:0]	Set to 1 for GPIO[n] as Open Drain output, else as Drive output.

4.19.46 GPD Debounce Control Register

Address Offset: P1_9Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	En_DeBnc_GPD[7:0]	Enable GPD[7:0] inputs de-bounce function.

4.19.47 GPF Output Enable Register

Address Offset: P6_20h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	oe_GPF[3:0]	Set to 1 for GPF[3:0] output enable, else acts as input.

4.19.48 GPF Output Register

Address Offset: P6_21h Default Value: FFh

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	o_GPF[3:0]	GPF[3:0] Output Value

4.19.49 GPF Status Register

Address Offset: P6_22h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	RO	i_GPF[7:0]	Report GPF[3:0] Pins current status

4.19.50 GPF Interrupt Register

Address Offset: P6_23h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	RO/W1C	Int_GPF[3:0] / Clr_Int_GPF[3:0]	Read to get interrupt status triggered by GPF[3:0] transition. Write 1 to clear.

4.19.51 GPF Interrupt Trigger Register

Address Offset: P6_24h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	En_Rise_GPF[3:0]	Enable GPF[3:0] rising edge to trigger interrupt.

4.19.52 GPF Interrupt Trigger Register

Address Offset: P6_25h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	En_Fall_GPF[3:0]	Enable GPF[3:0] falling edge to trigger interrupt.

4.19.53 GPF Open Drain Control Register

Address Offset: P6_26h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	OD_GPF[3:0]	Set to 1 for GPIO[n] as Open Drain output, else as Drive output.

4.19.54 GPF Debounce Control Register

Address Offset: P6_27h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	En_DeBnc_GPF[3:0]	Enable GPF[3:0] inputs de-bounce function.

4.19.55 GPF Clear Register

Address Offset: P6_28h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	WO	GPF_Clr[3:0]	

4.20 SPI OSD Register Set

4.20.1. SPI OSD: force alpha-blending

Address Offset: P3_80h Default Value: 40h

Bit	Access	Symbol	Description
[7]	R/W	Force_sOSD_aB_En	Enable to override the alpha value of SPI OSD with a fixed value
[6:0]	R/W	Force_sOSD_aB	Apply to background source [8:2]. (valid value: 0~64d)

4.20.4 Sprite: mask for SPI bus

Address Offset: P3_81h Default Value: 03h

Bit	Access	Symbol	Description

[7:2]		Reserved	
[1]	R/W	Sprite_BackMask_En	After the SPI read of Sprite is done, the SPI bus will be reserved to the upcoming SPI read of SPI_OSD if Sprite_BackMask_En is set to '1'.
[0]	R/W	Sprite_FrontMask_En	After the SPI read of SPI_OSD is done, the SPI bus will be reserved to the upcoming SPI read of Sprite if Sprite_FrontMask_En is set to '1'.

4.21.5 Register

Address Offset: P3_86h Default Value: 02h

Bit	Access	Symbol	Description
[7]	WO/RO	oSPI_DMA_Go/_Done	WO: oSPI DMA Trigger RO: oSPI DMA Done status
[6:4]		Reserved	
[3:2]	R/W	DMA_XferCount	DMA transfer Count when OSD_En is disable 00b: 256 bytes 01b: 384 bytes 1xb: sOSD_H_Size
[1]	R/W	HS_LeadingEdge	Check HS in leading or trailing edge
[0]	WO	sLUT_Ptr_Rst	Write '1' to reset

4.21.6 sLUT Data Port Register

Address Offset: P3_87h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	WO	sLUT_Data_Port	

4.21.7 SPI OSD: settings for display in panel

Address Offset: P3_88h Default Value: 20h

Bit	Access	Symbol	Description
[7:0]	R/W	sOSD_HStart[7:0]	Horizontal start position of SPI OSD / TWBC image

Address Offset: P3_89h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]		Reserved	
[2:0]	R/W	sOSD_HStart[10:8]	Horizontal start position of SPI OSD / TWBC image

Address Offset: P3_8Ah Default Value: 10h

Bit	Access	Symbol	Description
[7:0]	R/W	sOSD_VStart[7:0]	Vertical start position of SPI OSD / TWBC image

Address Offset: P3_8Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:2]		Reserved	
[1:0]	R/W	sOSD_VStart[9:8]	Vertical start position of SPI OSD / TWBC image

Address Offset: P3_8Ch Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	sOSD_HSize[7:0]	Horizontal size of SPI OSD / TWBC image in panel

Address Offset: P3_8Dh Default Value: 02h

Bit	Access	Symbol	Description
[7:3]		Reserved	
[2:0]	R/W	sOSD_HSize[10:8]	Horizontal size of SPI OSD / TWBC image in panel

Address Offset: P3_8Eh Default Value: E0h

Bit	Access	Symbol	Description
[7:0]	R/W	sOSD_VSize[7:0]	Vertical size of SPI OSD / TWBC image in panel

Address Offset: P3_8Fh Default Value: 01h

Bit	Access	Symbol	Description
[7:2]		Reserved	
[1:0]	R/W	sOSD_VSize[9:8]	Vertical size of SPI OSD / TWBC image in panel

4.21.8 Animation Plan: address in Flash memory

Address Offset: P3_90h Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_EmuA[7:0]	Animation plan address

Address Offset: P3_91h Default Value: 47h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_EmuA[15:8]	Animation plan address

Address Offset: P3_92h Default Value: 05h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_EmuA[23:16]	Animation plan address

4.21.9 SPI OSD: primary sLUT address in Flash Memory

Address Offset: P3_93h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_PsLUTA[7:0]	Primary sLUT address

Address Offset: P3_94h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_PsLUTA[15:8]	Primary sLUT address

Address Offset: P3_95h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_PsLUTA[23:16]	Primary sLUT address

4.21.10 SPI OSD: image address in Flash Memory

Address Offset: P3_96h Default Value: 80h

Bit	Access	Symbol	Description

[7:0]	R/W	oSPI_ImageA[7:0]	Image address

Address Offset: P3_97h Default Value: 01h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_ImageA[15:8]	Image address

Address Offset: P3_98h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_ImageA[23:16]	Image address

4.21.11 SPI OSD: Pre Occupy Register

Address Offset: P3_99h Default Value: 40h

Bit	Access	Symbol	Description
[7:0]	R/W	spi_pre_occupy	Refer to 0

4.21.12 SPI OSD: settings for 2 LUTs

Address Offset: P3_9Ah Default Value: 02h

Bit	Access	Symbol	Description
[7:0]	R/W	Switch_TC[7:0]	Horizontal or vertical count for image transition

Address Offset: P3_9Bh Default Value: 04h

Bit	Access	Symbol	Description
[7]	R/W	sOSD_Tx_En	SPI OSD image transition enable 0b: Disable (using primary sLUT only) 1b: Enable, then the left or upper image uses Primary sLUT; right or lower image uses Secondary sLUT
[6]	R/W	sOSD_Tx_in_V	SPI OSD image transition in vertical direction 0b: Transition in Horizontal direction 1b: Transition in Vertical direction
[5:4]		Reserved	
[3]	R/W	DMA_Sel_SsLUT	SPI OSD LUT DMA operation to/from 0b: Primary sLUT 1b: Secondary sLUT
[2:0]	R/W	Switch_TC[10:8]	Horizontal or vertical count for image transition

4.21.13 SPI OSD: image line jump of address in Flash memory

Address Offset: P3_9Ch Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	sOSD_LineJumpA[7:0]	Address increment for one line of OSD image in Flash memory

Address Offset: P3_9Dh Default Value: 02h

Bit	Access	Symbol	Description
[7:0]	R/W	sOSD_LineJumpA[15:8]	Address increment for one line of OSD image in Flash memory

4.21.14 SPI OSD: general settings

Address Offset: P3_9Eh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	sOSD_En	SPI OSD feature enable 0b: Allow I2C commands access and DMA transfer to sLUT RAM 1b: Allow oSPI burst 4x Read to rendering OSD
[6]	W1 / RO	sOSD_EmuTrig / Done	W1: Trigger animation process RO: Animation done status
[5]	R/W	sLUT_LoadEachFrm	0b: Do not load sLUT (via DMA operation once) 1b: Load sLUT every frame during V_BP
[4]	W1 / RO	sLUT_LoadOnce	W1: Trigger sLUT load RO: sLUT load done status
[3]	R/W	TrigLoad_PsLUT	Trigger to load Primary sLUT or not
[2]	R/W	TrigLoad_SsLUT	Trigger to load Secondary sLUT or not
[1]	R/W	oSPI_Hperf_En	oSPI high performance enable
[0]	W1	sOSD_ShdwUpdate	1. W1O to trigger shadow update when not in animation mode. 2. Auto shadow update when in animation mode (after menu load) 3. Writing to P3_9F will also trigger sOSD_ShdwUpdate

4.21.15 Animation Plan:

Address Offset: P3_9Fh Default Value: 00h

Bit	Access	Symbol	Description
[7]	W1O	sOSD_EmuExit	W1 to exist animation mode and back to fetch image (w/ or w/o sLUT) only
[6]	W1O	Jump_EmuA	W1 to Jump to oSPI_EmuA
[5:0]	R/W	Menu_PauseFrame	Pause frame number when in emulation rendering

4.21.16 TWBC Decompression:

Address Offset: P3_D0h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	TWBC_enable	Set '1' to enable the function of TWBC decompression and its output will take the place of SPI_OSD's.
[6]	R/W	TWBC_color_split_mode	Set '1' to split the SPI transmission of color data. This mode is used only when TWBC and Sprite are both enabled and SPI traffic is heavy. Because the color data of TWBC are transmitted every 4 lines with data size of sOSD_HSize times byte. If sOSD_clk and dclko_2x are 1:1 and sOSD_HSize is large enough, there will be SPI traffic confliction with Sprite.
[5:0]		Reserved	

4.21.17 TWBC Decompression: color data address in Flash memory

Address Offset: P3_D1h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	TWBC_colour_addr[7:0]	The address of TWBC color data in Flash memory.

Address Offset: P3_D2h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	TWBC_colour_addr[15:8]	The address of TWBC color data in Flash memory.

Address Offset: P3_D3h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	TWBC_colour_addr[23:16]	The address of TWBC color data in Flash memory.

4.21.18 TWBC Decompression: 4-line color data size in Flash memory

Address Offset: P3_D4h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	TWBC_colour_hsize[7:0]	The data size of TWBC color data of a vertical unit (4-line). For instance: assume sOSD_HSize = 4N = x, => the horizontal 4x4 block count of color data = (N + 2), => the data size of color data of 4-line = (N + 2) * 4 = (x + 8) bytes

Address Offset: P3_D5h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]		Reserved	
[2:0]	R/W	TWBC_colour_hsize[10:8]	The data size of TWBC color data of a vertical unit (4-line).

4.21.19 TWBC Decompression: Frame start

Address Offset: P3_D6h Default Value: 08h

Bit	Access	Symbol	Description
[7:5]		Reserved	
[4:0]	R/W	TWBC_FrameStart	Line count to assert TWBC_frame_start in each frame (bug: readback failed)

4.21.20 SPI OSD / Sprite: secondary sLUT address in Flash memory

Address Offset: P3_E0h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_SsLUTA[7:0]	Secondary sLUT address

Address Offset: P3_E1h Default Value: 04h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_SsLUTA[15:8]	Secondary sLUT address

Address Offset: P3_E2h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_SsLUTA[23:16]	Secondary sLUT address

4.21.21 Sprite: image address in Flash memory

Address Offset: P3_E3h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_SpriteA[7:0]	Sprite Image address

Address Offset: P3_E4h Default Value: C4h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_SpriteA[15:8]	Sprite Image address

Address Offset: P3_E5h Default Value: 36h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_SpriteA[23:16]	Sprite Image address

4.21.22 Sprite: image line jump of address in Flash memory

Address Offset: P3_E6h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Sprite_LineJumpA[7:0]	Address increment for one line of Sprite image in Flash memory

Address Offset: P3_E7h Default Value: 4Ah

Bit	Access	Symbol	Description
[7:0]	R/W	Sprite_LineJumpA[15:8]	Address increment for one line of Sprite image in Flash memory

4.21.23 Sprite: settings for display in panel (referenced to SPI OSD)

Address Offset: P3_E8h Default Value: 40h

Bit	Access	Symbol	Description
[7:0]	R/W	Sprite_HStart[7:0]	Horizontal start position of Sprite image

Address Offset: P3_E9h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]		Reserved	
[3:0]	R/W	Sprite_HStart[11:8]	Horizontal start position of Sprite image

Address Offset: P3_EAh Default Value: 20h

Bit	Access	Symbol	Description
[7:0]	R/W	Sprite_VStart[7:0]	Vertical start position of Sprite image

Address Offset: P3_EBh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]		Reserved	
[2:0]	R/W	Sprite_HStart[10:8]	Vertical start position of Sprite image

Address Offset: P3_ECh Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	Sprite_HSize[7:0]	Horizontal size of Sprite image in panel

Address Offset: P3_EDh Default Value: 60h

Bit	Access	Symbol	Description
[7:0]	R/W	Sprite_VSize[7:0]	Vertical size of Sprite image in panel

Address Offset: P3_EEh Default Value: F8h

Bit	Access	Symbol	Description
[7]	RO	PsLUT_Fail	BIST Fail of SRAM PsLUT
[6]	RO	SsLUT_Fail	BIST Fail of SRAM SsLUT
[5]	RO	Sprite_Fail	BIST Fail of SRAM Sprite
[4]	RO	TWBC_sram1_Fail	BIST Fail of SRAM TWBC_sram1
[3]	RO	TWBC_sram2_Fail	BIST Fail of SRAM TWBC_sram2
[2]		Reserved	
[1:0]	R/W	Sprite_VSize[9:8]	Vertical size of Sprite image in panel

4.21.24 Sprite:

Address Offset: P3_EFh Default Value: 10h

Bit	Access	Symbol	Description
[7]	R/W	Sprite_En	Set '1' to enable the function of Sprite.
[6]		Reserved	
[5]	R/W	Force_Sprite_aB_En	Enable to override the alpha value of Sprite with a fixed value
[4:0]	R/W	Force_Sprite_aB	

4.21 Power Down Control Register Set

4.23.4 ADC Power Down Control

Address Offset: P0_0Fh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	PD_SOY_	1: Power up 0: Power down
[6]	R/W	PD_Ch2_ (B)	1: Power up 0: Power down
[5]	R/W	PD_Ch1_ (G)	1: Power up 0: Power down
[4]	R/W	PD_Ch0_ (R)	1: Power up 0: Power down

4.23.5 Line Lock PLL Divider Register 2

Address Offset: P0_16h Default Value: 43h

Bit	Access	Symbol	Description
[7]	R/W	APLL_PwrDn_	1: power up, 0: power down
[5]	R/W	APLL_Reset_	1: Normal operation for RGB and SOY inputs 0: Reset Line-lock PLL

4.23.6 Output PLL Divider 3 Register

Address Offset: P0_CAh
Default Value: 03h

Bit	Access	Symbol	Description
[5]	R/W	DPLL_PowerDown_	Display PLL power down Control: 1: Display PLL power on 0: Display PLL power down

4.23.7 LVDS TX Power Down Control

Address Offset: P0_CFh Default Value: 00h

Bit	Access	Symbol	Description
[2]	R/W	LVDS_TD_PwnDn_	0:6-bit LVDS output; 1:8-bit LVDS output
[1]	R/W	LVDS_T1_PwnDn_	Set 1 to Power on LVDS channel 1
[0]	R/W	LVDS_T0_PwnDn_	Set 1 to Power on LVDS channel 0

4.22 FPLL Register Set

4.22.1 Fpll Phase Read Back LSB Register

Address Offset: P1_36h Default Value: -

Bit	Access	Symbol	Description
[7:0]	RO	Fpll_phase[7:0]	Fpll_phase

4.20.2 Fpll Phase Read Back Middle Register

Address Offset: P1_37h Default Value: -

Bit	Access	Symbol	Description
[7:0]	RO	Fpll_phase[15:8]	Fpll_phase

4.23.8 Fpll Phase Read Back MSB Register

Address Offset: P1_38h Default Value: -

Bit	Access	Symbol	Description
[7]	RO	Fpll_force_blue	
[6]	RO	Earlty_det_lost	
[5:3]	RO	Reserved	
[2:0]	RO	Fpll_phase[18:16]	Fpll_phase

4.23.9 Fpll Middle Byte Setting of Phase Difference Detect Register

Address Offset: P1_39h Default Value: 08h

Bit	Access	Symbol	Description
[7]	R/W	Phase_middle_byte[7:0]	Reference value for detect high error occurs

4.23.10 Fpll Control Register

Address Offset: P1_3Ah Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	En_fpll	En Fpll to lock input vsync
[6]	R/W	Use_fpll_vs	Use vsync locked from Fpll
[5]	R/W	En_force_blue	Before Fpll lock input vsync force frame to build-in setting frame color
[4]	R/W	Force_blue_wshd	Force blue signal with vsync shadow
[3]	RO	Reserved	
[2]	R/W	Fpll_Ignore_VS	Fpll ignore input vsync for testing
[1]	R/W	En_mask_shortVS	1: don't care shortvs
[0]	R/W	shortVS_md	0: use vs missing detect, 1: hs missing detect (include input source change)

4.23.11 Fpll Timing Constant of Loop Register

Address Offset: P1_3Bh Default Value: 22h

Bit	Access	Symbol	Description
[7]	R/W	Floop_tc[7:0]	Timing constant

4.23.12 Fpll Tolerance Error to lock Register

Address Offset: P1_3Ch Default Value: 0Ah

Bit	Access	Symbol	Description
[7]	R/W	Error_cnt[7:0]	Error count, count to some times when phase below some value, force blue state will jump to normal state

4.23.13 Fpll limitation Value of Loop LSB Register

Address Offset: P1_3Dh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	Floop_limit[7:0]	Limitation of vsync phase

4.23.14 Fpll limitation Value of Loop Middle Register

Address Offset: P1_3Eh Default Value: 80h

Bit	Access	Symbol	Description
[7]	R/W	Floop_limit[15:8]	

4.23.15 Fpll limitation Value of Loop MSB Register

Address Offset: P1_3Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	R/W	Stt_sel[1:0]	
[5:2]	RO	Reserved	
[1:0]	R/W	Floop_limit[17:16]	

4.23.16 Fpll Force Blue Control Register

Address Offset: P0_33h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3]	R/W	En_adc_swt_f_blue	Enable force blue screen when input adc source switching
[2]	R/W	En_inp_swt_f_blue	Enable force blue screen when input source switching
[1]	R/W	En_vde_detect	Enable valid vde detect
[0]	R/W	En_hs_detect	Enable hs missing detect

4.23.17 Fpll Detect Vsync 1ms Count Register

Address Offset: P0_34h Default Value: 05h

Bit	Access	Symbol	Description
[7:0]	R/W	Detv_1ms_cnt [7:0]	V Blank valid count, unit 1ms

4.23 dSPI Master Register Set

4.23.1 SPI Instruction

Address Offset: P6_60h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_Instruction	Command code to SPI NOR flash.

4.23.2 SPI_Address

Address Offset: P6_61h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_Address[7:0]	Address of data read from (or write to) SPI NOR flash.

Address Offset: P6_62h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_Address[15:8]	Address of data read from (or write to) SPI NOR flash.

Address Offset: P6_63h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_Address[23:16]	Address of data read from (or write to) SPI NOR flash.

4.23.3 SPI_SingleWr_Data

Address Offset: P6_64h Default Value: AAh

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_SingleWr_Data[7:0]	Write data used when P6_65[6:4]=100b or 110b, under non performance enhanced mode.

4.23.4 SPI Control1 Register

Address Offset: P6_65h Default Value: 00h

Bit	Access	Symbol	Description
[7]	WO/RO	SPI_Issue_Cmd / Busy	WO: Issue command RO: oSPI_Cycle, check if in busy (for polling)
[6:4]	R/W	SPI_Wr_Length[2:0]	SPI_Wr_Length: 011b=Write-2Byte(P6_63~62); 100b=Write-1Byte(P6_64); 101b=Write-3Bytes(P6_63~61); 110b=Write-4-Bytes(P6_63~61, 64); 111b=Write-3+N (P6_63~61, Buffer) Others=No-Write
[3:2]	R/W	SPI_Rd_Length[1:0]	SPI_Rd_Length: 00b=No Read; 01b=Read-1Byte; 10b=Read-3Bytes; 11b=Repeat Read.
[1]	WO/RO	Check_WIP / WIP_Fall	Write in progress(WIP), indicates whether the device is busy in program/erase/write status register progress. Write 1 to check write in progress. Read to check if WIP is done.
[0]	R/W	Wait_Burst	If set this bit 1 ,active cycle of SPI NOR flash will hold 8051 clock

4.23.5

Address Offset: P6_66h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	SPI_ReadBack_Data[7:0]/ SPI_Device_ID[7:0]/SPI_S tatus[7:0]	One of the following meanings according to different command to SPI NOR flash. 1. Read back data bit 7 to 0 2. SPI NOR flash device ID bit 7 to 0 3. SPI NOR flash status bits

4.23.6 SPI_Device_ID

Address Offset: P6_67h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	SPI_Device_ID[15:8]	SPI NOR flash device ID bit 15 to 8

4.23.7 SPI_Manufacture_ID

Address Offset: P6_68h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	SPI_Manufacture_ID[7:0]	SPI NOR flash manufacture ID

4.23.8 SPI_DMA_Address

Address Offset: P6_69h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_DMA_Address[7:0]	Address bit 7 to 0 for DMA to move data from/to.

Address Offset: P6_6Ah Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_DMA_Address[15:8]	Address bit 15 to 8 for DMA to move data from/to.

4.23.9 SPI_DMA_Count

Address Offset: P6_6Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_DMA_Count[7:0]	Bit 7 to 0 of number of bytes for DMA to move data from/to.

Address Offset: P6_6Ch Default Value: 60h

Bit	Access	Symbol	Description
[7]	WO/RO	SPI_DMA_Go/_Done	Write to trigger DMA. Read to check if DMA is done.
[6]	R/W	SPI_DMA_2_Chip	Direction bit. 0 : DMA source address to SPI NOR flash. 1 : SPI NOR flash to DMA destination address.
[5]	R/W	SPI_DMA_HolduP	If set this bit 1 ,active cycle of DMA will hold 8051 clock.
[4:0]	R/W	SPI_DMA_Count[12:8]	Bit 12 to 8 of number of bytes for DMA to move data from/to.

4.23.10 SPI Control2 Register

Address Offset: P6_6Ch Default Value: 60h

Bit	Access	Symbol	Description
[7]	WO/RO	SPI_DMA_Go/_Done	Write to trigger DMA. Read to check if DMA is done.
[6]	R/W	SPI_DMA_2_Chip	Direction bit. 0 : DMA source address to SPI NOR flash. 1 : SPI NOR flash to DMA destination address.
[5]	R/W	SPI_DMA_HolduP	If set this bit 1 ,active cycle of DMA will hold 8051 clock.
[4:0]	R/W	SPI_DMA_Count[12:8]	Bit 12 to 8 of number of bytes for DMA to move data from/to.

4.23.11

Address Offset: P6_6Dh Default Value: 00h

Bit	Access	Symbol	Description
[7:5]		Reserved	
[4]	W1O/RO	SPI_PRE_WREN / Ready	Set 1 to append WREN command prior to current command to SPI NOR flash
[3:2]		Reserved	
[1]	R/W	uSPI_4X	SPI_D width=4 in transfer data portion for uSPI_Master
[0]	R/W	dSPI_4X	SPI_D width=4 in transfer data portion for dSPI_Master

4.23.12 SPI_ToggleWr_Data

Address Offset: P6_6Eh Default Value: A5h

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_ToggleWr_Data[7:0]	Write data used when P6_65[6:4]=100b or 110b, under performance enhanced mode.

4.24 uSPI Master Register Set(shared with dSPI_Master)

4.24.1 SPI_Single Wr_Data Register

Address Offset: P6_64h Default Value: AAh

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_SingleWr_Data[7:0]	Write data used when P6_65[6:4]=100b or 110b, under non performance enhanced mode.

4.24.2 Register

Address Offset: P6_6Dh Default Value: 00h

Bit	Access	Symbol	Description
[7:5]		Reserved	
[4]	W1O/RO	SPI_PRE_WREN / Ready	Set 1 to append WREN command prior to current command to SPI NOR flash
[3:2]		Reserved	
[1]	R/W	uSPI_4X	SPI_D width=4 in transfer data portion for uSPI_Master
[0]	R/W	dSPI_4X	SPI_D width=4 in transfer data portion for dSPI_Master

4.24.3 SPI_ToggleWr_Data Register

Address Offset: P6_6Eh Default Value: A5h

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_ToggleWr_Data[7:0]	Write data used when P6_65[6:4]=100b or 110b, under performance enhanced mode.

4.25 oSPI_Master Register Set

4.25.1 oSPI_Instruction

Address Offset: P6_70h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_Instruction[7:0]	One of the following meanings according to different command to SPI NOR flash. 1. Read back data bit 7 to 0 2. SPI NOR flash device ID bit 7 to 0 3. SPI NOR flash status bits

4.25.2 oSPI_Address Register

Address Offset: P6_71h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_Address[7:0]	Address of data read from SPI NOR flash.

Address Offset: P6_72h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_Address[15:8]	Address of data read from SPI NOR flash.

Address Offset: P6_73h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_Address[23:16]	Address of data read from SPI NOR flash.

4.25.3 oSPI_SingleWr_Data Register

Address Offset: P6_74h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO/WO	oSPI_SingleWr_Data[7:0]	Write data used when P6_65[6:4]=100b or 110b, under non performance enhanced mode. Read data according to oSPI_RdMux 00b:Last write data 01b:Status/RdData/DID[7:0](device ID) 10b:DID[15:8] 11b:MID(manufacture ID)

4.25.4 oSPI Control1 Register

Address Offset: P6_75h Default Value: 00h

Bit	Access	Symbol	Description
[7]	WO/RO	SPI_Issue_Cmd / Busy	WO: Issue command RO: oSPI_Cycle, check if in busy (for polling)
[6:4]	R/W	oSPI_Wr_Length[2:0]	oSPI_Wr_Length: 011b=Write-2Byte(P6_73~72); 100b=Write-1Byte(P6_74); 101b=Write-3Bytes(P6_73~71); 110b=Write-4-Bytes(P6_73~71, 74); 111b=Write-3+N (P6_73~71, sLUT_Buffer) Others=No-Write
[3:2]	R/W	oSPI_Rd_Length[1:0]	oSPI_Rd_Length: 00b=No Read; 01b=Read-1Byte; 10b=Read-3Bytes; 11b=Repeat Read.
[1]	WO/RO	Check_WIP / WIP_Fall	Write in progress(WIP), indicates whether the device is busy in program/erase/write status register progress. Write 1 to check write in progress. Read to check if WIP is done.
[0]	R/W	oSPI_4X	oSPI_D width = 4 in transfer data portion

4.25.5 oSPI Control2 Register

Address Offset: P6_76h Default Value: 00h

Bit	Access	Symbol	Description
[7]		oSPI_DMA_Go/_DMA	See P3_86
[6]	R/W	oSPI_DMA_2_sLUT	SPI DMA direction 0b: sLUT => oSPI 1b: oSPI => sLUT
[5:4]	R/W	oSPI_RdMUX[1:0]	For oSPI_SingleWr_Data read data mux
[3:0]		Reserved	

4.25.6 oSPI_ToggleWr_Data Register

Address Offset: P7_77h Default Value: A5h

Bit	Access	Symbol	Description
[7:0]	R/W	oSPI_ToggleWr_Data[7:0]	Write data used when P6_75[6:4]=100b or 110b, under performance enhanced mode.

4.25.7 oSPI Control3 Data Register

Address Offset: P6_78h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	oSPI_H_Freq_Clk	Enable this bit to support flash with tCLKQV larger than half period of clk_sOSD.
[6]	R/W	clk_sOSD_Inv	Invert the phased clk_sOSD, which used to sample oSPI_D.
[5:0]	R/W	clk_sOSD_Sel[5:0]	Select clk_sOSD with different delay.

4.26 SPI Arbitration Register Set

4.26.1 Arbitration Setting to uSPI_Master Register

Address Offset: P6_80h Default Value: C7h

Bit	Access	Symbol	Description
[7:0]	R/W	uSPI_Arb_En[7:0]	Enable uSPI_Master to release SPI arbitration at the end of following stages of SPI protocol. uSPI_Arb_En[7] : M_RDt1 uSPI_Arb_En[6] : M_RDt2 uSPI_Arb_En[5] : M_RDt3 uSPI_Arb_En[4] : M_WDt1 uSPI_Arb_En[3] : M_W_Al uSPI_Arb_En[2] : M_W_Am uSPI_Arb_En[1] : M_W_Ah uSPI_Arb_En[0] : M_WCmd

4.26.2 Arbitration Setting to dSPI_Master Register

Address Offset: P6_81h Default Value: 07h

Bit	Access	Symbol	Description
[7:3]	R/W	dSPI_Arb_En[4:0]	Allow dSPI_Master to release SPI arbitration at the end of following stages of SPI protocol. uSPI_Arb_En[4] : M_RDt2 uSPI_Arb_En[3] : M_RDt3 uSPI_Arb_En[2] : M_WDt1 uSPI_Arb_En[1] : M_W_Ah, M_W_Am, M_W_Al uSPI_Arb_En[0] : M_WCmd
[2:0]	R/W	DMA_Burst_Size_Sel[2:0]	Burst Size selection for packetized DMA (in Bytes) 000b=2, 001b=4, 010b=6, 011b=8, 100b=10, 101b=12, 110b=14, 111b=16

4.26.3 Global Arbitration Register

Address Offset: P6_82h Default Value: 0Ch

Bit	Access	Symbol	Description
[7:4]		Reserved	
[3]	R/W	Preserve_Arb_4sOSD_En	Preserve SPI arbitration for SPI_OSD at the end of Sprite.
[2]	R/W	Round_Robin_En	When uSPI_Master & dSPI_Master request SPI arbitration simultaneously, the SPI arbitrator will grant one of them according to Round_Robin_En setting. 1b : Grant the other one rather than the one accessed the SPI bus recently. 0b : uSPI_Master always win the SPI arbitration.
[1]	RO	HP_Extra8T	To indicate whether all SPI_Masters getting into performance enhance mode or not.
[0]	R/W	SPI_HPerf_En	Enable performance enhance mode. Note: 1. Set to 1 only if uSPI_4X = dSPI_4X = oSPI_4X = 1, and only SPI instruction 'EB' is allowed. 2. Need to polling HP_Extra8T

4.26.4 Arbitration Status Register

Address Offset: P6_83h Default Value: 00h

Bit	Access	Symbol	Description
[7:3]		Reserved	
[2]	RO/W1C	H_align_fail	To indicate whether SPI arbitrator grant oSPI_Master in time.
[1]	RO	spi_pre_mask_underflow	To indicate whether spi_pre_master (P6_99) has been set too large under current panel timing.
[0]	RO/W1C	spi_pre_mask_overlapped	To indicate whether spi_pre_mask rising during transmission Sprite, if spi_pre_mask_overlapped == 1'b1, Preserve_Arb_4sOSD_En must set to 1'b1 to eliminate image artifacts.

4.27 Internal Pattern Register Set

4.27.1 Pattern Width Register

Address Offset: 98h Default Value: 3Bh

Bit	Access	Symbol	Description
[7:0]	R/W	PATT_BAR_WIDTH[7:0]	

4.27.2 Pattern Color Gradient & Dithering Mode Register

Address Offset: 9Ch Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	CLRGRDT[3:0]	When EFMCLR are enabled, CLRGRDT may set color gradient at pattern 2, 3 ,4, 5
[3:2]	RO	Reserved	
[1:0]	R/W	Patt_Bar_LSB_Sel[1:0]	Select the gray LSB value in Gray bar ramp

4.27.3 Frame Color Configuration Register

Address Offset: 9Dh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLRRED	8 bits of red color depth for frame color.

Address Offset: 9Eh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLRGRN	8 bits of green color depth for frame color.

Address Offset: 9Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLRBLU	8 bits of blue color depth for frame color.

4.28 Touch Panel Control Register Set

Address Offset: P3_20 Default Value: 6Ch

Bit	Access	Symbol	Description

[7:5]	R/W	SAR0_Freq_Sel	Select frequency of SAR0_Clk (0:clk disable, 1~7 : 2^2 ~ 2^8) (Note: SAR_ADC is limited up to 4MHz)
[4:2]	R/W	SAR0_StableMask	Available if TP_CPU_Ctrl=1
[1]	R/W	PDn_SAR0_	Power down of SAR0 (low active) 0: power down 1: power on
[0]	R/W	SAR0_DeBounce	Available if TP_CPU_Ctrl=1

Address Offset: P3_21 Default Value: 50h

Bit	Access	Symbol	Description
[7:4]		Reserved	
[3:0]	R/W	SAR0_Threshold [3:0]	Threshold value of average value

Address Offset: P3_22 Default Value: 20h

Bit	Access	Symbol	Description
[7:0]	R/W	SAR0_Threshold[11:4]	Threshold value of average value

Address Offset: P3_23 Default Value: 6Ch

Bit	Access	Symbol	Description
[7:5]	R/W	SAR1_Freq_Sel	Select frequency of SAR1_Clk (0:clk disable, 1~7 : 2^2 ~ 2^8) (Note: SAR_ADC is limited up to 4MHz)
[4:2]	R/W	SAR1_StableMask	Available if TP_CPU_Ctrl=1
[1]	R/W	PDn_SAR1_	Power down of SAR1
[0]	R/W	SAR1_DeBounce	Available if TP_CPU_Ctrl=1

Address Offset: P3_24 Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	SAR1_RITm_Value[3:0]	Real time value of SAR1 ADC

Address Offset: P3_25 Default Value: 20h

Bit	Access	Symbol	Description
[7:0]	R/W	SAR1_Threshold	Threshold value of average value

Address Offset: P3_27 Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	SAR01_Ltch_Value[7:0]	

Address Offset: P3_28 Default Value: 0Fh

Bit	Access	Symbol	Description
[7:6]	R/W	SAR0_Src_Sel	SAR0 ADC mux: 00/01/1x SAR0 0/1/2
[5:4]	R/W	SAR1_Src_Sel	SAR1 ADC mux: 00/01/1x SAR1 0/1/2
[3:0]	RO	SAR0_RITm_Value[3:0]	Real time value of SAR0 ADC

Address Offset: P3_29 Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	SAR0_RITm_Value [11:4]	Real time value of SAR0 ADC

Address Offset: P3_2A Default Value: 00h

Bit	Access	Symbol	Description
[7:6]		Reserved	
[5]	R/W	Mask_ReIntr	Mask interrupt of Pen Release
[4]	R/W	Mask_PDIntr	Mask interrupt of Pen Down
[3:0]	RO	TP_Value[3:0]	Available if TP_CPU_Ctrl=1

Address Offset: P3_2B Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	RO	TP_Value [11:4]	Available if TP_CPU_Ctrl=1

Address Offset: P3_2C Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	TP_Seperate_XY	Available if TP_CPU_Ctrl=1
[6]	R/W	TP_Rdbk_Sel_Y	Available if TP_CPU_Ctrl=1
[5]	RO	ReIntr_I	Latch Pen Release interrupt
[4]	RO	PDIntr_I	Latch Pen Down interrupt
[3]	R/W	TP_CPU_Ctrl	If 1, let CPU control touch panel; otherwise, state machine take over.
[2:0]	R/W	TP_Measure[2:0]	If TP_CPU_Ctrl =1, 000 disable 100/001/010 PenDown/X/Y (4-wire). Otherwise, read back real time TP_Measure status.

Address Offset: P3_2D Default Value: 10h

Bit	Access	Symbol	Description
[7]	RO	TP_PDD_Result_I	Latch Pen Down
[6]	RO	TP_Move_I	Latch Pen Move
[5]		Reserved	
[4]	R/W	TP_PSEN	Power down touch panel part except SAR ADC
[3]	RO	TP_PDD_Result	Pen Down status
[2]	RO	TP_Move	Pen Move status
[1]	R/W	TP_PDD_Trig_En	Trigger Pen down interrupt
[0]	R/W	TP_Move_Trig_En	Trigger Pen Move interrupt

Address Offset: P3_2E Default Value: 21h

Bit	Access	Symbol	Description
[7]		Reserved	
[6:4]	R/W	TP_Measure_Y[2:0]	Configuration of Measure Y
[3]		Reserved	
[2:0]	R/W	TP_Measure_X[2:0]	Configuration of Measure X

Address Offset: P3_2F Default Value: 04h

Bit	Access	Symbol	Description
[7:5]	R/W	TP_Freq_Sel[2:0]	Touch panel clock divider(0:clk_4timer, 1~7 : 2^2 ~ 2^8)
[4]		Reserved	
[3]	R/W	SAR0_Clk_Inv	Invert clock of SAR0 ADC
[2:0]	R/W	TP_Measure_PDD[2:0]	Configuration of Measure PDD

Address Offset: P3_31 Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	TP_Measure_Gap	Gap among switching TP_measure

Address Offset: P3_3A Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R	TPY_D0[3:0]	Value of 1st Measure Y
[3:0]	R	TPX_D0[3:0]	Value of 1st Measure X

Address Offset: P3_3B Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPX_D0[11:4]	Value of 1st Measure X

Address Offset: P3_3C Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPY_D0[11:4]	Value of 1st Measure Y

Address Offset: P3_3D Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R	TPY_AVG[3:0]	Average value of Measure Y
[3:0]	R	TPX_AVG[3:0]	Average value of Measure X

Address Offset: P3_3E Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPX_AVG[11:4]	Average value of Measure X

Address Offset: P3_3F
Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPY_AVG[11:4]	Average value of Measure Y

Address Offset: P3_40 Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	PDD_Measure_Gap [7:0]	Gap between Pen down and Measurement

Address Offset: P3_41 Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Measure Gap[7:0]	Gap among each measure X/Y

Address Offset: P3_42
Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPX_D1_diff[7:0]	Difference value of 2nd Measure X

Address Offset: P3_43 Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPX_D2_diff[7:0]	Difference value of 3rd Measure X

Address Offset: P3_44
Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPX_D3_diff[7:0]	Difference value of 4th Measure X

Address Offset: P3_45 Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPX_D4_diff[7:0]	Difference value of 5th Measure X

Address Offset: P3_46 Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPX_D5_diff[7:0]	Difference value of 6th Measure X

Address Offset: P3_47 Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPX_D6_diff[7:0]	Difference value of 7th Measure X

Address Offset: P3_48 Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPX_D7_diff[7:0]	Difference value of 8th Measure X

Address Offset: P3_49 Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPY_D1_diff[7:0]	Difference value of 2nd Measure Y

Address Offset: P3_4A Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPY_D2_diff[7:0]	Difference value of 3rd Measure Y

Address Offset: P3_4B Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPY_D3_diff[7:0]	Difference value of 4th Measure Y

Address Offset: P3_4C Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPY_D4_diff[7:0]	Difference value of 5th Measure Y

Address Offset: P3_4D Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPY_D5_diff[7:0]	Difference value of 6th Measure Y

Address Offset: P3_4E Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPY_D6_diff[7:0]	Difference value of 7th Measure Y

Address Offset: P3_4F Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TPY_D7_diff[7:0]	Difference value of 8th Measure Y

Address Offset: P3_50 Default Value: 05h

Bit	Access	Symbol	Description
[7:0]	R/W	TPX_Bouncing_Threshold[7:0]	Bouncing threshold of Measure X 8'h00: no bouncing detection

Tune it depends on bouncing statistic counter (P3_53/74).

Address Offset: P3_51 Default Value: 05h

Bit	Access	Symbol	Description
[7:0]	R/W	TPY_Bouncing_Threshold[7:0]	Bouncing threshold of Measure Y 8'h00: no bouncing detection

Tune it depends on bouncing statistic counter (P3_53/74).

Address Offset: P3_52 Default Value: 00h

Bit	Access	Symbol	Description
[7:5]		Reserved	
[4]	R/W	TP_Boucing_Clear	Reset statistic counter of bouncing
[3:2]	R/W	TPY_Time[1:0]	(0:2^1, 1~2 : 2^2 ~ 2^3) Times of measure Y

[1:0]	R/W	TPX_Time[1:0]	(0:2^1, 1~2 : 2^2 ~ 2^3) Times of measure X

More times do more accurate average value while stop at the same point.

Address Offset: P3_53 Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TP_Bouncing_cnt[15:8]	Bouncing Statistic Counter

This statistical counter is for detect if our configuration is appropriate or too aggressive.

Address Offset: P3_54 Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R	TP_Bouncing_cnt[7:0]	Bouncing Statistic Counter

Address Offset: P3_55 Default Value: 22h

Bit	Access	Symbol	Description
[7:4]	R/W	Pen_Down_Time[3:0]	Times of measure pen down
[3:0]	R/W	Pen_Release_Time [3:0]	Times of measure pen release 4'h0: no pen release interrupt

4.29 Digital PWM Register Set

4.29.1 PWM23 Control Register – 1

Address Offset: P1_60h Default Value: 02h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5]	R/W	PFM2_Mode	Enable PFM mode
[4]	R/W	PFM3_Mode	Enable PFM mode
[3:0]	R/W	PWM2_DeadTimer_sel	When PWM2_DeadTimer[2:1]==00b, shutdown immediately

4.29.2 PWM23 Control Register - 2

Address Offset: P1_61h Default Value: 02h

Bit	Access	Symbol	Description
[7]	R/W	PWM2_avg_en	Enable PWM2 averaging successive inputs
[6]	R/W	PWM2_avg_mode	PWM2 average mode, 0b: average 2, 1b: average 4
[5]	R/W	PWM3_avg_en	Enable PWM3 averaging successive inputs
[4]	R/W	PWM3_avg_mode	PWM3 average mode, 0b: average 2, 1b: average 4
[3:0]	R/W	PWM3_DeadTimer_sel	When PWM3_DeadTimer[2:1]==00b, shutdown immediately

4.29.3 PWM2 Control Register

Address Offset: P1_62h Default Value: 42h

Bit	Access	Symbol	Description
[7]	R/W	PWM2_En	Enable PWM2
[6]	R/W	PWM2_Track	0b: Assign mode, 1b: Track mode;
[5:4]	R/W	PWM2_Freq_Sel	00b~11b: divided 1/2/4/8
[3:2]	R/W	PWM2_Step_Sel	00b~11b: slower -> faster tracking

[1]	R/W	PWM2_FTClk_en	Enable Fractional Fine Tune
[0]	R/W	PWM2_4bits_mode	Enable 4 bits mode, 0b: 1 bit, 1b: 4 bit

4.29.4 PWM2 Duty Register

Address Offset: P1_63h Default Value: 05h

Bit	Access	Symbol	Description
[7:0]	R/W	PWM2_High[7:0]	00~FFh means 1/PWM2_Period ~ 256/PWM2_Period; PWM2_En=0 means 0/PWM2_Period;

4.29.5 PWM2 Period Register

Address Offset: P1_64h Default Value: 1Ah

Bit	Access	Symbol	Description
[7:0]	R/W	PWM2_Period[7:0]	PWM2 period

4.29.6 PWM3 Control Register

Address Offset: P1_65h Default Value: 42h

Bit	Access	Symbol	Description
[7]	R/W	PWM3_En	Enable PWM3
[6]	R/W	PWM3_Track	0b: Assign mode, 1b: Track mode;
[5:4]	R/W	PWM3_Freq_Sel	00b~11b: divided 1/2/4/8
[3:2]	R/W	PWM3_Step_Sel	00b~11b: slower -> faster tracking
[1]	R/W	PWM3_FTClk_en	Enable Fractional Fine Tune
[0]	R/W	PWM3_4bits_mode	Enable 4 bits mode, 0b: 1 bit, 1b: 4 bit

4.29.7 PWM3 Duty Register

Address Offset: P1_66h Default Value: 05h

Bit	Access	Symbol	Description
[7:0]	R/W	PWM3_High[7:0]	00~FFh means 1/PWM3_Period ~ 256/PWM3_Period; PWM3_En=0 means 0/PWM3_Period;

4.29.8 PWM3 Period Register

Address Offset: P1_67h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	PWM3_Period[7:0]	PWM3 period

4.29.9 PWM23 Control Register – 3

Address Offset: P1_68h Default Value: 16h

Bit	Access	Symbol	Description
[7:6]	RO		Reserved
[5]	R/W	PWM23_Rd_Track	P1_63h/66h read back value as: 1b:tracked value; 0b:programmed PWM2/3_High[7:0]
[4]	R/W	PWM23_ShutDn_En	Enable over current protection

[3:2]	R/W	PWM3_TurnAround	CCFL full bridge skew
[1:0]	R/W	PWM23_Tip_Ahead	Tip ahead 00b:16, 01b:32, 10b:48, 11b:64

4.29.10 PWM2 Range Register

Address Offset: P1_69h Default Value: 08h

Bit	Access	Symbol	Description
[7:0]	R/W	PWM2_High_Min	Lower limit of PWM2 duty

Address Offset: P1_6Ah Default Value: 60h

Bit	Access	Symbol	Description
[7:0]	R/W	PWM2_High_Max	Upper limit of PWM2 duty

4.29.11 PWM3 Range Register

Address Offset: P1_6Bh Default Value: 08h

Bit	Access	Symbol	Description
[7:0]	R/W	PWM3_High_Min	Lower limit of PWM3 duty

Address Offset: P1_6Ch Default Value: 60h

Bit	Access	Symbol	Description
[7:0]	R/W	PWM3_High_Max	Upper limit of PWM3 duty

4.29.12 PWM2 Trace Register

Address Offset: P1_6Dh Default Value: 3Ch

Bit	Access	Symbol	Description
[7:4]	R/W	PWM2_Threshold	Trace threshold
[3:0]	R/W	PWM2_Target	Target of trace level

4.29.13 PWM3 Trace Register

Address Offset: P1_6Eh Default Value: 3Ch

Bit	Access	Symbol	Description
[7:4]	R/W	PWM3_Threshold	Trace threshold
[3:0]	R/W	PWM3_Target	Target of trace level

4.29.14 PWM23 Read Value Register

Address Offset: P1_6Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	VFB[3:0]	PWM2 ADC value
[3:0]	RO	VFBL[3:0]	PWM3 ADC value
[3:0]	R/W	PWM2_wgt3[3:0]	

4.29.15 PWM2 Phase Error Read Back Register

Address Offset: P1_75h Default Value: 86h

Bit	Access	Symbol	Description
[7:5]	R/W	Reserved	
[4:0]	R/W	PWM2_Error[[4:0]	PWM2 Error

4.29.16 PWM3 Phase Error Read Back Register

Address Offset: P1_76h Default Value: 45h

Bit	Access	Symbol	Description
[7:5]	R/W	Reserved	
[4:0]	R/W	PWM3_Error[4:0]	PWM3 Error

4.29.17 PWM2 Delat Period Register

Address Offset: P1_77h Default Value: 06h

Bit	Access	Symbol	Description
[7:0]	R/W	PWM2_dltprd	PWM2 delta shift period for PFM

4.29.18 PWM3 Delat Period Register

Address Offset: P1_78h Default Value: 06h

Bit	Access	Symbol	Description
[7:0]	R/W	PWM3_dltprd	PWM3 delta shift period for PFM

4.29.19 PWM23 PI Control Register

Address Offset: P1_79h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	PWM2_pi_en	Enable PWM2 pi control
[6]	RO	Reversed	
[5]	WO	PWM2_dlt_md	Delta shift mode for PFM
[4]	R/W	PWM2_dlt_en	Enable delta shift for PFM mode
[3]	R/W	PWM3_pi_en	Enable PWM3 pi control
[2]	R/W	Reversed	
[1]	R/W	PWM3_ dlt _md	Delta shift mode for PFM
[0]	R/W	PWM3_dlt_en	Enable delta shift for PFM mode

4.29.20 PWM2 PI Loop Timing Constant Control Register

Address Offset: P1_7Ah Default Value: 24h

Bit	Access	Symbol	Description
[7:4]	R/W	PWM2_p_loop_tc[3:0]	PWM2 p control timing constant, higher value means tracking slower
[3:0]	R/W	PWM2_i_loop_tc[3:0]	PWM2 i control timing constant, higher value means tracking slower

4.29.21 PWM3 PI Loop Timing Constant Control Register

Address Offset: P1_7Bh Default Value: 24h

Bit	Access	Symbol	Description
[7:4]	R/W	PWM3_p_loop_tc[3:0]	PWM3 p control timing constant, higher value means tracking slower
[3:0]	R/W	PWM3_i_loop_tc[3:0]	PWM3 i control timing constant, higher value means tracking slower

4.29.22 PWM2 PI Loop Limitation Register

Address Offset: P1_7Ch Default Value: 02h

Bit	Access	Symbol	Description
[7:0]	R/W	PWM2_loop_limit[7:0]	Limitation of PWM2 error correction

4.29.23 PWM3 PI Loop Limitation Register

Address Offset: P1_7Dh Default Value: 02h

Bit	Access	Symbol	Description
[7:0]	R/W	PWM3_loop_limit[7:0]	Limitation of PWM3 error correction

4.29.24 PWM2/3 Shutdown and Tip Control Register

Address Offset: P1_7Eh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	PWM2_sd_rst	Enable PWM2 shutdown reset
[7:5]	R/W	Reserved	
[5]	R/W	PWM2_Tip_Ahd_0	Force PWM2 tip ahead to zero
[3]	R/W	PWM3_sd_rst	Enable PWM3 shutdown reset
[3:1]	R/W	Reserved	
[0]	R/W	PWM3_Tip_Ahd_0	Force PWM3 tip ahead to zero

4.29.25 PWM2/3 Tip Selecction Register

Address Offset: P1_7Fh Default Value: 44h

Bit	Access	Symbol	Description
[6:4]	R/W	PWM2_Tip_Sel[2:0]	PWM2 Tip Select, 0~7: div 2^4/5/6/7/8/9/10/11
[2:0]	R/W	PWM3_Tip_Sel[2:0]	PWM3 Tip Select, 0~7: div 2^4/5/6/7/8/9/10/11

4.30 Infra-Red Register Set

4.30.1 IR Sampleing Tick Register

Address Offset: P1_40h Default Value: 10h

Bit	Access	Symbol	Description
[7:0]	R/W	IR_Tick[7:0]	Sampling Tick LSB byte (Unit: XCLK is 27MHz): NEC mode: 560 s (3B10h); Philips RC5 mode: 900 s (5EECh)

Address Offset: P1_41h Default Value: 3Bh

Bit	Access	Symbol	Description
[7:0]	R/W	IR_Tick[15:8]	Sampling Tick MSB byte.

4.30.2 IR Stream 1~4 Register (when IR_Counter_Mode=0)

Address Offset: P1_42h~45h Default Value: xxxxxxxxh

Bit	Access	Symbol	Description
[7:0] x4	RO	IR_Stream[0..31]	Decoded IR stream (packet) stored in P1_42h~45h The first received bit is IR_Stream[0], then the next IR_Stream[1], …. and the last available bit is IR_Stream[31] if packet that long. IR_Stream[7:0] in P1_42, IR_Stream[15:8] in P1_43, IR_Stream[23:16] in P1_44, IR_Stream[31:24] in P1_45;

4.30.3 IR Duration 1~3 Register (when IR_Counter_Mode=1)

Address Offset: P1_42h~44h Default Value: xxxxxxh

Bit	Access	Symbol	Description
[7:0] x3	RO	IR_Duration[0..21] (P1_44<7:6> are 00b)	The duration (count in XCLK) of input IR. When IR protocol is not supported, F/W can use this counter result and IR interrupt to decode.

4.30.4 IR Repeat Block Setting

Address Offset: P1_46h Default Value: 9Ah

Bit	Access	Symbol	Description
[7]	R/W	IR_LagRepeat_Block_En	Enable delay Repeat Block only in NEC mode
[6:0]	RO	IR_LagRepeat_Due[6:0] (*16 *IR_Tick)	unit: 16*IR_Tick default Enable Repeat Block after235ms

4.30.5 IR Stream 1 Register

Address Offset: P1_47h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	IR_En	Enable IR Decoder.
[6]	R/W	IR_Counter_Mode	Set to 0 for supported IR protocols; Set to 1 for monitoring IR transition duration (count in XCLK)
[5:4]	R/W	IR_Mode[1:0]	IR Decoder Mode: 00: NEC mode; 01: Philips RC5 mode; 1X: Sony mode
[3]	R/W	IR_Invert	Invert IR1 input to IR Decoder.
[2]	RO	IR_Value	Current IR value (high or low)
[1]	RO	IR_Overflow	IR duration counter overflow if get 1, then the
[0]	RO	IR_Repeat	Getting 1 indicates the current IR packet is Repeat.

4.30.6 IR Stream 1 Register

Address Offset: P1_47h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	IR_En	Enable IR Decoder.
[6]	R/W	IR_Counter_Mode	Set to 0 for supported IR protocols; Set to 1 for monitoring IR transition duration (count in XCLK)
[5:4]	R/W	IR_Mode[1:0]	IR Decoder Mode: 00: NEC mode; 01: Philips RC5 mode; 1X: Sony mode
[3]	R/W	IR_Invert	Invert IR1 input to IR Decoder.
[2]	RO	IR_Value	Current IR value (high or low)
[1]	RO	IR_Overflow	IR duration counter overflow if get 1, then the
[0]	RO	IR_Repeat	Getting 1 indicates the current IR packet is Repeat.

4.30.7 IR Interrupt Key Register

Address Offset: P1_49h Default Value: 9Ah

Bit	Access	Symbol	Description
[7:0]	R/W	IR_Int_Key[7:0]	

Address Offset: P1_4Ah Default Value: 9Ah

Bit	Access	Symbol	Description
[7:0]	R/W	IR_Int_Key[15:8]	

Address Offset: P1_4Bh Default Value: 9Ah

Bit	Access	Symbol	Description
[7:0]	R/W	IR_Int_Key[23:16]	

Address Offset: P1_4Ch Default Value: 9Ah

Bit	Access	Symbol	Description
[7:0]	R/W	IR_Int_Key[31:24]	

4.31 UART0 Register Set

4.31.1 Receiver Buffer / Transmit Holding / Divisor Latch Low Register

Address Offset: P4_00h Default Value:00h

Bit	Access	Symbol	Description
[7:0]	R	RBR	Data byte received on the serial input port (sin) in UART mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.
[7:0]	W	THR	Data to be transmitted on the serial output port (sout) in UART mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFOs are disabled (FCR[0]=0) and THRE is set, writing a single character to THR clears the THRE. Any additional writes to THR before the THRE is set again causes the THR data to be overwritten. If FIFOs are enabled (FCR[0]=1) and THRE is set, 16 characters of data may be written to THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.
[7:0]	R/W	DLL	Lower 8 bits of a 16 bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero); The output baud rate is equal to the serial clock (pclk) frequency divided by sixteen times the value of the baud rate divisor, as follows : baud rate = (serial clock freq)/ (16*divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest DW_apb_uart clock should be allowed to pass before transmitting or receiving data.

4.31.2 Divisor Latch High Register

Address Offset: P4_04h Default Value:00h

Bit	Access	Symbol	Description

[7:0]	R/W	DLH	Upper 8 bits of a 16 bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (pclk) frequency divided by sixteen times the value of the baud rate divisor, as follows : baud rate = (serial clock freq)/ (16*divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest DW_apb_uart clock should be allowed to pass before transmitting or receiving data.

4.31.3 Interrupt Enable Register

Address Offset: P4_04h Default Value:00h

Bit	Access	Symbol	Description
[7]	R/W	PTIME	This is used to enable/disable the generation of THRE Interrupt. 0 = disabled 1 = enabled
[6:4]		Reserved	
[3]	R/W	EDSSI	Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0 = disabled 1 = enabled
[2]	R/W	ELSI	Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0 = disabled 1 = enabled
[1]	R/W	ETBEI	Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0 = disabled 1 = enabled
[0]	R/W	ERBFI	Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if FIFOs enabled). This are the second highest priority interrupts. 0 = disabled 1 = enabled

4.31.4 Interrupt Identity Register

Address Offset: P4_08h Default Value:01h

Bit	Access	Symbol	Description
[7:6]	R	FIFOSE	FIFOs Enabled. This is used to indicate whether the FIFOs are enabled or disabled. 00 = disabled 11 = enabled
[5:4]		Reserved	

[3:0]	R	IID	Interrupt ID. This indicates the highest priority pending interrupt which can be one of the following types : 0000 = modem status 0001 = no interrupt pending 0010 = THR empty 0100 = received data available 0110 = receiver line status 0111 = busy detect 1100 = character timeout Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

4.31.5 FIFO Control Register

Address Offset: P4_08h Default Value:00h

Bit	Access	Symbol	Description
[7:6]	W	RT	RCVR Trigger. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. The following trigger levels are supported : 00 = 1 character in the FIFO 01 = FIFO 1/4 full 10 = FIFO 1/2 full 11 = FIFO 2 less than full
[5:4]W	W	TET	This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported : 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO 1/4 full 11 = FIFO 1/2 full
[3]		Reserved	
[2]	W	XFIFOR	XMIT FIFO Reset.. This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self -clearing'. It is not necessary to clear this bit.
[1]	W	RFIFOR	RCVR FIFO Reset.. This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self –clearing'. It is not necessary to clear this bit.
[0]	W	FIFOE	FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

4.31.6 Line Control Register

Address Offset: P4_0Ch Default Value:00h

Bit	Access	Symbol	Description
[7]	R/W	DLAB	Divisor Latch Access Bit. It is writable only when UART is not busy (USR[0] is zero). This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
[6]	R/W	BC	Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic o) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
[5]		Reserved	

[4]	R/W	EPS	Even Parity Select. It is writable only when UART is not busy (USR[0] is zero); This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.
[3]	R/W	PEN0	Parity Enable. It is writable only when UART is not busy (USR[0] is zero). This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0 = parity disabled 1 = parity enabled
[2]	R/W	STOP	Number of stop bits. It is writable only when UART is not busy (USR[0] is zero). This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted, Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0 = 1 stop bit 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
[1:0]	R/W	DLS	Data Length Select. It is writable only when UART is not busy (USR[0] is zero). This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected as follows : 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits

4.31.7 Modem Control Register

Address Offset: P4_10h Default Value:00h

Bit	Access	Symbol	Description
[7:5]	R/W	Reserved	
[4]	R/W	LB	LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode, data on the sout line is held high, while serial data output is loop back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control output (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally
[3:0]		Reserved	

4.31.8 Line Status Register

Address Offset: P4_14h Default Value:60h

Bit	Access	Symbol	Description
[7]	R	RFE	Receiver FIFO Error bit. This bit is only relevant when FIFOs are enabled (FCR[0] set to one). This is used to indicated if there is at least one parity error, framing error, or break indication in the FIFO. 0 = no error in RX FIFO 1 = error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.

[6]	R	TEMT	Transmitter Empty bit. If FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
[5]	R	THRE	Transmit Holding Register Empty bit. If THRE mode is disable (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also cause a THRE Interrupt to occur, if the THRE Interrupt is enabled. If IER[7] set to one and FCR[0] set to one respectively, the functionality is switched to indicated the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
[4]	R	BI	Break Interrupt bit. This is used to indicated the detection of a break sequence on the serial input data. It is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input cause one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
[3]	R	FE	Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no framing error 1 = framing error Reading the LSR clears the FE bit.
[2]	R	PE	Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no parity error 1 = parity error Reading the LSR clears the PE bit.
[1]	R	OE	Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read, In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. O = no overrun error 1= overrun error Reading the LSR clears the OE bit

[0]	R	DR	Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0 = no data ready 1 = data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

4.31.9 Modem Status Register

Address Offset: P4_18h Default Value:00h

Bit	Access	Symbol	Description
[7]	R	DCD	Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0 = dcd_n input is de-asserted (logic 1) 1 = dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2). **This bit is always zero.**
[6]	R	RI	Ring Indicator. This is used to indicate the current state of the modem control line ri_n. This bit is the complement if ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0 = ri_n input is de-asserted (logic 1) 1 = ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1). **This bit is always zero.**
[5]	R	DSR	Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. 0 = dsr_n input is de-asserted (logic 1) 1 = dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR). **This bit is always zero.**
[4]	R	CTS	Clear to Send. This is used to indicate the current state of the modem control line cts_n. This bit is the complement if cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. 0 = cts_n input is de-asserted (logic 1) 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4]=1), CTS is the same as MCR[1] (RTS) **This bit is always zero.**
[3]	R	DDCD	Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0 = no change on dcd_n since last read of MSR 1 = change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4]=1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted. **This bit is always zero.**

[2]	R	TERI	Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active-low to an inactive high state) has occurred since the last time the MSR was read. 0 = no change on ri_n since last read of MSR. 1 = change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4]=1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low. **This bit is always zero.**
[1]	R	DDSR	Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0 = no change on dsr_n since last read of MSR 1 = change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4]=1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted. **This bit is always zero.**
[0]	R	DCTS	Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0 = no change on cts_n since last read of MSR 1 = change on cts_n since last read of MSR Reading the MSR clears DCTS bit. In Loopback Mode (MCR[4]=1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted. **This bit is always zero.**

4.31.10 Scratchpad Register

Address Offset: P4_1Ch Default Value:00h

Bit	Access	Symbol	Description
[7:0]	R/W	Scratchpad Register	This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart.

4.31.11 Shadow Receive Buffer Register

Address Offset: P4_30h~P4_6Ch Default Value:00h

Bit	Access	Symbol	Description
[7:0]	R	Shadow Receive Buffer Register	This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs.

4.31.12 Shadow Transmit Holding Register

Address Offset: P4_30h~P4_6Ch Default Value:00h

Bit	Access	Symbol	Description
[7:0]	W	Shadow Transmit Holding Register	This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFOs are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFOs are enabled (FCR[0] set to one) and THRE is set, 16 characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data begin lost.

4.31.13 FIFO Access Register

Address Offset: P4_70h Default Value:00h

Bit	Access	Symbol	Description
[7:1]	R/W	Reserved	
[0]	R/W	FIFO Access Register	This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not enabled it allows the RBR to be written by the master and the THR to be read by the master. 0 = FIFO access mode disable 1 = FIFO access mode enabled Notes, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty.

4.31.14 Transmit FIFO Register

Address Offset: P4_74h Default Value:00h

Bit	Access	Symbol	Description
[7:0]	R	Transmit FIFO Read	Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not enabled, reading this register gives the data in the THR.

4.31.15 Receive FIFO Write Register

Address Offset: P4_78h Default Value:00h

Bit	Access	Symbol	Description
[7:0]	W	RFWD	Receive FIFO write Data. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not enabled, the data that is written to the RFWD is pushed into the RBR.

4.31.16 UART Status Register

Address Offset: P4_7Ch Default Value:06h

Bit	Access	Symbol	Description
[7:5]	R/W	Reserved	
[4]	R	RFF	Receive FIFO full. This is used to indicate that the receive FIFO is completely full. 0 = Receive FIFO not full 1 = Receive FIFO full This bit is cleared when the RX FIFO is no longer full.
[3]	R	RFNE	Receive FIFO Not Empty. This is used to indicate that the receive FIFO contains one or more entries. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty
[2]	R	TFE	Transmit FIFO Empty. This is used to indicate that the transmit FIFO is completely empty. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
[1]	R	TFNF	Transmit FIFO Not Full. This is used to indicate that the transmit FIFO is not full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
[0]	R	BUSY	UART Busy. It indicate that a serial transfer is in progress; when cleared, indicates that the DW_apb_uart is idle or inactive. 0 = DW_apb_uart is idle or inactive 1 = DW_apb_uart is busy (actively transferring data) NOTE : It is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the DW_apb_uart has no data in THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the DW_apb_uart. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is depdent on the baud divisor that has been programmed.

4.31.17 Transmit FIFO Level Register

Address Offset: P4_80h Default Value:00h

Bit	Access	Symbol	Description
[7:5]	R/W	Reserved	
[4:0]	R/W	Transmit FIFO Level	Transmit FIFO Level. This indicates the number of data entries in the transmit FIFO.

4.31.18 Receive FIFO Level Register

Address Offset: P4_84h Default Value:00h

Bit	Access	Symbol	Description
[7:5]	R/W	Reserved	
[4:0]	R/W	Receive FIFO Level	Receive FIFO Level. This indicates the number of data entries in the receive FIFO.

4.31.19 Software Reset Register

Address Offset: P4_88h Default Value:00h

Bit	Access	Symbol	Description
[7:3]	R/W	Reserved	

[2]	W	XFR	XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
[1]	W	RFR	RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO. This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
[0]	W	UR	UART Reset. This asynchronously resets the DW_apb_uart and synchronously removes the reset assertion.

4.31.20 Shadow Request to Send Register

Address Offset: P4_8Ch Default Value:00h

Bit	Access	Symbol	Description
[7:1]	R/W	Reserved	
[0]	R/W	Shadow Request To Send	Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that DW_apb_uart is ready to exchange data. The rts_n signal is set low by programming MCR[1] (RTS) to a high. Note that in Loopback mode (MCR[4]=1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input.

4.31.21 Shadow Break Control Register

Address Offset: P4_90h Default Value:00h

Bit	Access	Symbol	Description
[7:1]	R/W	Reserved	
[0]	R/W	Shadow Break Control Register	Shadow Break Control Bit. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read-modify-write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. When in Loopback Mode, the break condition is internally looped back to the receiver.

4.31.22 Shadow FIFO Enable Register

Address Offset: P4_98h Default Value:00h

Bit	Access	Symbol	Description
[7:1]	R/W	Reserved	
[0]	R/W	Shadow FIFO enable	Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit get updated. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset.

4.31.23 Shadow RCVR Trigger Register

Address Offset: P4_9Ch Default Value:00h

Bit	Access	Symbol	Description
[7:2]	R/W	Reserved	
[1:0]	R/W	Shadow RCVR Trigger	Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receive FIFO at which the Received Data Available Interrupt is generated. The following trigger levels are supported : 00 = 1 character in the FIFO 01 = FIFO 1/4 full 10 = FIFO 1/2 full 11 = FIFO 2 less than full

4.31.24 Shadow TX Empty Trigger Register

Address Offset: P4_A0h Default Value:00h

Bit	Access	Symbol	Description
[7:2]	R/W	Reserved	
[1:0]	R/W	Shadow TX Empty Trigger	Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit get updates. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported : 00 = FIFO empty 01 = 2 character in the FIFO 10 = FIFO 1/4 full 11 = FIFO 1/2 full

4.31.25 Hold TX Register

Address Offset: P4_A4h Default Value:00h

Bit	Access	Symbol	Description
[7:1]	R/W	Reserved	
[0]	R/W	Halt TX	This register is ued to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are enabled. 0 = Halt TX disabled 1 = Halt TX enabled

4.31.26 Component Parameter Register

Address Offset: P4_F4h Default Value:22h

Bit	Access	Symbol	Description
[7]	R	SIR_LP_MODE	configure as 0 in eagle's UART
[6]	R	SIR_MODE	configure as 0 in eagle's UART
[5]	R	THRE_MODE	configure as 1 in eagle's UART
[4]	R	AFCE_MODE	configure as 0 in eagle's UART
[3:2]	R	Reserved	
[1:0]	R	APB_DATA_WIDTH	configure as 10 in eagle's UART

Address Offset: P4_F5h Default Value:1Fh

Bit	Access	Symbol	Description
[7:6]	R	Reserved	
[5]	R	DMA_EXTRA	configure as 0 in eagle's UART
[4]	R	UART_ADD_ ENCODED_PARAMS	configure as 1 in eagle's UART
[3]	R	SHADOW	configure as 1 in eagle's UART
[2]	R	FIFO_STAT	configure as 1 in eagle's UART
[1]	R	FIFO_ACCESS	configure as 1 in eagle's UART
[0]	R	ADDITIONAL_FEAT	configure as 1 in eagle's UART

Address Offset: P4_F6h Default Value:01h

Bit	Access	Symbol	Description
[7:0]	R	FIFO_MODE	0x01 = 16

4.31.27 UART Component Version Register

Address Offset: P4_F8h Default Value:2Ah

Bit	Access	Symbol	Description
[7:0]	R	UART Component Version	Bit [7:0] of ASCII value for each number in the version, follow by *. For example 32_30_31_2A represents the version 2.01*

Address Offset: P4_F9h Default Value:35h

Bit	Access	Symbol	Description
[7:0]	R	UART Component Version	Bit [15:8] of ASCII value for each number in the version, follow by *. For example 32_30_31_2A represents the version 2.01*

Address Offset: P4_FAh Default Value:30h

Bit	Access	Symbol	Description
[7:0]	R	UART Component Version	Bit [23:16] of ASCII value for each number in the version, follow by *. For example 32_30_31_2A represents the version 2.01*

Address Offset: P4_FBh Default Value:33h

Bit	Access	Symbol	Description
[7:0]	R	UART Component Version	Bit [31:24] of ASCII value for each number in the version, follow by *. For example 32_30_31_2A represents the version 2.01*

4.31.28 Component Type Register

Address Offset: P4_FCh Default Value:10h

Bit	Access	Symbol	Description
[7:0]	R	Peripheral ID	This register contains the bit [7:0] of peripherals identification code.

Address Offset: P4_FDh Default Value:01h

Bit	Access	Symbol	Description
[7:0]	R	Peripheral ID	This register contains the bit [15:8] of peripherals identification code.

Address Offset: P4_FEh Default Value:57h

Bit	Access	Symbol	Description
[7:0]	R	Peripheral ID	This register contains the bit [23:16] of peripherals identification code.

Address Offset: P4_FFh Default Value:44h

Bit	Access	Symbol	Description
[7:0]	R	Peripheral ID	This register contains the bit [31:24] of peripherals identification code.

4.32 UART1 Register Set

UART1 registers are all the same as UART0, replace P4 with P5 is the corresponding address of register

4.33 Serial Bus Slave Device Address Register Set

Address Offset: P0_F0h Default Value: 40/60h

Bit	Access	Symbol	Description
[7:4]	R/W	SDADDR	default = 40 if CPUINT is low while reset default = 60 if CPUINT is high while reset
[3]	R/W	smbA3	ambA3 for 7181 bonding only, else = 0
[2:0]	RO	Reserved	

4.34 I2C Master Register Set

4.34.1 Register

Address Offset: P2_E0h Default Value: 40h

Bit	Access	Symbol	Description
[7]	R/W	I2C_Host_400K	1: high speed 0: low speed
[6]	R/W	SMB_SW_Reset	I2C master software reset, default 1
[5]	RO	I2C_InUse	Write 1 Clear, Triggered when Read P3_E0 register
[4]	RO	Failed	W1C, staus of P2_E7[3] Kill_Smb
[3]	RO	Bus_Error	W1C, pull high when SDA inconsistent
[2]	RO	Device_Eror	W1C, Pull high when access to Device Error (Cmmand Error, No Act, Time Out)
[1]	RO	Finish_Intr	W1C, Instruction finish
[0]	RO	Host_Busy	W1C, Host Busy flag

4.34.2 Register

Address Offset: P2_E1h Default Value: 1Eh

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4]	R/W	Mask_Failed	
[3]	R/W	Mask_Bus_Err	
[2]	R/W	Mask_Dev_Err	
[1]	R/W	Mask_Finish_Intr	
[0]	RO	Reserved	

4.34.3 Register

Address Offset: P2_E3h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	{Slave_Address[7:1], R/W_}	[7:1] I2C Host Address, [0]: 1/0 I2C Host Read/Write Command

4.34.4 Register

Address Offset: P2_E4h Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Host_Command[7:0]	I2C Host Command

4.34.5 Register

Address Offset: P2_E5h Default Value: FFh

Bit	Access	Symbol	Description
[7:0]	R/W	Host_RW_D0[7:0]	RO the Data byte 0; Write Data byte 0

4.34.6 Register

Address Offset: P2_E6h Default Value: FFh

Bit	Access	Symbol	Description
[7:0]	R/W	Host_RW_D1[7:0]	RO the Data byte 1; Write Data byte 1

4.34.7 Register

Address Offset: P2_E7h Default Value: 20h

Bit	Access	Symbol	Description
[7]	R/W	Start_SMB	Start smb flow
[6]	R/W	I2C_Host_En	Enable I2C Host
[5]	R/W	I2C_Host_Wait_	SCL pull high action wait until I2C_Host_Wait_ = 1
[4]	R/W	Reserved	
[3]	R/W	Kill_SMB	Cancel smb process
[2:0]	R/W	SMB_Command[2:0]	smb_cmd=3'b101/110/111 is Reserved command 000:Quick_Cmd 001 Receive_Byte (Host_Read) / Send_Byte (~Host_Read) 010 Wrt_Byte (~Host_Read) 011 100 Prcss_Call : Skip Command

4.35 Misc Register Set

Address Offset: P0_E2h Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO	ShutDn_DC2DC	Shut Down Status, PWM2
[6]	RO	ShutDn_LED	Shut Down Status, PWM3 for LED

Address Offset: P5_B0h Default Value: 08h

Bit	Access	Symbol	Description
[5:3]	R/W	Reserved	
[2:0]	R/W		Please refer to DCTi/DLTi

4.36 ADC Bypass Through Line Buffer Register Set

Address Offset: P0_78h Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	R/W	LB_Rd_Mode[1:0]	Line Buffer Read Out Mode: 00b: Normal Path 01b: Read 1 byte per ADC dot from Line Buffer 10b: Read 2 bytes per ADC dot from Line Buffer 11b: Read 3 bytes per ADC dot from Line Buffer

Address Offset: P1_CFh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	ADC_Into_LB	Set to 1 for enabling ADC data to be stored into Line Buffer
[6]	R/W	ADC_sel_NoDith	ADC Data select, 1: bypass dither block

4.37 Color Probing Register Set

4.37.1 Color Probing Sync Source Selection Register

Address Offset: P1_0Fh Default Value: 06h

Bit	Access	Symbol	Description
[7]	R/W	CP_Sel_CVD	Color Probing select CVD sync signal

4.38 BIST and Bypass Register Set

4.38.1 BIST Enable Register

Address Offset: P3_F0h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	FeH_BIST_En	1: FeH Line Buffer Enable BIST
[6]	R/W	EsLUTBIST	1: SPI OSD RAM Enable BIST
[5]	R/W	CQ_BIST_En	1: Command Queue RAM Enable BIST
[4]	R/W	ECacheBIST	1: Enable Cache BIST
[3]	R/W	ENRBIST	1: Noise Reduction Enable BIST
[2]	R/W	EODBIST	1: OSD2 Enable BIST
[1]	R/W	ECBBIST	1: Comb Line Buffer Enable BIST
[0]	R/W	ESMBIST	1: Scale RAM Enable BIST

Address Offset: P3_F1h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	DDC_BIST_En	1:DDC RAM Enable BIST
[2]	R/W	EVVRAMBIST	1: Vivid Color RAM Enable BIST
[1]	R/W	EVVROMBIST	1: Vivid Color ROM Enable BIST
[0]	R/W	EGMBIST	1: Gamma RGB RAM Enable BIST

4.38.2 BIST Done Register

Address Offset: P3_F2h Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO	sLUT_BIST_Done	1: BIST Done of SPI OSD RAM
[6]	RO	CQ_BIST_Done	1: BIST Done of Command Queue RAM
[5]	RO	BIST_VHf_Done	1: BIST Done of VHalf Line Buffer
[4]	RO	BistDone_Cache	1: BIST Done of Cache
[3]	RO	NR_BIST_Done	1 : BIST Done of Noise Reduction
[2]	RO	BD_OSD	1: BIST Done of OSD2 RAM
[1]	RO	CB_BIST_Done	1: BIST Done of Comb Line Buffer
[0]	RO	BD_SM	1: BIST Done of Scale Line Buffer

Address Offset: P3_F3h Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO	DDC_BIST_Done	1: BIST Done of DDC RAM
[3]	RO	VVC_BIST_Done	1: BIST Done of Vivid Color RAM
[1]	RO	Gamma_BIST_Done	1: BIST Done of Gamma RGB RAM
[0]	RO	FeH_BIST_Done	1: BIST Done of FeH Line Buffer

4.38.3 BIST Fail Status Register

Address Offset: P3_F4h Default Value: FFh

Bit	Access	Symbol	Description
[7]	RO	NR_Fail_RD	1: Noise Reduction BIST Fail
[6:5]	RO	OSD_BIST_RD	1: OSD2 RAM BIST Fail
[4]	RO	LBtap_Fail_RD	1: Comb Line Buffer BIST Fail
[3:0]	RO	SMLB_BIST_RD	1: Scale Line Buffer RAM BIST Fail

Address Offset: P3_F5h Default Value: FFh

Bit	Access	Symbol	Description
[7]	RO	sLUT_Fail_Rd	1: SPI OSD RAM BIST Fail
[6]	RO	CQ_Fail_Rd	1: Command Queue RAM BIST Fail
[5]	RO	VHalf_BIST_RD	1: VHalf Line Buffer RAM BIST Fail
[4:1]	RO	Cache_Fail_RD	1:Cache BIST Fail
[0]	RO	ThinL_Fail_Rd	1:Thin Line RAM BIST Fail

Address Offset: P3_F6h Default Value: 8Bh

Bit	Access	Symbol	Description
[7]	RO	DDC_Fail_Rd	1:DDC RAM BIST Fail
[3]	RO	VVC_BIST_RD	1: Vivid Color RAM BIST Fail
[1]	RO	Gamma_BIST_RD	1: Gamma RGB RAM BIST Fail

[0]	RO	FeH_BIST_RD	1: FeH Line Buffer RAM BIST Fail

Address Offset: P3_EEh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	sLUT_Fail_Rd	SPI OSD local BIST fail status. It is included of five signals, PsLUT_Fail_Rd、SsLUT_Fail_Rd、Sprite_Fail_Rd、sram1_Fail_Rd and sram2_Fail_Rd. 5'h01 : TWBC_sram2 BIST Fail. 5'h02 : TWBC_sram1 BIST Fail 5'h04 : Sprite RAM BIST Fail 5'h08 : SsLUT BIST Fail 5'h10 : PsLUT BIST Fail

4.38.4 Bypass Enable Register

Address Offset: P0_FEh Default Value: 00h

Bit	Access	Symbol	Description
[5:4]	RW	BYPS_ADC_Src	00: Video-ADC 01: PWM 10: SAR0 11: SAR1
[0]	R/W	BYPS_ADC	Bypass ADC 1: Signals from Chip bypass to Pin_Out

Address Offset: P0_EFh Default Value: 0

Bit	Access	Symbol	Description
[5]	RW	ByPass_CVD1	Bypass CVD1 1: Signals from Chip bypass to Pin_Out

4.39 DDC Register Set

4.39.1 uP Access DDC Register

Address Offset: P1_5Bh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	DDC_RAM_Address[7:0]	

4.39.2 uP Access DDC Register

Address Offset: P1_5Ch Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	DDC_Data_Address[7:0]	

4.39.3 DDC ID Register

Address Offset: P1_5Dh Default Value: A0h

Bit	Access	Symbol	Description
[7:1]	R/W	DDC_Slave_Address[7:1]	
[1]	R/W	En_DDC_Modify	

4.39.4 DDC Modify Register

Address Offset: P1_5Eh Default Value: A0h

Bit	Access	Symbol	Description

[7:0]	R/W	DDC_ModifyAddress[7:0]	

4.39.5 DDC Modify Register

Address Offset: P1_5Fh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	DDC_ModifyCount[7:0]	

4.40 Watch Dog Timer Register Set

4.40.1 Watch Dog Expired Counter Register

Address Offset: P1_4Eh Default Value: FFh

Bit	Access	Symbol	Description
[7:0]	R/W	WDT_Epr_Cnt[7:0]	Watch Dog timer(WDT) Expire count, max 256(16ms unit)

4.40.2 Watch Dog Enable/Clear Register

Address Offset: P1_4Eh Default Value: FFh

Bit	Access	Symbol	Description
[7]	R/W	WDT_En	WDT_En:enable WDT;
[6]	W1C/WO	WDT_Trig_Clr	WdtRst_2_(item) : enable key for reset item when WDT expired
[5:0]	RO	Reserved	

4.41 Scratch Register Set

4.41.1 Non WDT Reset Register

Address Offset: P1_AFh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Buffer[7:0]	

4.41.2 WDT Reset Register

Address Offset: P1_E0~EFh Default Value: 00h

Bit	Access	Symbol	Description
[7:0]	R/W	Buffer[7:0]	Communication Buffers between i8051 and external MCU (through I2C bus)

4.42 I8051 Control Register Set

4.42.1 BIU Cache Control Register

Address Offset: P1_FDh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	Cache_En	Set to 1 enables the Code Cache
[6]	R/W	TimerClk_Sel	0: i8051_Clk, same as i8051 core 1: XCLK, 27MHz
[5]	R/W	TimerClk_Inv	Set to 1 to inverse clock to Timer
[4:1]	RO	Reserved	
[0]	R/W	RS232_Sel	1: External UART, 0: MCU Internal UART

4.42.2 BIU Control Register

Address Offset: P1_FEh Default Value: 05h

Bit	Access	Symbol	Description
[7]	R/W %Strap	i8051_En	This is RSTB reset strap from GPOA6 pin, to default enable built-in 8051 or not. Later, it can be enabled or disabled via setting this bit.
[6]	WO	i8051_Reset	Write 1 to reset the internal 8051 block
[5]	RO	Reserved	
[4:2]	R/W	ORAM_IO_WaitState[2:0]	Extra Wait State for burst accessing OSD RAM when OSD_En=1
[1:0]	R/W	DClk_IO_WaitState[1:0]	Wait State for accessing slow I/O in output clock domain.

4.42.3 Page Select Register

Address Offset: P1_FFh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	I8051_Hold	Set to 1 to hold i8051, should only be set by I2C
[6:3]	RO	Reserved	
[2]	R/W	Page[3]	
[1]	R/W	Page[1]	
[0]	R/W	Page[0]	

4.43 Pad Control Register Set

4.43.1 Pin Function Register

Address Offset: P1_ACh Default Value: 00h

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4]	R/W	RS232TX1_oeSel	0:others, 1: RS232TX1
[3:2]	R/W	RLUD_oeSel[1:0]	1:RLUD, 2: RS232_AFC, 3: RL out CPUINT
[1:0]	R/W	CPUINT_oeSel[1:0]	0: CPUINT, 1:RS232, 2/3: DDC

4.44 Pad Setting Register Set

4.44.1 Pad Driving Strength Register

Address Offset: P1_A0h Default Value: DCh

Bit	Access	Symbol	Description
[7:0]	R/W	DS[7:0]	

Address Offset: P1_A1h Default Value: F7h

Bit	Access	Symbol	Description
[7:0]	R/W	DS[15:8]	

Address Offset: P1_A2h Default Value: 0Fh

Bit	Access	Symbol	Description
[7:0]	R/W	DS[23:16]	

Address Offset: P1_A3h Default Value: 08h

Bit	Access	Symbol	Description
[7:0]	R/W	DS[31:24]	

4.44.2 Pad Pull Enable Register

Address Offset: P1_A4h Default Value: FFh

Bit	Access	Symbol	Description
[7:0]	R/W	PE[7:0]	

Address Offset: P1_A5h Default Value: FFh

Bit	Access	Symbol	Description
[7:0]	R/W	PE [15:8]	

Address Offset: P1_A6h Default Value: 0Fh

Bit	Access	Symbol	Description
[7:0]	R/W	PE [23:16]	

Address Offset: P1_A7h Default Value: 0Fh

Bit	Access	Symbol	Description
[7:0]	R/W	PE [31:24]	

4.44.3 Pad Pull Selection Register

Address Offset: P1_A4h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	R/W	PS[23:20]	
[3:0]	RO	Reserved	

4.45 Global Control Register Set

4.45.1 Power Management Control Register

Address Offset: P0_E0h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	PD_TotalPad_	Set to 0 for Power Down all I/O pads, except I^2C I/F.
[6]	R/W	PD_ADCD_	Set to 0 for Power Down ADC digital portion.
[5]	R/W	PD_V656_	Power down ITU-R656, L601 interface, active low
[4]	R/W	PD_VD_Clk_	Set to 0 for Power Down Comb Video Decoder block.
[3]	R/W	LLCK1_EN	LLCK1 enable
[2:1]	RO	Reserved	
[0]	R/W	PD_TC_	Set to 0 for Power down TC interface.

4.45.2 Output Pin Configuration Register

Address Offset: P0_E1h Default Value: 00h

Bit	Access	Symbol	Description
[7:6]	R/W	RowSTV_Sel	

RowSTV_Sel	Mode
2'b00	Output both
2'b01	Output both
2'b10	Output STV1
2'b11	Output STV2

[5:4]	R/W	ColSTH_Sel	<table><tr><th>ColSTH_Sel</th><th>Mode</th></tr><tr><td>2'b00</td><td>Output both</td></tr><tr><td>2'b01</td><td>Output both</td></tr><tr><td>2'b10</td><td>Output STH1</td></tr><tr><td>2'b11</td><td>Output STH2</td></tr></table>
[3]	R/W	UD_Sel	Set UD output value
[2]	R/W	RL_Sel	Set RL output value
[1:0]	RO	Reserved	

4.45.3 Shadow Control Configuration Register

Address Offset: P0_E2h Default Value: 10h

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4]	R/W	Shadow_Enable	1: Enable registers shadow control
[3:1]	RO	Reserved	
[0]	WO	Shadow_Sync	Write 1 to sync all shadowed registers

4.45.4 PDBias Control Register

Address Offset: P0_E3h Default Value: 10h

Bit	Access	Symbol	Description
[7]	R/W	PDn_Bias_	0: power down Bias circuit 1: power on Bias circuit
[6:5]	RO	Reserved	
[4]	R/W	PDn_DC2DC_	0: power down DC to DC circuit 1: power on DC to DC circuit
[3:0]	RO	Reserved	

4.45.5 PDBias Control Register

Address Offset: P0_E6h Default Value: C0h

Bit	Access	Symbol	Description
[7]	R/W	PD_CombLB_	0: power down Video Decoder Comb Line Buffers 1: power on Video Decoder Comb Line Buffers
[6]	R/W	PD_XCLK2MC_	0: Tri-state XCLK2MC output 1: Allow XCLK2MC output
[5]	R/W	PDn_BackLight_	0: power down BackLight circuit 1: power on BackLight circuit
[4]	RO	ShutDn_BackLight	Shutdown result
[3]	RO	ShutDn_DC2DC	Shutdown result
[2]	R/W	Byps_656ClkDly	debug
[1]	R/W	Byps_sClkDly	debug
[0]	R/W	Byps_ClkDly	debug

4.45.6 PWM1 General Control Register

Address Offset: P0_E8h Default Value: 07h

Bit	Access	Symbol	Description
[7:6]	R/W	PWM1_Low[4:3]	
[5]	R/W	PWM1_Alt_Mode	1: Alternative PWM1 mode; 0: Legacy {PWM1_High/256} mode
[4]	R/W	PWM1_En	Enable PWM_1
[3]	RO	Reserved	

[2:0]	R/W	PWM1_Freq_Sel	This register set the PWM1 counter base clock = XCLK / 2^N, N=0, 1, 2, 3, 5, 7, 9, 11. That is, the PWM1 freq = PWM1 base clock freq / 256.

4.45.7 PWM1 Active High Time Counter Register

Address Offset: P0_E9h Default Value: 80h

Bit	Access	Symbol	Description
[7:5]	R/W	PWM1_High[7:5] / PWM1_Low[2:0]	InPWM1 legacy mode, this register set PWM1 high time (PWM1_High[7:0]/256) counted by PWM1 base clock. In PWM1 Alternative mode, the PWM1 output: PWM1_High[4:0] / (PWM1_Low[4:0] + PWM1_High[4:0]), based clock is divide from XCLK , see P0_E8<2:0>
[4:0]	R/W	PWM1_High[4:0]	This register set PWM1 high time counted by PWM1 base clock. The based clock is divide from XCLK , see P0_E8<2:0>

4.45.8 PWM4 General Control Register

Address Offset: P0_EAh Default Value: 07h

Bit	Access	Symbol	Description
[7:6]	R/W	PWM4_Low_MSB[4:3]	
[5]	R/W	PWM4_Alt_Mode	1: Alternative PWM4 mode; 0: Legacy {PWM4_High/256} mode
[4]	R/W	PWM4_En	Enable PWM_4
[3]	RO	Reserved	
[2:0]	R/W	PWM4_Freq_Sel[2:0]	This register set the PWM4 counter base clock = XCLK / 2^N, N=0, 1, 2, 3, 5, 7, 9, 11. That is, the PWM4 freq = PWM4 base clock freq / 256.

4.45.9 PWM4 Active High Time Counter Register

Address Offset: P0_EBh Default Value: 80h

Bit	Access	Symbol	Description
[7:5]	R/W	PWM4_High[7:5] / PWM4_Low[2:0]	InPWM4 legacy mode, this register set PWM4 high time (PWM4_High[7:0]/256) counted by PWM4 base clock. In PWM4 Alternative mode, the PWM4 output: PWM4_High[4:0] / (PWM4_Low[4:0] + PWM4_High[4:0]), based clock is divide from XCLK , see P0_E8<2:0>
[4:0]	R/W	PWM4_High[4:0]	This register set PWM4 high time counted by PWM4 base clock. The based clock is divide from XCLK , see P0_E8<2:0>

4.45.10 Shutdown Control Register

Address Offset: P0_EFh Default Value: 40h

Bit	Access	Symbol	Description
[7:6]	R/W	XCLK2MC_Div[1:0]	Extra divider for XCLK oscillator to XCLK2MC output: 00b: stop; 01b:1/1; 10b:1/2; 11b:1/4;
[5]	R/W	Byps_CVD1	
[4:0]	RO	Reserved	

4.45.11 Serial Bus Slave Device Address Register

Address Offset: P0_F0h Default Value: 40/50h

Bit	Access	Symbol	Description
[7:3]	R/W	I2C Slave Address/ID	default = 40 if SPI_SO_ is low while reset default = 50 if SPI_SO_ is high while reset
[2:0]	RO	Reserved	

4.45.12 Serial Bus Control Register

Address Offset: P0_F1h Default Value: C4h

Bit	Access	Symbol	Description
[7]	R/W	SCL_Out	SCL output value, when i8051 enabled and acts as an I2C master
[6]	RO	SCL_In	SCL input status
[5]	R/W	SDA_Out	SDA output value, when i8051 enabled and acts as an I2C master
[4]	RO	SDA_In	SDA input status
[3]	R/W	Xbus_En	
[2]	R/W	Auto_Inc_Address	Set to 1 for enabling 2-wire serial bus automatic address increment in multiple R/W Access mode. Default=1'b1.
[1:0]	R/W	Reserved	

4.45.13 Foundry ID Register

Address Offset: P0_F3h Default Value: 01h

Bit	Access	Symbol	Description
[7:0]	RO	FID	Foundry ID

4.45.14 Chip ID Register

Address Offset: P0_F4h Default Value: 23h

Bit	Access	Symbol	Description
[7:0]	RO	CID	Chip ID

4.45.15 Revision ID Register

Address Offset: P0_F5h Default Value: AAh

Bit	Access	Symbol	Description
[7:0]	RO	RID	Revision ID, ECO version

4.45.16 Date Code ID Register

Address Offset: P0_F6h Default Value: C3h

Bit	Access	Symbol	Description
[7:0]	RO	DID_H	Date code ID, Year/Month

4.45.17 Wakeup Control Register 1

Address Offset: P0_FCh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	SAR0_PwrM_En	1: enable power management function
[6]	RO/W1C	SAR_PwrM_WakeUp	Read to get the wake up event trigger; Write 1 to clear
[5]	R/W	SAR1_PwrM_En	
[4]	RO	Reserved	
[3:0]	R/W	PwrM_SAR_Threshold	SAR Threshold for Power management event trigger

4.45.18 Wakeup Control Register 2

Address Offset: P0_FDh Default Value: ACh

Bit	Access	Symbol	Description
[7:4]	R/W	PwrM_GPIO_Value	Set Wakeup control value on GPIOs
[3:0]	R/W	PwrM_GPIO_Sel	Select which GPIO[n] for Power management

4.45.19 Pin Function Select Register

Address Offset: P0_FEh Default Value: 00h

Bit	Access	Symbol	Description

[7:6]	RO	Reserved	
[5:4]	R/W	Byps_ADC_Src	00: video ADC, 01: PWM, 10: SAR0, 11:SAR1
[3]	R/W	Panel_TTL_6bits	1: RGB666 output 0: RGB888 output
[2]	R/W	En_TTL_Output	1:Enable TTL output
[1]	RO	Reserved	
[0]	R/W	ByPass_ADC	Bypass ADC 1: Signals from Chip bypass to Pin_Out

4.45.20 Page Select Register

Address Offset: P0_FFh Default Value: 00h

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	Page[2:0]	

4.46 SOY Register Set

4.46.1 SOY Tracking Control Register

Address Offset: P1_00h Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	SOY_Track_En	Enable SOY tracking
[6]	R/W	Fake_HRef_En	
[5]	R/W	AutoSwtch_XCLK_En	
[4]	RO	Reserved	
[3]	R/W	SOY_LPF_En	Enable low pass filter of sync slicer
[2:0]	R/W	SOY_LPF_Sel	Low-pass filter bandwidth selection for sync slicer 000 : 200MHz 001 : 175 MHz 010 : 150 MHz 011 : 105 MHz 100 : 60 MHz 101 : 35 MHz 110 : 12 MHz 111 : 6.5MHz

4.46.2 SOY Tracking BP Register

Address Offset: P1_01h Default Value: 35h

Bit	Access	Symbol	Description
[7:0]	R/W	SOY_Track_BP[7:0]	

4.46.3 SOY Tracking FP LSB Register

Address Offset: P1_02h Default Value: 12h

Bit	Access	Symbol	Description
[7:0]	R/W	SOY_Track_FP[7:0]	

4.46.4 SOY Tracking FP MSB Register

Address Offset: P1_03h Default Value: 06h

Bit	Access	Symbol	Description
[7:4]	RO	Reserveed	
[3:0]	R/W	SOY_Track_FP[11:8]	

4.46.5 Fake HRef Low LSB Register

Address Offset: P1_04h Default Value: 80h

Bit	Access	Symbol	Description
[7:0]	R/W	Fake_HRef_Low[7:0]	

4.46.6 Fake HRef Low MSB Register

Address Offset: P1_05h Default Value: 00h

Bit	Access	Symbol	Description
[7:4]	RO	Reserveed	
[3:0]	R/W	Fake_HRef_Low[11:8]	

4.46.7 Fake HRef High LSB Register

Address Offset: P1_06h Default Value: 34h

Bit	Access	Symbol	Description
[7:0]	R/W	Fake_HRef_ High [7:0]	

4.46.8 Fake HRef High MSB Register

Address Offset: P1_07h Default Value: 06h

Bit	Access	Symbol	Description
[7:4]	RO	Reserveed	
[3:0]	R/W	Fake_HRef_High[11:8]	

4.46.9 Fake Ref Test Register

Address Offset: P1_08h Default Value: 00h

Bit	Access	Symbol	Description
[7:1]	RO	Reserveed	
[0]	R/W	Fake_Ref_Test	

4.46.10 SOY PreFilter Control Register

Address Offset: P1_0Ah Default Value: 20h

Bit	Access	Symbol	Description
[7]	R/W	En_SOY_PreFilter	
[6]	R/W	En_SOYPF_Detect	
[5:0]	R/W	SOY_PreF_DecideWindow	

4.46.11 SOY PreFilter Check Window Register

Address Offset: P1_0Bh Default Value: 10h

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	SOY_PreF_CheckWindow	

4.46.12 SOY PreFilter Period LSB Register

Address Offset: P1_0Ch Default Value: 5Ah

Bit	Access	Symbol	Description
[5:0]	R/W	SOY_PreF_Preriod[7:0]	

4.46.13 SOY PreFilter Period MSB Register

Address Offset: P1_0Dh Default Value: 03h

Bit	Access	Symbol	Description

[7:4]	RO	Reserved	
[3:0]	R/W	SOY_PreF_Preriod[11:8]	

4.46.14 SOY PF Period ReadBack LSB Register

Address Offset: P1_0Eh Default Value: -

Bit	Access	Symbol	Description
[5:0]	R/W	SOYPF_Preriod[7:0]	

4.46.15 SOY PF Period ReadBack MSB Register

Address Offset: P1_0Fh Default Value: -

Bit	Access	Symbol	Description
[7:0]	R/W	SOYPF_Preriod [15:8]	

4.47 CCIR656 Encoder Register Set

4.47.1 CCIR656 Encoder Control Register

Address Offset: P0_ECh Default Value: 00h

Bit	Access	Symbol	Description
[7]	R/W	enfld_mode	Enable Input Field mode enfld_mode = 0: enc656 field using input field enfld_mode = 1: enc656 field using free run field or register setting P0_F7[4]
[6]	R/W	manu_fld_en	manual field mode Enable, 1/0 : free run field / P0_1C[1] Setting
[5]	R/W	YC_Range	Output data range 1/0 : 1~254/16~240
[4]	R/W	FV_Sync_EOV	Field & VSync changing Mode 1: Field & Vsync change at EAV(End of VDE) status
[3]	R/W	Filp_yc	Flip yc data
[2]	R/W	Flip_uv	Flip uv data
[1]	R/W	Shift_uv	Shift one pixel uv data
[0]	R/W	Enable656	Enable CCIR656 coding

4.47.2 CCIR656 Encoder Control2 Register

Address Offset: P0_EDh Default Value: 00h

Bit	Access	Symbol	Description
[7:2]	RO	Reserved	
[1]	R/W	fld_por	Field polarity
[0]	RO	Reserved	

4.48 Interrupt Register Set

4.48.1 Interrupt Status Register Set 1

Address Offset: P6_12h Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO/W1C	IR_int	IR packet received interrupt
[6]	RO/W1C	SPI_DMA_Done	SPI DMA Done interrupt
[5]	RO/W1C	Vsync_Lead_edge	Vsync Leading Edge interrupt
[4]	RO/W1C	10ms_time_out	10 ms timer time out interrupt
[3]	RO/W1C	Hsync_timing_chg	Hsync timing change interrupt
[2]	RO/W1C	Vsync_timing_chg	Vsync timing change interrupt
[1]	RO/W1C	Hsync_missing	Hsync missing interrupt

[0]	RO/W1C	Vsync_missing	Vsync missing interrupt

4.48.2 Interrupt Status Register Set 2

Address Offset: P6_13h Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO/W1C	CQ_int	CQ (Command queue) interrupt
[6]	RO	GPIO_INT	GPIO interrupt
[5]	RO/W1C	UART1_int	UART1 interrupt
[4]	RO/W1C	UART0_int	UART0 interrupt
[3]	RO/W1C	DDC_Int_to_uP	DDC interrupt
[2]	RO/W1C	ShortVS_FreeRun_Trig	ShortVS interrupt
[1]	RO/W1C	SAR1_Trig_Int	SAR1 interrupt
[0]	RO/W1C	SAR0_Trig_Int	SAR0 interrupt

4.48.3 Interrupt Mask Register Set 1

Address Offset: P6_14h Default Value: FFh

Bit	Access	Symbol	Description
[7]	R/W	Mask_IR_int	Mask Trigger of IR packet received interrupt
[6]	R/W	Mask_SPI_DMA_Done	Mask Trigger of SPI DMA Done interrupt
[5]	R/W	Mask_Vsync_Lead_edge	Mask Trigger of Vsync Leading Edge interrupt
[4]	R/W	Mask_10ms_time_out	Mask Trigger of 10 ms timer time out interrupt
[3]	R/W	Mask_Hsync_timing_chg	Mask Trigger of Hsync timing change interrupt
[2]	R/W	Mask_Vsync_timing_chg	Mask Trigger of Vsync timing change interrupt
[1]	R/W	Mask_Hsync_missing	Mask Trigger of Hsync missing interrupt
[0]	R/W	Mask_Vsync_missing	Mask Trigger of Vsync missing interrupt

4.48.4 Interrupt Mask Register Set 2

Address Offset: P6_15h Default Value: FFh

Bit	Access	Symbol	Description
[7]	R/W	Mask_CQ_int	Mask Trigger of CQ (Command queue) interrupt
[6]	R/W	Mask_GPIO_INT	Mask Trigger of GPIO interrupt
[5]	R/W	Mask_UART1_int	Mask Trigger of UART1 interrupt
[4]	R/W	Mask_UART0_int	Mask Trigger of UART0 interrupt
[3]	R/W	Mask_DDC_Int_to_uP	Mask Trigger of DDC interrupt
[2]	R/W	Mask_ShortVS_FreeRun_Trig	Mask Trigger of ShortVS interrupt
[1]	R/W	Mask_SAR1_Trig_Int	Mask Trigger of SAR1 interrupt
[0]	R/W	Mask_SAR0_Trig_Int	Mask Trigger of SAR0 interrupt

4.48.5 Interrupt Status Register Set 3

Address Offset: P6_16h Default Value: 00h

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6]	RO	Reserved	
[5]	RO/W1C	Vsync_Lead_edge_sub	Vsync Leading Edge interrupt
[4]	RO	Reserved	
[3]	RO/W1C	Hsync_timing_chg_sub	Hsync timing change interrupt
[2]	RO/W1C	Vsync_timing_chg_sub	Vsync timing change interrupt
[1]	RO/W1C	Hsync_missing_sub	Hsync missing interrupt
[0]	RO/W1C	Vsync_missing_sub	Vsync missing interrupt

4.48.6 Interrupt Mask Register Set 3

Address Offset: P6_17h Default Value: 2Fh

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6]	RO	Reserved	
[5]	R/W	Mask_Vsync_Lead_edge_sub	Mask Trigger of Vsync Leading Edge interrupt
[4]	RO	Reserved	
[3]	R/W	Mask_Hsync_timing_chg_sub	Mask Trigger of Hsync timing change interrupt
[2]	R/W	Mask_Vsync_timing_chg_sub	Mask Trigger of Vsync timing change interrupt
[1]	R/W	Mask_Hsync_missing_sub	Mask Trigger of Hsync missing interrupt
[0]	R/W	Mask_Vsync_missing_sub	Mask Trigger of Vsync missing interrupt

5 Electrical Characteristics

5.1 Digital I/O Pad Operation Condition

Table 5-1 Operation Condition

	Parameter	Min	Typ	Max
VDD18	Digital Core Power Supply	1.62V	1.8V	1.98V
VD33	Digital I/O Power Supply	3.0V	3.3V	3.6V
V_{IL}	Input Low Voltage	-0.3V		0.8V
V_{IH}	Input High Voltage	2.0V		5.0V
V_{T+}	Schmitt Trigger Low-to-High Threshold	1.44V	1.58V	1.71V
V_{T+}	Schmitt Trigger High-to-Low Threshold	1.09V	1.19V	1.31V
I_I	Input Leakage Current@ V_I=3.3V or 0V			±1μA
I_{OZ}	Tri-state Output Leakage Current@ V_o=3.3V or 0V			±1μA
I_{OL}	Low level Output Current@ V_{OL}=0.4V			
	2mA	2.1mA	3.4mA	4.2mA
	4mA	4.2mA	6.9mA	8.6mA
	8mA	8.4mA	13.9mA	17.2mA
	12mA	12.5mA	20.8mA	25.8mA
I_{OH}	High level Output Current@ V_{OH}=2.4V			
	2mA	3.0mA	6.2mA	10.0mA
	4mA	5.7mA	11.6mA	18.6mA
	8mA	9.5mA	19.4mA	30.9mA
	12mA	13.3mA	27.1mA	43.3mA
R_{PU}	Pull-up resistor	74KΩ	104KΩ	177KΩ
R_{PD}	Pull-down resistor	62KΩ	90KΩ	176KΩ

Note: R_{PU} and R_{PD} are always present no matter normal operation or power down mode is enabled. A typical 30~40μA false leakage current is resulted from R_{PU} and R_{PD} when a tester forces I/O to 3.3V or 0.0 V.

5.2 DC Characteristics

(VDD18=1.8V; VD33=3.3V; VD33ADC=PVD33=VD33PWM=3.3V; Temp=75oC, unless otherwise noted)

Table 5-2 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
AVD33 Operating voltage range	VD33ADC PVD33 VD33PWM	3.0	3.3	3.6	V	
Operating voltage range	VDD18	1.62	1.8	1.98	V	
AVD33 supply current	IAVD33	--	77		mA	typical YpbPr 720p
VDD33 supply current	IVDD33	--	149		mA	typical YpbPr 720p
VDD18 supply current	IVDD18	--	66		mA	typical YpbPr 720p
Integral non-	INL	--	0.5	+-2	LSB	.

linearity error						
Differential non-linearity error	DNL	--	0.5	+-1	LSB	.

5.3 AC Characteristics

(VDD18=1.8V; VD33=3.3V; VD33ADC=PVD33=VD33DAC=VD33PWM =3.3V; VREF=1.235V; RL=37.5ohm; CL=10pF; RSET=386ohm; Temp=75oC, unless otherwise noted)

Table 5-3 AC Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Condition
CK period	Tck	5	--	--	Ns	
CK to valid output	Tdelay	--	--	0.5*Tck+2	Ns	
Output rise time	Tr	--	--	4	Ns	10% to 90% IOFS; assume no package inductance.
Output fall time	Tf	--	--	4	Ns	90% to 10% IOFS; assume no package inductance.
Output settling time	Tsettle	--	--	TBD	Ns	assume no package inductance
Glitch energy	--	--	--	--	pvs	assume no package inductance

5.4 Analog Processing and A/D Converters

Table 5-4 Analog Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zi	Input impedance, analog video inputs	By design	500			kΩ
Ci	Input capacitance, analog video inputs	By design		10		pF
Vi(pp)	Input voltage range†	Ccoupling = 0.1µF	0.7	1.0	1.3	V
△G	Gain control range		0		12	dB
DNL	DC differential nonlinearity	A/D only		±0.5		LSB
INL	DC integral nonlinearity	A/D only		±1		LSB
Fr	Frequency response	6 MHz		−0.9		dB
			−3			
SNR	Signal-to-noise ratio	6 MHz, 1.0 Vp-p		50		dB
NS	Noise spectrum	50% flat field		50		dB
DP	Differential phase		1.5			
DG	Differential gain			0.5%		

5.5 Absolute Maximum Rating

Table 5-5 Min and Max Temperature

	Parameter	Min	Max	Unit
Topr	Operation Temperature	-20	+85	°C
Tstg	Storage Temperature *Note	-65	+150	°C

***Note 1** – Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)
***Note 2** – Floor life (Out of bag) at factory conditions (30°C/60% RH) is 168 hours (Level 3 compliant)

5.6 I²C Host Interface Timing

Table 5-6 I²C Host Interface Timing

	Parameter	Min	Typ	Max
t1	Bus free time between a Stop and Start condition	4.7us		
t2	Hold time (repeated) Start condition	4.0us		
t3	Rise time of both SDA and SCL			1000ns
t4	Data hold time	5.0us		
t5	Data setup time	250ns		
t6	Fall time of both SDA and SCL			300ns
t7	Setup time for a repeated Start condition	4.7us		
t8	Setup time for Stop condition	4.0us		
tLow	Low period of the SCL	4.7us		
tHigh	High period of the SCL	4.0us		
fSCL	SCL clock frequency			1Mhz
Cb	Capacitive load for each bus line			400pF

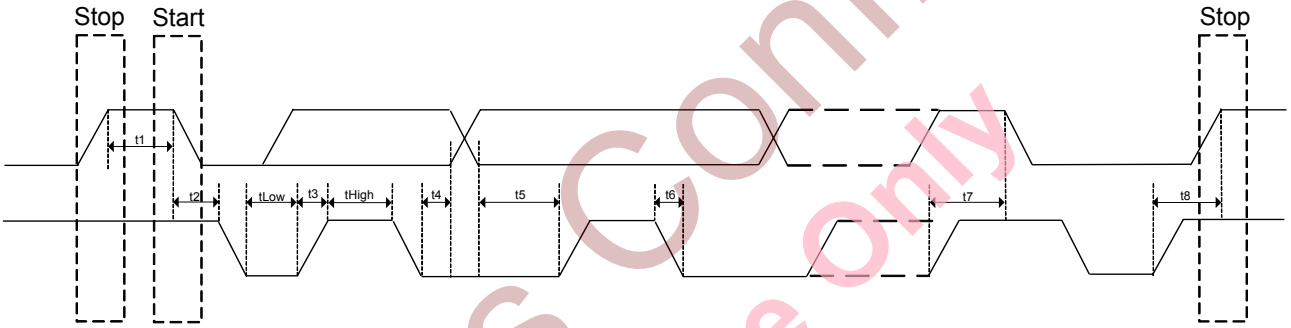
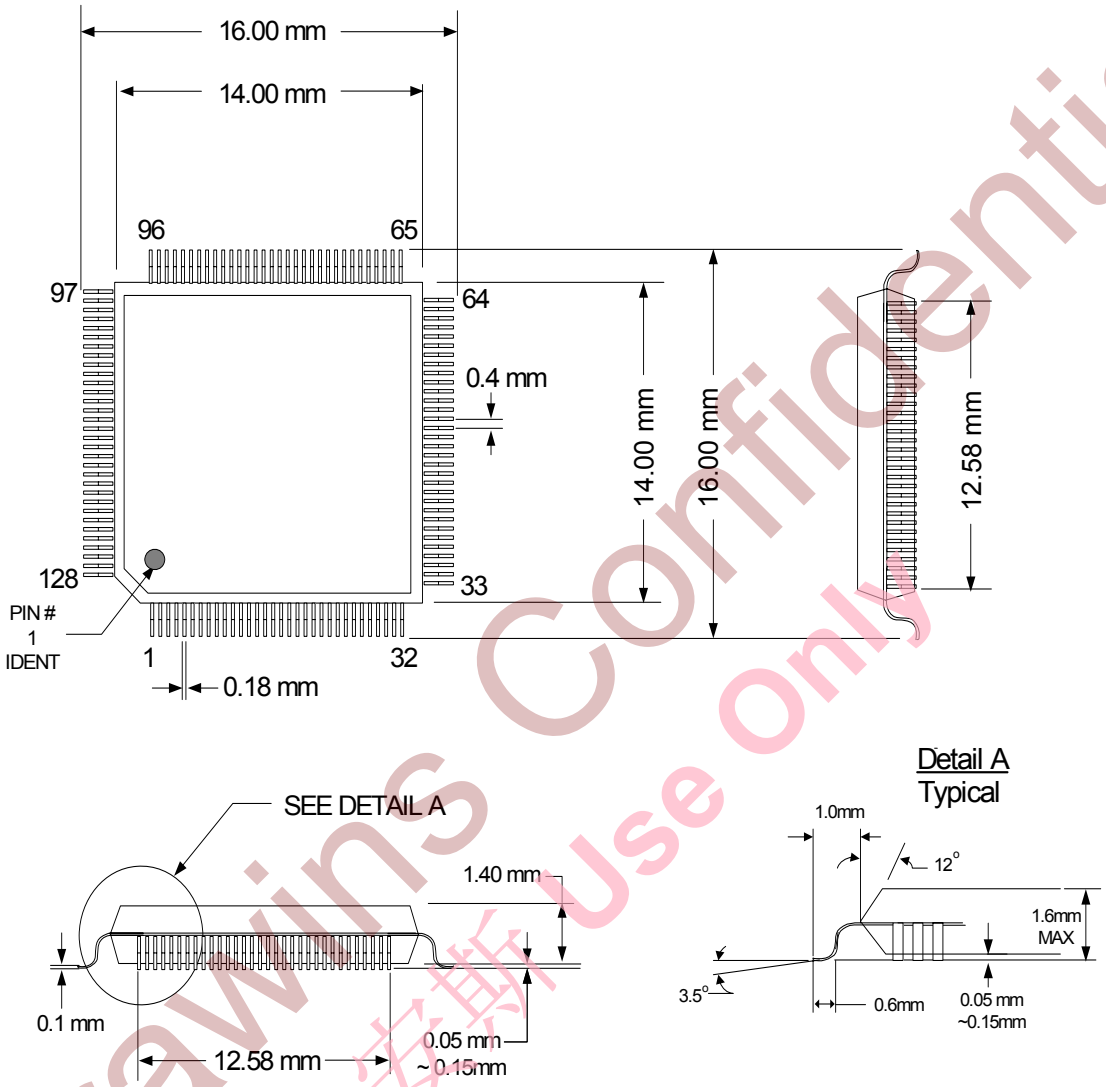


Figure 5-1 I²C Timing

6 Package Dimensions



128 LQFP 14 X 14 X 1.4 mm

Figure 6-1 128-Pin LQFP Dimensions

7 Ordering Information

Table 7-1 Ordering Information

Part No.	Package
T123AI	128 LQFP

8 General Disclaimer

Disclaimer

This document provides technical information for the user. The information furnished by Terawins Inc. believed to be accurate and reliable. However, this document subject to change without any notice. The customer should make sure that they have the most recent version. Terawins Inc. holds no responsibility for any errors that may appear in this document , and Terawins, Inc. does not assume any responsibility for its use, nor for infringement of patents or any other rights of third parties.

Copyright Notice

Trademark Acknowledgment

Terawins is the Terawins Logo.
VESA is a registered trademark of Video Electronics Standards Association.
All other trademarks are the property of their respective companies.

Life Support Policy

Terawins' products are not authorized for use within Life Support Systems without the specific written consent of Terawins, Inc.
Life support systems are systems which are intended for support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user. A critical component in any component of a life support system whose failure to perform can be reasonably expected to cause the failure of the life support system, or to affect its safety or effectiveness.

9 Contact Information

ANGUS TECHNOLOGY LIMITED

Tel: (852) 2345 0540 Fax: (852) 2345 9948 Web Site: www.angus.com.hk