CMOS Digital Integrated Circuit Silicon Monolithic

TC358860XBG

Mobile Peripheral Devices

Overview

TC358860XBG

P-TFBGA65-0505-0.50-001
Weight: **48.2** mg (Typ.)

TC358860XBG converts an Embedded Display Port (eDP^{TM}) video stream into an MIPI® DSI stream. There are four eDP main link lanes in TC358860XBG, they can toggle at either 1.62, 2.16, 2.7, 3.24, 4.32 or 5.4 Gbps/link to receive up to 17.28 Gbps (5.4 Gbps * 0.8 * 4) of video stream. The 4-data lanes dual link DSI Tx can transmit up to 8 Gbps (1 Gbps * 4 * 2) of video stream.

For input video stream with bandwidth (BW) < 4 Gbps, TC358860XBG can output the video data either with a single DSI link or performs left-right line split to output the video data stream with dual DSI links. For input video stream with BW requirements between 4 Gbps and 8 Gbps, left-right line split and dual DSI links usage is necessary.

TC358860XBG provides a compression engine which compress video data with 2-to-1 ratio. This enables TC358860XBG to receive 4K @60fps video streams at eDP Rx, compress and send out to a dual DSI link 4K panel for display. A de-compress engine is expected in the DSI panel.

Host/eDPTx controls/configures TC358860XBG chip by using its AUX channel (I^{2}C over AUX). TC358860XBG provides mail box register/command queue for host to control/configure/command DSI panels, too. After host writes to the command queue, TC358860XBG starts DSI "command packets" to communicate with the DSI panels.

Alternatively, an external I^{2}C master can configure TC358860XBG via I^{2}C bus. Command queue address can also be access via I^{2}C bus, which means Host can use I^{2}C to access command queue, which in turn, controls DSI panel parameters.

Please note that host can not use both AUX ch. and I^{2}C bus for register setting simultaneously.

Features

● TC358860XBG follows the following standards:
  ◇ MIPI Alliance Specification for Display Serial Interface (DSI) version 1.1, Nov 22 2011
  ◇ MIPI Alliance Specification for D-PHY Version 1.1, Nov 7 2011
  ◇ VESA DisplayPort Standard version 1.2a, May 23 2012.
  ◇ VESA Embedded DisplayPort Standard version 1.4 Feb. 28 2013

● eDP Sink (Receiver)
  ◇ Bit Rate @ 1.62, 2.16, 2.7, 3.24, 4.32 or 5.4Gbps, Voltage Swing @0.2 to 1.2 V, Pre-Emphasis Level @3.5dB.
  ◇ There are four lanes available in eDP main Link, which can operate in 1-, 2- or 4-lane configuration.
  ◇ Support Single-Stream Transport (SST), not multi-Stream Transport (MST)
  ◇ Capable of Full and Fast Link Training
  ◇ AUX channel with nominal bit rate at 1 Mbps.
  ◇ Video input data formats supported: RGB666 and RGB888

  ◇ Absolute maximum pixel rate is 600 Mpixel/s.
  ◇ Support Alternate Scrambler Seed Reset (ASSR) is used for content protection, Does not support HDCP encryption.
    - System designer can connect ASSR_Disable Pad to GND, which prevents eDPTx (Source device) to disable ASSR mode TC358860XBG.
    - In order words, when ASSR_Disable Pad is grounded, the Source device cannot clear the ALTERNATE_SCRAMBLER_RESET_ENABLE bit of the eDP_CONFIGURATION_SET register (DPCD Address 0010Ah, bit 0) to 0.
  ◇ No audio SDP, Multi-touch and Backlight DPCD registers support
  ◇ Support REFCLK: 24,25,26 and 27 MHz.

● DSI Transmitter
  ◇ Dual 4-Data Lane DSI Links with Bi-direction support at Data Lane 0. Each link can be used in 1-, 2-, 3- or 4-data lane configuration. Maximum speed at 1.0 Gbps/lane.
  ◇ No deep color support, Video input data formats: RGB666 and RGB888

2015-10-05

- TC358860XBG performs dithering for RGB888 video stream to RGB666 panel
- TC358860XBG appends MSB bits of RGB666 video stream (RGB[5:0] ➔ {RGB[5:0], RGB[5:4]) to RGB888 panel

✧ <u>Interlaced video mode is not supported.</u>

✧ Dual links with Left-Right split: DSI0 carries the left half data of eDP Rx video stream and DSI1 carries the right one

- DSI0 can be assigned/programmed to either DSITx port.
- The maximum length of each half is limited to 2048-pixel plus up to 32-pixel overlap.
- The skew (DSI1 delay w.r.t. to DSI0) between DSI0 and DSI1 can be programmed by register

✧ Provide path for eDP host/transmitter to control TC358860XBG and its attached panel.

✧ Built in Color Bar Generator to verify Dual DSI link without eDPRx input.

✧ DSITx operates in video mode when video stream is continuously received at eDPRx port.

● Video function
  ✧ Compression engine : 2 to 1 compression for 4k2k resolution
  ✧ Magic square
  ✧ Color bar output for debug

● I²C Slave Port
  ✧ Support for normal (100 kHz), fast (400 kHz or 1 MHz, if SysClk is running at 25 MHz) modes.
  ✧ External I²C master can access TC358860XBG internal and DPCD registers and read/write DSI panel register (via DSI link).
  ✧ Address auto increment is supported.
  ✧ TC358860XBG Slave Port address is 0x68, (binary 1101_000x) where x = 1 for read and x = 0 for write. The slave address can be changed to 0x0E (binary 0001_110x) by a weak pull up to pin HPD during boot time.

● Power Supply
  ✧ MIPI D-PHY   1.2 V
  ✧ Core, MIPI D-PHY and   eDP-PHY   1.1 V
  ✧ eDP-PHY: 1.8 V
  ✧ I/O: 1.8 V or 3.3 V (all IO pins must be same power level)
  ✧ HPD Output Pad   1.8 V or 3.3 V

● Power Consumption (Typical Condition)
  ✧ 126 mW
    - Condition: Input 5.4 Gbps eDP 1 lane, Output DSI port 4 data lane, Full HD@60fps resolution,24 bpp
    See Page-82 Power consumption during Typical Operations)

● Packaging
  ✧ 65-pin FBGA Package with 0.5 mm ball pitch
  ✧ 5 x 5 mm^2

Table of content

Table of Figures

List of Tables

- MIPI is registered trademark of MIPI Alliance, Inc.
- VESA, VESA logo and the DisplayPort Icon are trademarks of the Video Electronics Standards Association.

1   **NOTICE OF DISCLAIMER**

2   The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled

3   by any of the authors or developers of this material or MIPI. The material contained herein is provided on

4   an "AS IS" basis and to the maximum extent permitted by applicable law, this material is provided AS IS

5   AND WITH ALL FAULTS, and the authors and developers of this material and MIPI hereby disclaim all

6   other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if

7   any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of

8   accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of

9   negligence.

10   All materials contained herein are protected by copyright laws, and may not be reproduced, republished,

11   distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express

12   prior written permission of MIPI Alliance. MIPI, MIPI Alliance and the dotted rainbow arch and all related

13   trademarks, tradenames, and other intellectual property are the exclusive property of MIPI Alliance and

14   cannot be used without its express prior written permission.

15   ALSO, THERE IS NO WARRANTY OF CONDITION OF TITLE, QUIET ENJOYMENT, QUIET

16   POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD

17   TO THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT. IN NO EVENT WILL ANY

18   AUTHOR OR DEVELOPER OF THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT OR

19   MIPI BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE

20   GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL,

21   CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER

22   CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR

23   ANY OTHER AGREEMENT, SPECIFICATION OR DOCUMENT RELATING TO THIS MATERIAL,

24   WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH

25   DAMAGES.

26   Without limiting the generality of this Disclaimer stated above, the user of the contents of this Document is

27   further notified that MIPI: (a) does not evaluate, test or verify the accuracy, soundness or credibility of the

28   contents of this Document; (b) does not monitor or enforce compliance with the contents of this Document;

29   and (c) does not certify, test, or in any manner investigate products or services or any claims of compliance

30   with the contents of this Document. The use or implementation of the contents of this Document may

31   involve or require the use of intellectual property rights ("IPR") including (but not limited to) patents,

32   patent applications, or copyrights owned by one or more parties, whether or not Members of MIPI. MIPI

33   does not make any search or investigation for IPR, nor does MIPI require or request the disclosure of any

34   IPR or claims of IPR as respects the contents of this Document or otherwise.

35   Questions pertaining to this document, or the terms or conditions of its provision, should be addressed to:

36   MIPI Alliance, Inc.

37   c/o IEEE-ISTO

38   445 Hoes Lane

39   Piscataway, NJ 08854

40   Attn: Board Secretary

This Notice of Disclaimer applies to all DSI input and processing paths related descriptions throughout this
document.

REFERENCES

1. MIPI D-PHY, "MIPI Alliance Specification for D-PHY Version 1.00.00 14-May-2009"
2. MIPI Alliance Standard for DSI Version 1.02.00 – 28 June 2010
3. VESA DisplayPort Standard (Version 1, Revision 2a May 23, 2012)
4. VESA Embedded DisplayPort (eDP) Standard (Version 1.4 February 28, 2013)
5. I^2C bus specification, version 2.1, January 2000, Philips Semiconductor

1. Introduction

This Functional Specification defines operation of TC358860 chip, which converts an Embedded Display Port (eDP) video stream into an MIPI DSI stream. There are four eDP main link lanes in TC358860, they can toggle at either 1.62, 2.16, 2.7, 3.24, 4.32 or 5.4Gbps/link to receive up to 17.28Gbps (5.4Gbps * 0.8 * 4) of video stream. The 4-data lanes dual link DSI Tx can transmit up to 8Gbps (1Gbps * 4 * 2) of video stream.

For input video stream with bandwidth (BW) < 4Gbps, TC358860 can output the video data either with a single DSI link or performs left-right line split to output the video data stream with dual DSI links. For input video stream with BW requirements between 4Gbps and 8Gbps, left-right line split and dual DSI links usage is necessary.

TC358860 provides a compression engine which compress video data with 2-to-1 ratio. This enables TC358860 to receive 4K @60fps video streams at eDP Rx, compress and send out to a dual DSI link 4K panel for display. A de-compress engine is expected in the DSI panel.

Host/eDPTx controls/configures TC358860 chip by using its AUX channel (I^2C over AUX). TC358860 provides mail box register/command queue for host to control/configure/command DSI panels, too. After host writes to the command queue, TC358860 starts DSI "command packets" to communicate with the DSI panels.

Alternatively, an external I^2C master can configure TC358860 via I^2C bus. Command queue address can also be access via I^2C bus, which means Host can use I^2C to access command queue, which in turn, controls DSI panel parameters.

Please note that host can not use both AUX ch. and I^2C bus for register setting simultaneously.

The target system diagram and TC358860XBG block diagram are shown in Figure 1-1 and Figure 1-2, respectively.
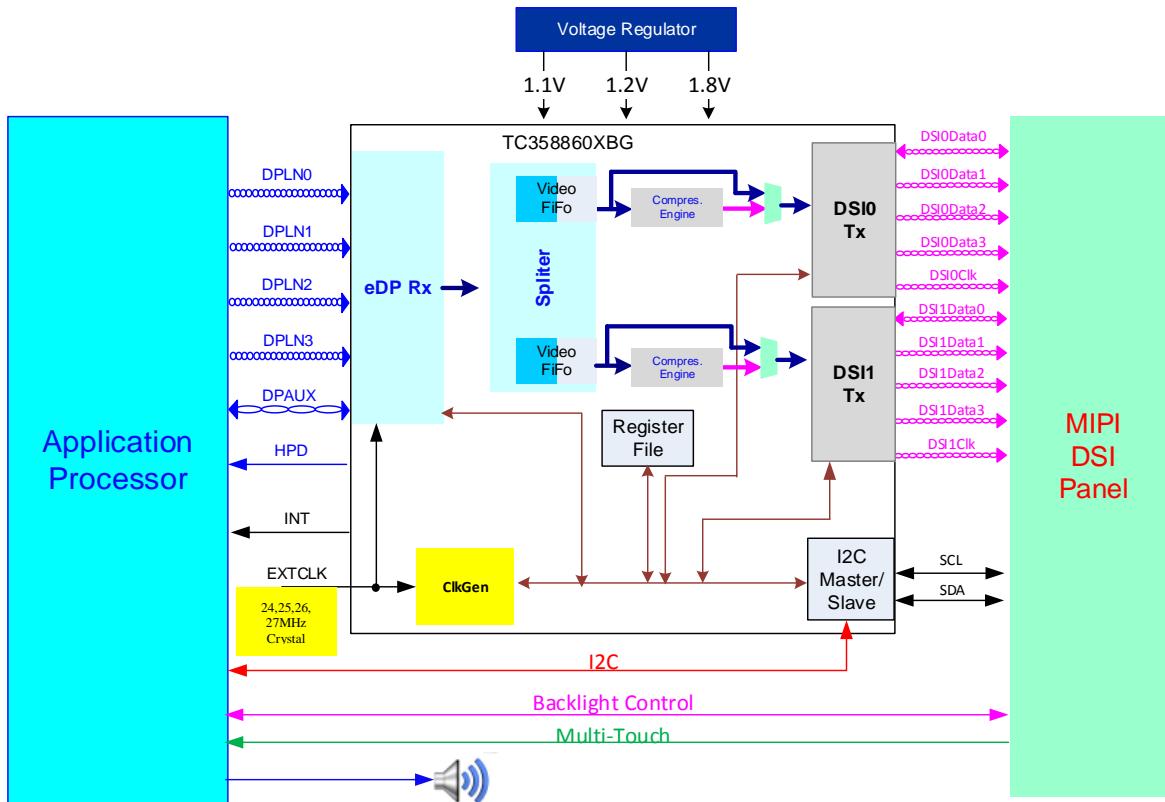
Figure 1-1   TC358860 in System Application
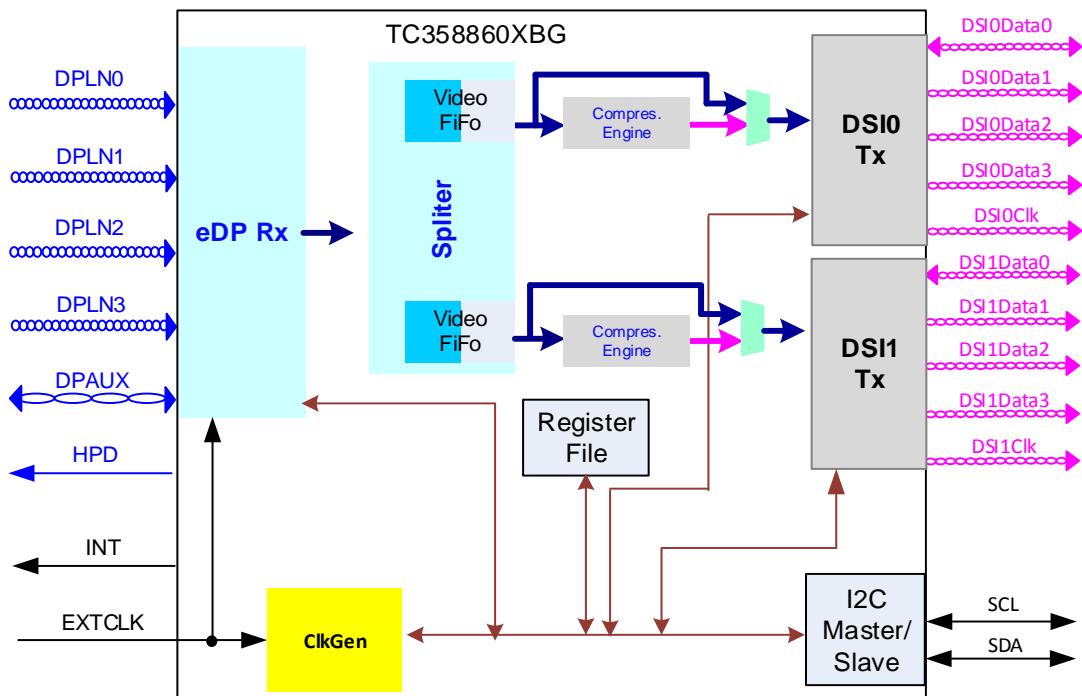
Figure 1-2   TC358860XBG Block Diagram and Functional

2. Features

- TC358860XBG follows the following standards:
  - ✧ MIPI Alliance Specification for Display Serial Interface (DSI) version 1.1, Nov 22 2011
  - ✧ MIPI Alliance Specification for D-PHY Version 1.1, Nov 7 2011
  - ✧ VESA DisplayPort Standard version 1.2a, May 23 2012.
  - ✧ VESA Embedded DisplayPort Standard version 1.4 Feb. 28 2013

- eDP Sink (Receiver)
  - ✧ Bit Rate @ 1.62, 2.16, 2.7, 3.24, 4.32 or 5.4Gbps, Voltage Swing @0.2 to 1.2 V, Pre-Emphasis Level @3.5dB.
  - ✧ There are four lanes available in eDP main Link, which can operate in 1-, 2- or 4-lane configuration.
  - ✧ Support Single-Stream Transport (SST), not multi-Stream Transport (MST)
  - ✧ Capable of Full and Fast Link Training
  - ✧ AUX channel with nominal bit rate at 1 Mbps.
  - ✧ Video input data formats supported: RGB666 and RGB888
  - ✧ Absolute maximum pixel rate is 600Mpixel/s.
  - ✧ Does not support HDCP encryption, Alternate Scrambler Seed Reset (ASSR) is used for content protection.
    - System designer can connect ASSR_Disable Pad to GND, which prevents eDPTx (Source device) to disable ASSR mode TC358860XBG.
    - In order words, when ASSR_Disable Pad is grounded, the Source device cannot clear the ALTERNATE_SCRAMBER_RESET_ENABLE bit of the eDP_CONFIGURATION_SET register (DPCD Address 0x0010A, bit 0) to 0.
  - ✧ No audio SDP, Multi-touch and Backlight DPCD registers support
  - ✧ Support REFCLK 24,25,26 and 27MHz .

- DSI Transmitter
  - ✧ Dual 4-Data Lane DSI Links with Bi-direction support at Data Lane 0. Each link can be used in 1-, 2-, 3- or 4-data lane configuration. Maximum speed at 1.0 Gbps/lane.
  - ✧ No deep color support, Video input data formats: RGB666 and RGB888
    - TC358860XBG performs dithering for RGB888 video stream to RGB666 panel
    - TC358860XBG appends MSB bits of RGB666 video stream (RGB[5:0] ➔ {RGB[5:0], RGB[5:4]}) to RGB888 panel
  - ✧ Interlaced video mode is not supported.
  - ✧ Dual links with Left-Right split: DSI0 carries the left half data of eDP Rx video stream and DSI1 carries the right one
    - DSI0 can be assigned/programmed to either DSITx port.
    - The maximum length of each half is limited to 2048-pixel plus up to 32-pixel overlap.
    - The skew (DSI1 delay w.r.t. to DSI0) between DSI0 and DSI1 can be programmed by register (DSI0VSDelay/DSI1VSDelay and DSI0HBPR/DSI1HBPR shown in Figure 4-17)
  - ✧ Provide path for eDP host/transmitter to control TC358860XBG and its attached panel.
  - ✧ Built in Color Bar Generator to verify Dual DSI link without eDPRx input.
  - ✧ DSITx operates in video mode when video stream is continuously received at eDPRx port.

- Video function

  - ✧ Compression engine : 2 to 1 compression

  - ✧ Magic square

  - ✧ Color bar output for debug

- I^{2}C Slave Port

  - ✧ Support for normal (100 kHz), fast (400 kHz or 1 MHz, if SysClk is running at 25 MHz) modes.

  - ✧ External I^{2}C master can access TC358860XBG internal and DPCD registers and read/write DSI panel register (via DSI link).

  - ✧ Address auto increment is supported.

  - ✧ TC358860XBG Slave Port address is 0x68, (binary 1101_000x) where x = 1 for read and x = 0 for write. The slave address can be changed to 0x0E (binary 0001_110x) by a weak pull up to pin GPIO0 during boot time.

- Power Supply

  - ✧ MIPI D-PHY: 1.2 V

  - ✧ Core, MIPI D-PHY and eDP-PHY: 1.1 V

  - ✧ eDP-PHY: 1.8 V

  - ✧ I/O: 1.8 V or 3.3 V (all IO pins must be same power level)

  - ✧ HPD Output Pad: 1.8 V or 3.3 V

- Power Consumption (Typical Condition)

  - ✧ 126 mW
    - Condition: Input 5.4 Gbps eDP 1 lane, Output DSI port 4 data lane, Full HD@60fps resolution,24 bpp

- Packaging

  - ✧ 65-pin FBGA Package with 0.5 mm ball pitch

  - ✧ 5 x 5 mm^2

3. External Pins

3.1. Pinout Description

The following table gives the signals of TC358860XBG and their function.

Table 3.1   TC358860XBG Functional Signal List

Group	Pin Name	I/O	Type	Initial	Function	Power Supply
System (8)	RESET_N	I	SCH	I	System Reset – active Low	VDDIO
	EXTCLK	I	SCH	I	Ref Clock : 24,25,26,27 MHz	VDDIO
	DIS_ASSR	I	Normal	I	1: Source device can Disable ASSR 0: Source device cannot Disable ASSR	VDDIO
	INT	O	Normal	O(L)	Interrupt	VDDIO
	GPIO[3:0]	I/O	Normal	I(PD)	GPIO	VDDIO
DSI0Tx (10)	DSI0CP	O	MIPI-DPHY	O(L)	MIPI-DSI0 Tx Clock Lane Positive	1.2 V
	DSI0CM	O	MIPI-DPHY	O(L)	MIPI-DSI0 Tx Clock Lane Negative	1.2 V
	DSI0DP_0	I/O	MIPI-DPHY	O(L)	MIPI-DSI0 Tx Data Lane0 Positive	1.2 V
	DSI0DM_0	I/O	MIPI-DPHY	O(L)	MIPI-DSI0 Tx Data Lane0 Negative	1.2 V
	DSI0DP_3,2,1	O	MIPI-DPHY	O(L)	MIPI-DSI0 Tx Data Lane Positive	1.2 V
	DSI0DM_3,2,1	O	MIPI-DPHY	O(L)	MIPI-DSI0 Tx Data Lane Negative	1.2 V
DSI1Tx (10)	DSI1CP	O	MIPI-DPHY	O(L)	MIPI-DSI1 Tx Clock Lane Positive	1.2 V
	DSI1CM	O	MIPI-DPHY	O(L)	MIPI-DSI1 Tx Clock Lane Negative	1.2 V
	DSI1DP_0	I/O	MIPI-DPHY	O(L)	MIPI-DSI1 Tx Data Lane0 Positive	1.2 V
	DSI1DM _0	I/O	MIPI-DPHY	O(L)	MIPI-DSI1 Tx Data Lane0 Negative	1.2 V
	DSI1DP_3,2,1	O	MIPI-DPHY	O(L)	MIPI-DSI1 Tx Data Lane Positive	1.2 V
	DSI1DM_3,2,1	O	MIPI-DPHY	O(L)	MIPI-DSI1 Tx Data Lane Negative	1.2 V
eDP Rx (11)	DPLNP_3,2,1,0	I	eDP-PHY	I	eDP Output Main Link Positive	1.8 V
	DPLNM_3,2,1,0	I	eDP-PHY	I	eDP Output Main Link Negative	1.8 V
	DPAUXP	I/O	eDP-PHY	I	eDP Output AUX Channel Positive	1.8 V
	DPAUXM	I/O	eDP-PHY	I	eDP Output AUX Channel Negative	1.8 V
	HPD	O	Normal	O(L)	eDP Rx INT/Detected Output	VDDIO
I2C (2)	I2C_SCL	I/O	FS/SCH	I	I^{2}C Clock	VDDIO
	I2C_SDA	I/O	FS/SCH	I	I^{2}C Data	VDDIO
Test(4)	TM	I	Normal	I(PD)	Test Pins, tie to GND	VDDIO
	TEST1	I	-	I	Test Pins, tie to GND	1.8 V
	TEST2	O	Analog	O(L)	Analog TEST , Open	-
	TEST3	I	Normal	I	Test Pins, connect to Pull-Up 1kΩ	1.1 V
Power (10)	VDDC (2)	-	-	-	VDD for internal Core	1.1 V
	VDDIO(1)	-	-	-	VDD for I/O voltage	1.8 or 3.3 V
	VDDP2(1)	-	-	-	VDD for PLL	1.1 V
	VDD_DP18(2)	-	-	-	VDD for DP PHY	1.8 V
	VDD_DP11(2)	-	-	-	VDD for DP PHY	1.1 V
	VDD_DSI0(1)	-	-	-	VDD for MIPI DPHY	1.2 V
	VDD_DSI1(1)	-	-	-	VDD for MIPI DPHY	1.2 V
Ground(10)	VSS(10)	-	-	-	VSS for internal core/I/O, DPHY	-

Normal:	Normal IO (Programmable Output Drive Strength 2,4,8 and 12 mA)
OD:	Pseudo open-drain output, schmidtt input
FS/SCH:	Fail Safe schmidtt input buffer
MIPI-PHY:	Front-end analog IO for MIPI
eDP-PHY:	Front-end analog IO for eDP RX
PD	Pull Down

Table 3.2   Pin Count Summary

Group Name	Pin Count	Notes
System	8	
DSI0Tx, DSI1Tx	20	CLK + Data 4 lane x 2 port
eDP Rx	11	Data 4 lane + AUX 1 lane+ HPD
I2C	2	
Test	4	
Power	10	
Ground	10	
Total	**65**	

3.2. Pin Layout

The mapping of TC358860XBG signals to the external pins is shown in the figure below.

DSI1

A1	A2	A3	A4	A5	A6	A7	A8	A9
VDD_DSI0	VDD_DSI1	DSI1DP_3	DSI1DP_2	DSI1CP	DSI1DP_1	DSI1DP_0	VDDC	VDDIO
B1	B2	B3	B4	B5	B6	B7	B8	B9
DSI0DP_0	DSI0DM_0	DSI1DM_3	DSI1DM_2	DSI1CM	DSI1DM_1	DSI1DM_0	RESET_N	DIS_ASSR
C1	C2	C3	C4	C5	C6	C7	C8	C9
DSI0DP_1	DSI0DM_1	no-ball	no-ball	no-ball	no-ball	no-ball	I2C_SDA	I2C_SCL
D1	D2	D3	D4	D5	D6	D7	D8	D9
DSI0CP	DSI0CM	no-ball	VSS	VSS	TEST1	no-ball	GPIO2	GPIO3
E1	E2	E3	E4	E5	E6	E7	E8	E9
DSI0DP_2	DSI0DM_2	no-ball	VSS	VSS	TM	no-ball	GPIO0	GPIO1
F1	F2	F3	F4	F5	F6	F7	F8	F9
DSI0DP_3	DSI0DM_3	no-ball	VSS	TEST2	TEST3	no-ball	INT	EXTCLK
G1	G2	G3	G4	G5	G6	G7	G8	G9
VDDC	VSS	no-ball	no-ball	no-ball	no-ball	no-ball	HPD	VDDP2
H1	H2	H3	H4	H5	H6	H7	H8	H9
VSS	DPLNM_3	VSS	DPLNM_2	VSS	DPLNM_1	VSS	DPLNM_0	DPAUXM
J1	J2	J3	J4	J5	J6	J7	J8	J9
VDD_DP11	DPLNP_3	VDD_DP18	DPLNP_2	VDD_DP11	DPLNP_1	VDD_DP18	DPLNP_0	DPAUXP

DSI0

eDP

Figure 3-1   TC358860XBG Chip Pin Layout (Top view)

☐	Signal(VDDIO)
☐	Differential signal
☐	Analog signal
☐	Power
☐	GND
☐	No-ball or Reserved ball

4. Operations

eDP source/Host needs to initialize/program TC358860XBG in order to for it to operate properly. Host programs TC358860XBG either by using AUX Chanel (I^2C over AUX) or via an I^2C bus. TC358860XBG provides "a 128-byte command queue, CmdQue" for Host to access DSI panel's registers.

In addition to program TC358860XBG and DSI panel, the following operations are also discussed in this section:

● Split eDP stream into Dual link DSI streams

● Compression Operations

4.1. eDP RX

eDP RX block consist of 3 function parts: main link which consist of eDPRX PHY and digital block , AUX ch. block and HPD.
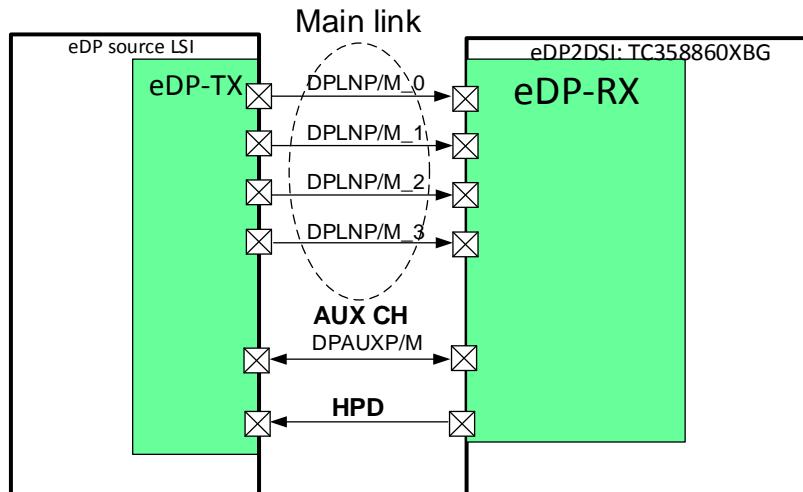
Figure 4-1   System Implementation of eDP

4.1.1. Main link

- eDP-RX PHY
    - Max four lanes available and can operate in 1-, 2- or 4-lane configuration.
    - 8 types of Bit Rate

Link Rate name	Parameter	Nominal per lane Transfer rate [Gbps/lane]	DPCD registers (SUPPORTED_LINK_RATES)
R162 (**RBR**)	Transfer Rate 1	1.62	Address 0x8000 =0x1FA4(8100d)
R216	Transfer Rate 2	2.16	Address 0x8002 =0x2A30(10800d)
R270 (**HBR**)	Transfer Rate 4	2.70	Address 0x8006 =0x34BC(13500d)
R324	Transfer Rate 5	3.24	Address 0x8008 =0x3F48(16200d)
R432	Transfer Rate 6	4.32	Address 0x800A =0x5460(21600d)
R540 (**HBR2**)	Transfer Rate 7	5.40	Address 0x800E =0x6978(27000d)

    - Swing level 200mV to 1.2V
    - Pre-Emphasis level @3.5dB
    - De-Serializer circuit using CDR(Clock and Data Recovery) circuit with local PLL
- Digital block
    - ANS 8B/10B decoding
    - Descramble ASSR(Alternative Scrambler Seed Reset) for Contents protection
    - Support only Single-Stream Transport (SST), not multi-Stream Transport (MST)
    - Link Training: Fast and Full Link Training
    - Video input data formats : RGB666 and RGB888
    - Absolute maximum pixel rate is 600Mpixel/s.
    - System designer can connect ASSR_Disable Pad to GND, which prevents eDPTx (Source device) to disable ASSR mode TC358860XBG.
    - In order words, when ASSR_Disable Pad is grounded, the Source device cannot clear the ALTERNATE_SCRAMBER_RESET_ENABLE bit of the eDP_CONFIGURATION_SET register (DPCD Address 0010Ah, bit 0) to 0.
- REFCLK from 24,25,26 and 27MHz

● No support feature
  – HDCP decryption
  – Video feature: Y-Only, YCbCr data and interlace data
  – PSR mode
  – GTC
  – 3D
  – SDP (Secondary Data Packet)
  – Audio SDP, Multi-touch and Backlight DPCD registers support

4.1.2. AUX channel

AUX channel I/O has differential bi-directional transmitter and receiver functionality that complies with the eDP specification version 1.4, and supports data transfers at rates up to 1Mbps. AUX channel I/O can also support DP specification ver.1.2a and 1.2, by using optional settings: high swing "AUXTXHSEN[1:0] of DPRX_PL_AUX_IO_CTRL0 register". Operation at the Fast-AUX data rates up to 720Mbps is not supported.

4.2. HPD

HPD has following three functionalities.

- Connection indication : To inform connection of Sink device to Source device
- IRQ_HPD(Interrupt): To generate interrupt (IRQ_HPD) to Source device which included with sink specific IRQ like DSI and boot block.
- Hot Plug(HPD) event: To generate Hot Plug event to Source device whenever sink device is connected to main power supply

4.2.1. IRQ_HDP and INT

TC358860XBG has two interrupt output pins with HPD of eDP RX block and INT pin as showing following diagram.
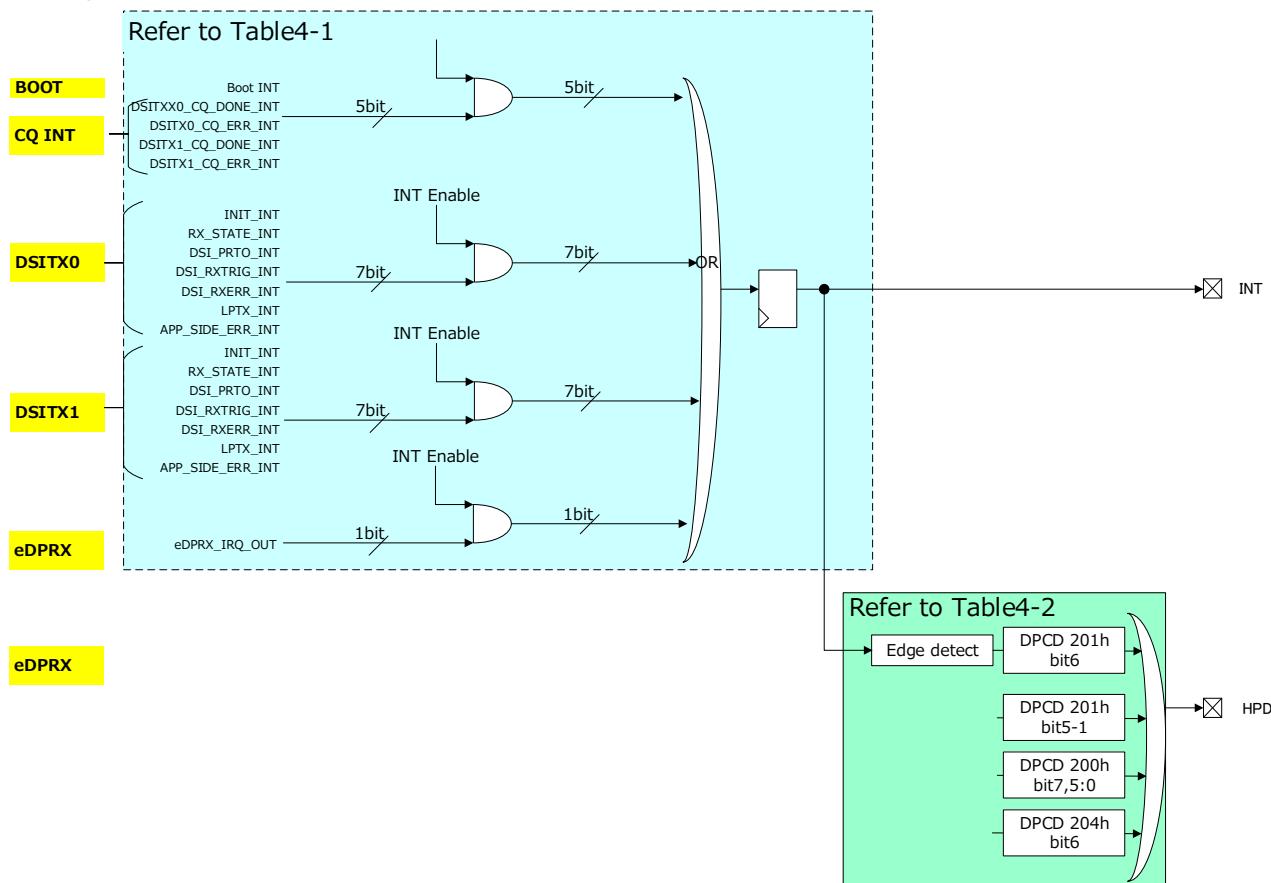
Figure 4-2   IRQ_HPD/INT connection

Table 4.1 Register for IRQ_HPD/INT

Group	Address	Register	Description	Interrupt signal
Boot registers	0x1018	Boot Status	Boot status register	Boot INT
DSITx0 Command Queue Registers	0x2204	DSI0_CQ_STATUS	DSITx0 CQ error interrupt	DSIRX0_CQ_DONE_INT, DSIRX0_CQ_ERR_INT
DSITx1 Command Queue Registers	0x3204	DSI1_CQ_STATUS	DSITx1 CQ error interrupt	DSIRX1_CQ_DONE_INT, DSIRX1_CQ_ERR_INT
DSITX0 registers	0x2160 0x21A8 0x2208 0x20A8 0x2118 0x2120 0x2110	DSI0_INIT_INT_STAT DSI0_RX_STATE_INT_STAT DSI0_PRTO_INT_STAT DSI0_RXTRIG_INT_STAT DSI0_RXERR_INIT_STAT LPTX_INT_STAT APP_SIDE_ERR_INT_STAT	DSITX0 block interrupt	INIT_INT RX_STATE_INT DSI_PRTO_INT DSI_RXTRIG_INT DSI_RXERR_INT LPTX_INT APP_SIDE_ERR_INT
DSITX1 registers	0x3160 0x31A8 0x3208 0x30A8 0x3118 0x3120 0x3110	DSI1_INIT_INT_STAT DSI1_RX_STATE_INT_STAT DSI1_PRTO_INT_STAT DSI1_RXTRIG_INT_STAT DSI1_RXERR_INIT_STAT LPTX_INT_STAT APP_SIDE_ERR_INT_STAT	DSITX1 block interrupt	INIT_INT RX_STATE_INT DSI_PRTO_INT DSI_RXTRIG_INT DSI_RXERR_INT LPTX_INT APP_SIDE_ERR_INT
eDPRX registers	0xB012 0xB40E 0xB629 0xB62A 0xB62B 0xB62C 0xB64A 0xB64E	HPD_CMD AL_ERR_STS PL_AUXRX_ERR_STS0 PL_AUXRX_ERR_STS1 PL_AUXRX_ERR_STS2 PL_AUXRX_ERR_STS3 PL_MAINLINK_AFE_ERR_STS PL_MAINLINK_FIFO_STS	HPD command eDP ALPM Error Status register eDP AUX RX Error Status0 register eDP AUX RX Error Status1 register eDP AUX RX Error Status2 register eDP AUX RX Error Status3 register Main-Link AFE Error Status Register Main-Link FIFO status Register	IRQ_OUT

4.2.2. IRQ_HPD

Following table shows factor of supported Interrupt.

Table 4.2   IRQ_HPD factors

No.	Factor of INT	Comment	Condition	
			from L to H	From H to L
1	Status change	DPCD Address 0x0200: "SINK_COUNT"	Generate IRQ_HPD	
		DPCD Address 0x0201: "DEVICE_SERVICE_IRQ_VECTOR"	Generate IRQ_HPD	-
		DPCD Address 0x0204 bit6 "LANE_ALIGN__STATUS_UPDATED"	Generate IRQ_HPD	-
2	Fail of Synchronization(Lock)	When Fast link training is failed	AL_FASTTRNTO_SETPLS=1 (Pulse)	
3	ALPM Lock Error	To generate ALPM lock time out	AL_ALPM_LOCK_TIMEOUT_SETPLS = 1 (Pulse)	
4	Loss of Synchronization	Loss of Synchronization	Change AL_ERRTRANS_TO_STANDBY from 0 to 1	
5	Indication of ALPM from ACTIVE to STANDBY	To generate IRQ_HPD when transition	When AL_ERRTRANS_TO_STANDBY=1, IRQ_HPD is generated in every RG_HPD_LOW*4096*128 cycle	
6	Command		RG_IRQ_HPD_CMD = 1(Pulse)	
7	SINK_SPECIFIC_IRQ	DPCD address: 0x0201, bit6(SINK_SPECIFIC_IRQ)	This factor is Included with No.1.	

Following table shows list of nonsupport interrupt factor which eDP standard spec is supported.

Table 4.3   IRQ_HPD Nonsupport factors

No.	Factor of INT	Comment	Reason of remove
1	Change Downstream HPD	Downstream HPD is changed (only BRANCH_DEVICE_CTRL bit0=1)	Nonsupport feature
2	Change Downstream Status	Downstream Status is changed (when DOWNSTREAM_PORT_STATUS_CHANGED=1)	Nonsupport feature
3	Change Capability	Capability change (when RX_CAP_CHANGED=1)	Nonsupport for active capability change because of embedded system
4	PSR related		Nonsupport feature: PSR
5	AUX_FRAM_SYNC related		Nonsupport feature: AUX_FRAME_SYNC
6	FAUX related		Nonsupport feature: FAUX
7	MST related		Nonsupport feature: MST
8	TOUCH DEVICE related		Nonsupport feature: TOUCH DEVICE
9	COMPRESSION related		Nonsupport feature: COMPRESSION

4.2.2.1. IRQ_HPD timing

According to eDP standard spec, IRQ_HPD need to setup Low period with 0.5 to 1.0 ms periods and High period over 2.0 ms.

It is necessary to setup low period timing by programing "RG_HPD_LOW[7:0]" bits of HPD_LOW register (0xB011).
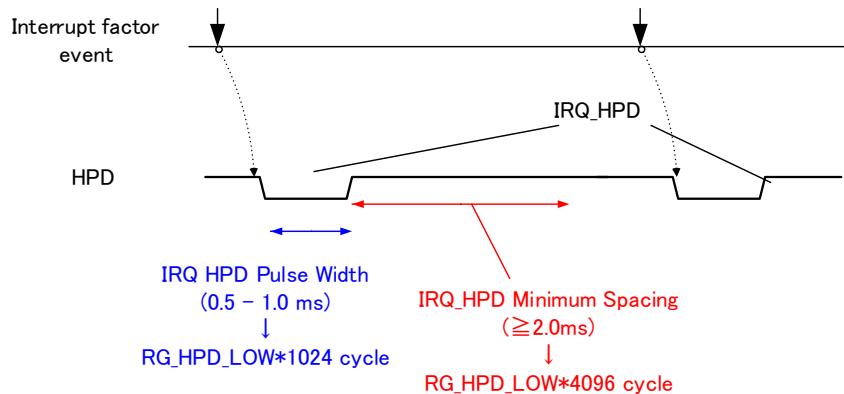
Figure 4-3   IRQ_HPD generate timing (One Interrupt)
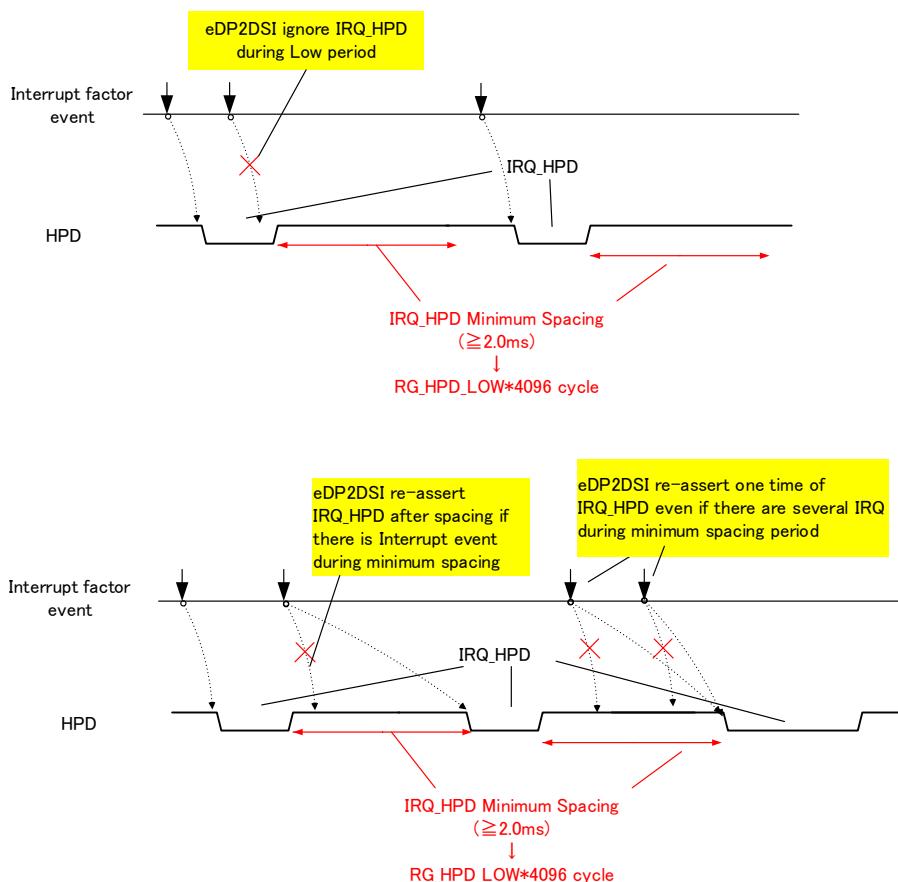
Figure 4-4   IRQ_HPD generate timing (Several Interrupt)

4.2.2.2. Hot Plug Event timing

According to eDP standard spec, HPD pin need to assert Low over 2ms period for Hot Plug event. So it is necessary to set up **RG_HPD_LOW** $\times$ 4096 cycles.
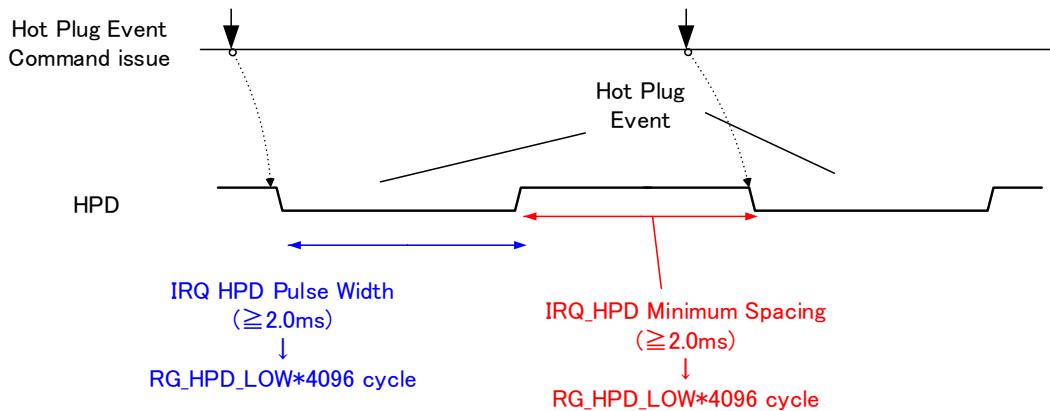
Figure 4-5   Hot Plug event

When TC358860XBG gets both factor of IRQ_HPD and Hot Plug Event command, Hot plug event has priority to issue other IRQ after issuing existing iRQ/Hot plug event.

When it is issued Hot Plug Event first, it will be clear factor of IRQ_HPQ automatically.
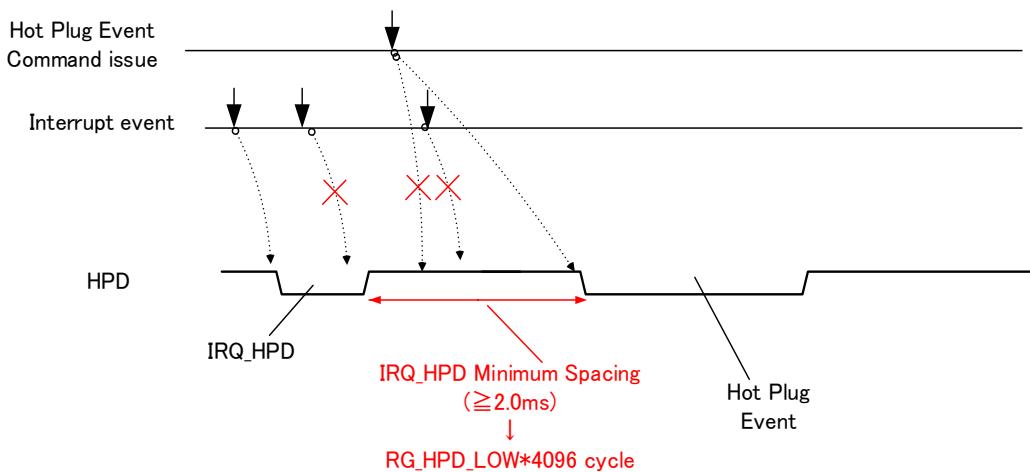
Figure 4-6   IRQ_HPD and Hot Plug event

4.3. Register access

TC358860XBG has several ways to access both internal and external registers from AUX or I^{2}C interface. Following figure shows write register direction, although TC358860XBG has capability to support both write and read access.

1) AUX access to internal registers of TC358860XBG (I^{2}C over AUX)
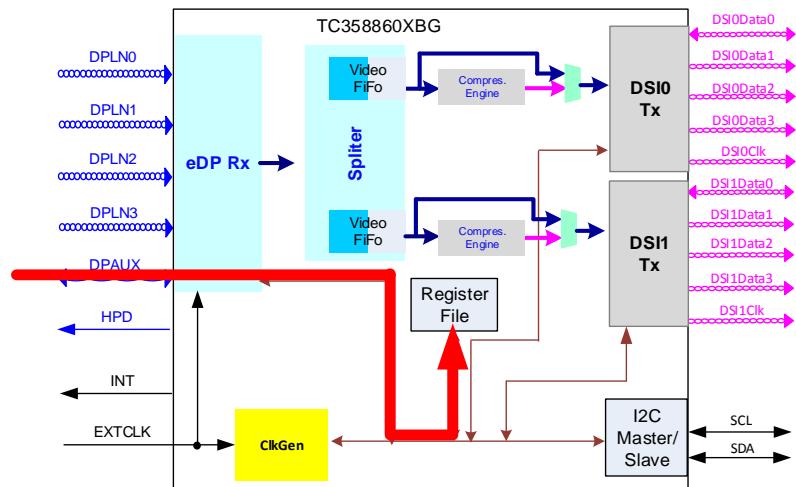
Figure 4-7 AUX access to internal registers 1)

2) AUX access to external registers of I^{2}C devices (I^{2}C over AUX)

HOST can access external I^{2}C devices when configured I^{2}C pins as I^{2}C master. As default, the I/O direction of I^{2}C CLK is input with having I^{2}C slave function. This use case is useful for EDID ROM.
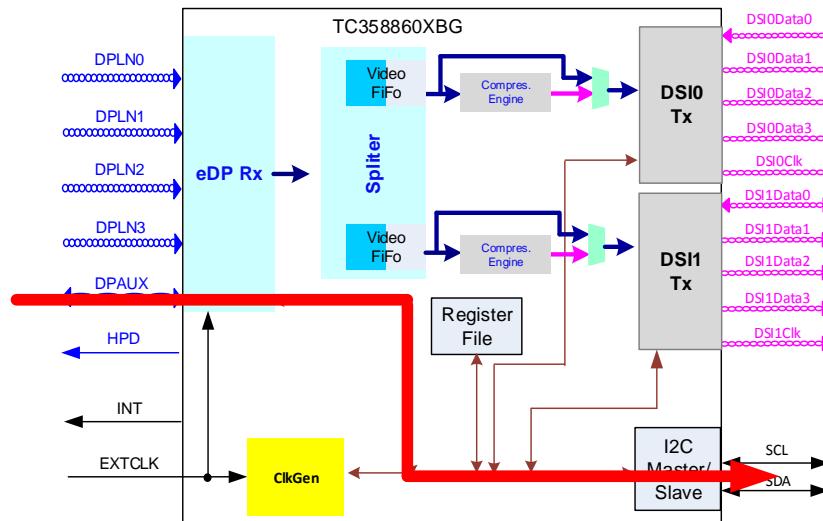
Figure 4-8 AUX access to internal registers 2)

3) AUX Bus Access to external registers of DSI device
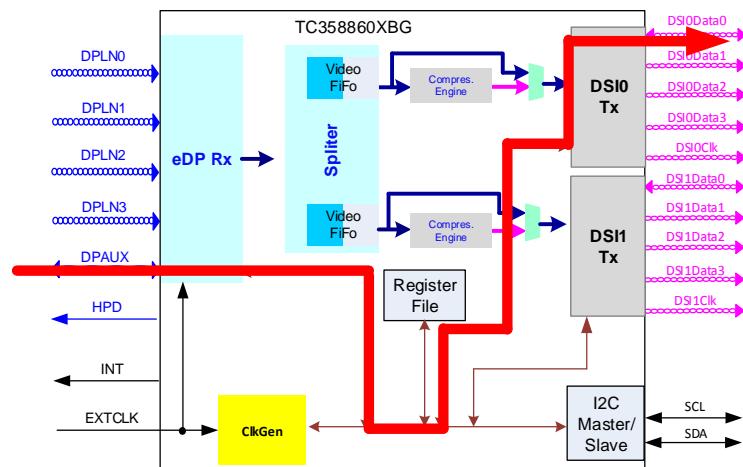
Figure 4-9 AUX access to internal registers 3)
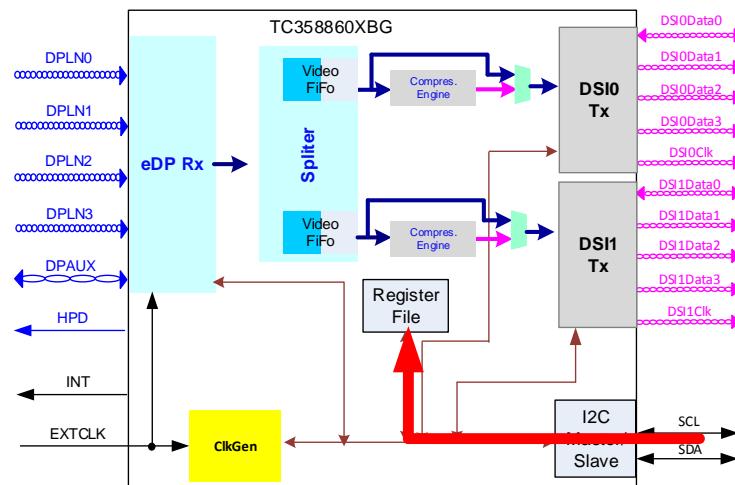
4) I²C Bus Access to TC358860XBG Registers

Figure 4-10 AUX access to internal registers 4)
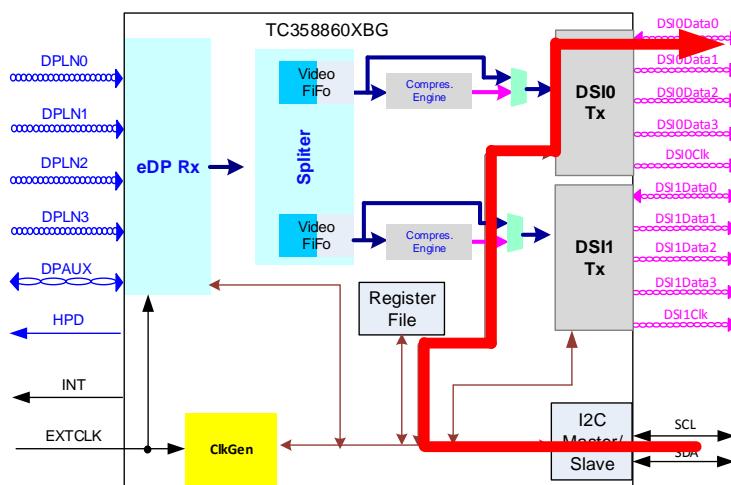
5) I²C Bus Access to external registers of DSI device

Figure 4-11 AUX access to internal registers 5)

4.3.1. AUX Access to TC358860XBG internal Registers

4.3.1.1. I^{2}C-over-AUX Channel

When using AUX channel to program TC358860XBG, eDP source device is expected to use I^{2}C-over-AUX transaction method 2. Please refer to section 2.7 Table 2-71 of VESA DisplayPort Standard version 1.2a for details.

A write and a read access to TC358860XBG's internal registers are given in sections 4.3.1.2 and 4.3.1.3, respectively.

4.3.1.2. I^{2}C-over-AUX Write Example

Here is an example to write TC358860XBG registers starting with address **0x0168** with 3 data words (3 contiguous registers write) 0x67452301, 0xefcdab89, and 0x88885a5a

{CMD, 12'b0, 1'b0, 7-bit Slave Addr}, {Length Byte = 0xd},

{0x01, 0x68, 0x01, 0x23, 0x45, 0x67, 0x89, 0xab, 0xcd, 0xef, 0x5a, 0x5a, 0x88, 0x88}

a. CMD = 4'b0_0_00 indicates I^{2}C, 1-transaction, write operation {I2C_MOT_Write}

b. Slave Address == TC358860XBG I^{2}C Slave Address, indicating access to TC358860XBG internal register address space

c. Length Byte = 0xd indicates there are (13 + 1) bytes of data in this AUX transaction

d. TC358860XBG interprets the first two bytes in the data phase as the beginning internal register address field **0x0168**. The following 4-bytes, 0x67452301, as the data to be written into address **0x0168**. Data words 0xefcdab89 and 0x88885a5a will be written to registers **0x016C** and **0x0170** (address auto increment), respectively.

e. Please note the address field is MSB first while data field is LSB first

4.3.1.3. I^{2}C-over-AUX Read Example

An example of reading 8-byte of data (2 registers) from TC358860XBG registers starts at address 0x0168 is shown below:

1. Host/eDP source performs I^{2}C-over-AUX writes with two bytes of data, 0x0168. TC358860XBG interprets this 2-byte as address offset, similar to that of I^{2}C operation.

   {CMD, 12'b0, 1'b0, 7-bit Slave Addr}, {Length Byte = 0x1},

   {0x01, 0x68}

   a. CMD = 4'b0_0_00 indicates I^{2}C, 1-transaction, write operation {I2C_MOT_Write}

   b. Slave Address == TC358860XBG I^{2}C Slave Address, indicating access to TC358860XBG internal register address space

   c. Length Byte = 0x1 indicates there are (1 + 1) bytes of data in this AUX transaction

   d. 0x0168 is latched into an internal (address) offset register, which is used as the starting read address when an I^{2}C-over-AUX Read command comes, it is auto increment to the next address when more than 4-byte of data being read.

2. Host/eDP source issues read command

   {CMD, 12'b0, 1'b0, 7-bit Slave Addr}, {Length Byte = 0x7}

   a. CMD = 4'b0_0_01 indicates I^{2}C, 1-transaction, read operation {I2C_MOT_Read}

   b. Slave Address == TC358860XBG I^{2}C Slave Address, indicating access to TC358860XBG internal register address space

   c. Length Byte = 0x7 indicates there are (7 + 1) bytes of data in this AUX transaction

3. TC358860XBG returns 8-byte of data

   {I2C_ACK, AUX_ACK, 4'b00, 0x01, 0x23, 0x45, 0x67, 0x89, 0xab, 0xcd, 0xef}

   a. I2C_ACK = 2'b00, AUX_ACK = 2'b00

   b. 8 bytes of data returned, start from the internal offset register, 0x168 = {0x67452301} and address 0x016C = 0xEFCDAB89

4.3.2. I^{2}C Bus Access to TC358860XBG Registers
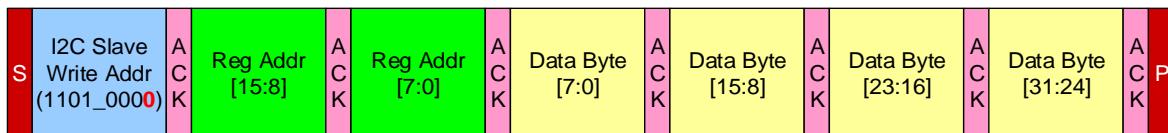
Alternatively, Host can access TC358860XBG registers via the I^{2}C slave port.

1. TC358860XBG I^{2}C bus can run at either standard speed (100 kHz), fast speeds (400 kHz or 1 MHz).

2. The default I^{2}C slave address is 0x68 (1101_000x, x= 0/1 for write/read). Which can be changed to 0x0E (0001_110x, x= 0/1 for write/read) when GPIO0 pin is pulled during power on reset.

3. Please refer to reference 5, I^{2}C bus specification, version 2.1, January 2000, Philips Semiconductor.
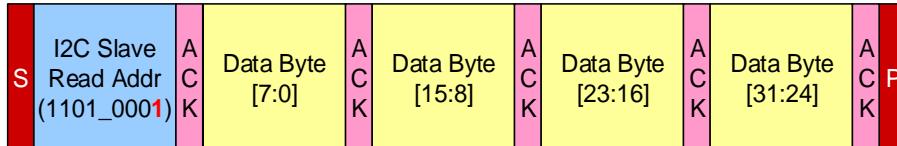
The data byte order used in TC358860XBG I^{2}C bus for write and read transactions are shown Figure 4-12 and

4. Figure 4-13, respectively. Please note the register address is sent MSB first and data field is LSB first.

Figure 4-12   I^{2}C Bus Write Transaction: Register Address/Data Byte Order Expected

Figure 4-13   I^{2}C Bus Read Transaction: Data Byte Order Driven

4.4. DSI Panel Registers Access

DSI panel also needs to be initialized by eDP host/source/Tx after power on reset. TC358860XBG provides a 128-byte command queue, CmdQue, for host to write/issue command. TC358860XBG DSI Tx block fetches data from CmdQue and issues DSI (command) packet to configure panel via DSI link. Host can also read from a 32x4-Byte DSI_RXFIFO (register address 0x20B8, 0x30B8) to obtain the status parameters of panel's. The details on how to use CmdQue and DSI (command) packet capability are described below with examples.

1. By default, the DSI commands are sent via DSI0 link (please refer to section 4.5.1 for the definition of DSI0 and DSI1 links). User can program TC358860XBG to send commands to a specified DSI link in the case two independent LCD controllers are used in the panel. TC358860XBG can also send the same commands simultaneously to both links.

2. A DSI packet with header is shown in Figure 4-14. Host is responsible to write the whole DSI packet, including header bytes, into the CmdQue. ECC and Checksum will be appended by TC358860XBG before sending out via DSI link.

3. TC358860XBG interprets the 1st data in CmdQue as the packet Data ID, 2nd and 3rd bytes as Word Count for a long packet (or Data 0 and Data 1 for a short packet). The 4th byte as Data 0 for a long packet, 5th byte as Data 1... as indicated in the bottom of Figure 4-14.

4. CmdQue is a read/write register (address = 0x22fc to 0x23fc) located in TC358860XBG's register space. A write to registers 0xabcd push data into command queue. While a read to register 0xabcd requests TC358860XBG to report CmdQue content to eDP host.

5. TC358860XBG can transmit DSI command packet in either LP or HS mode, depending on panel's capability.

6. In addition to initialize the panel, host can change panel parameters dynamically when video stream is active. TC358860XBG will issue DSI command packets during video vertical blank period. HS DSI command packets are recommended when muxing with video streams.

7. CmdQue is used to issue one panel configuration/command at a time, host is expected to wait for TC358860XBG finishing DSI command packet transaction before issuing another command. TC358860XBG can generate an interrupt, via HPD pin, when a command has been successfully sent out.
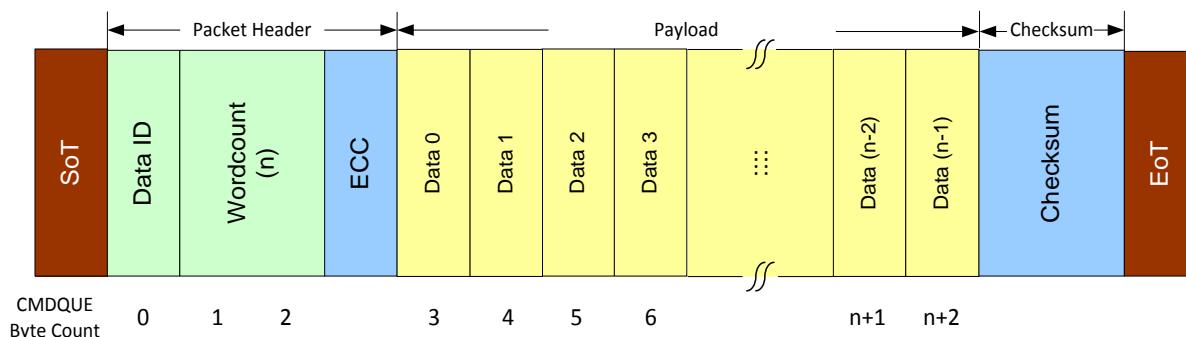
Figure 4-14   DSI Packet Byte Location in CmdQue

4.4.1. Issue DCS Short Command 0x29 to Turn On Panel

*{CMD, 12'b0, 1'b0, 7-bit Slave Addr}, {Length Byte = 0x4}, {**0xAB, 0xCD**, 0x05, 0x29, 0x00}*

a. CMD = 4'b0_0_00 indicates I²C, 1-transaction, write operation {I2C_MOT_Write}

    i. MOT, middle-of-transaction, bit

    MOT = 0, the end of AUX transaction.

    MOT = 1, middle-of-transaction more data will come for the same DSI packet

b. Slave Address == TC358860XBG I²C Slave Address, indicating access to TC358860XBG internal register address space, 0xABCD(CmdQue)

c. Length Byte = 0x4 indicates there are (4 + 1) bytes of data in this AUX transaction

d. Write to command queue **0xABCD,** with data bytes 0x05, 0x29 , 0x00

    i. Data ID = 0x05 ➔ DCS Short Write command, no parameter

    ii. DCS Command: 0x29 ➔ set_display_on, No parameter

    iii. DCS set_display_on command without parameter ➔ 0x00

e. After receiving/pushing 3 (Length Byte + 1 – 2) byte of data into CmdQue and MOT = 0, TC358860XBG issues DSI packet to flush out the CmdQue.

    i. TC358860XBG does Not interpret CmdQue data, the DSI Tx of panel should decode Data ID byte and decode the command accordingly.

    ii. Depending on the bytes of data in CmdQue, TC358860XBG will issue a DSI short or long packet and appends ECC, and Checksum if necessary.

    iii. Here 3-byte of data is in CmdQue at the end of AUX transaction. ➔ A short DSI packet will be issued by TC358860XBG DSI Tx with ECC appended.

4.4.2. Issue Generic Long Write Command to Panel with 32-byte of Data

Since the maximum data length for each AUX transaction is 16-byte. Host might need to break one generic long write command into multiple transactions. Middle-of-transaction, MOT, bit is used to indicate the end of transactions. MOT is asserted for the all transactions except the last one. When receiving MOT = 1'b0, TC358860XBG recognize it is the end of AUX transaction. It starts Generic Long Write Command packet on DSI link.

1st Transaction

{CMD, 12'b0, 1'b0, 7-bit Slave Addr}, {Length Byte = 0x0f},

*{**0xAB, 0xCD**, 0x29, 0x20, 0x00, Data0, Data1…. Data10}*

a. CMD = 4'b0_1_00 indicates I²C, middle-of-transaction, write operation {I2C_MOT_Write}

    i. MOT, middle-of-transaction, bit

    MOT = 0, the end of AUX transaction.

    MOT = 1, middle-of-transaction more data will come for the same DSI packet

b. Slave Address == TC358860XBG I²C Slave Address, indicating access to TC358860XBG internal register address space, 0xabcd (CmdQue)

c. Length Byte = 0x0f indicates there are (15 + 1) bytes of data in this AUX transaction

d. Write to command queue **0xABCD,** with data bytes 0x29, 0x20, 0x00, Data0, Data1…. Data10

    i. Data ID = 0x29 ➔ Generic Long Write Command

    ii. Word Count: 0x0020 ➔ 32-byte of data in the Generic Long Write Command

    iii.   The first 11 bytes of data

e. CmdQue_wrPtr = 14, indicating 14-byte of data has been written in to the queue. More data is coming since MOT = 1

2st Transaction

{CMD, 12'b0, 1'b0, 7-bit Slave Addr}, {Length Byte = 0x0f},

{Data11, Data12…. Data26}

a. CMD = 4'b0_1_00 indicates I²C, middle-of-transaction, write operation {I2C_MOT_Write}

b. Slave Address == TC358860XBG I²C Slave Address, indicating access to TC358860XBG internal register address space, 0xabcd (CmdQue) is implied (continue from last transaction).

c. Next 16-byte of data

d. CmdQue_wrPtr = 30, indicating total of 30 bytes of data has been written in to the queue. More data is coming since MOT = 1

3rd (and last) Transaction

{CMD, 12'b0, 1'b0, 7-bit Slave Addr}, {Length Byte = 0x04},

{Data27, Data28…. Data31}

a. CMD = 4'b0_0_00 indicates I²C, end-of-transaction, write operation {I2C_MOT_Write}

b. Slave Address == TC358860XBG I²C Slave Address, indicating access to TC358860XBG internal register address space, 0xABCD (CmdQue)

c. CmdQue address 0xabcd is not sent, only the final 5-byte of data is sent

d. CmdQue_wrPtr = 35, indicates 5 more bytes of data has been written in to the queue.

    i.   The last AUX transaction is indicated by MOT = 0

    ii.   Here 35 bytes of data is in CmdQue at the end of AUX transaction. ➔ A long DSI packet will be issued by TC358860XBG.

    iii.   TC358860XBG DSI Tx fetches the first 3 bytes of data from CmdQue appended ECC to form the header of the command. The remaining 32 bytes of data plus its calculated Checksum will be added as payload of the packet as shown in Figure 4-14.

4.4.3. <mark>Issue a Generic Read Command with 2 Parameters to Read Panel Status</mark>

(To be Updated)

Assume panel has a status register, PStatus, located at its address space PStatus_Addr and with four bytes of Data, PStatus_Data[3:0]. The following steps are required for host to read PStatus_Data.

4.4.3.1. Host writes a read PStatus command into CmdQue

{CMD, 12'b0, 1'b0, 7-bit Slave Addr}, {Length Byte = 0x04},

*{**0xab, 0xcd**, 0x24, PStatus_Addr_MSB, PStatus_Addr_LSB}*

a. CMD = 4'b0_0_00 indicates I²C, 1-transaction, write operation {I2C_MOT_Write}

b. Slave Address == TC358860XBG I²C Slave Address, indicating access to TC358860XBG internal register address space, 0xabcd (CmdQue)

c. Length Byte = 0x04 indicates there are (4 + 1) bytes of data in this AUX transaction

d. Write to command queue **0xABCD,** with data bytes *0x24, PStatus_Addr_MSB, PStatus_Addr_LSB*

    i.   Data ID = 0x24 ➔ Generic Read Command with 2 parameters

ii.   Two parameters for this short Generic Read Packet {*PStatus_Addr_MSB, PStatus_Addr_LSB},* panel status register address

4.4.3.2. TC358860XBG starts DSI Tx Read PStatus

a.   TC358860XBG sends out a DSI short packet with {0x24, PStatus_Addr_MSB, PStatus_Addr_LSB, ECC} and performs BTA, Bus Turn Around, for Panel to drive data back.

b.   Panel LCD driver/DSI Tx interprets and response with required data.

c.   After performing DSI link BTA (Bus Turn Around), PStatus_Data[31:0] will be fetched into CmdQue for host to read

4.4.3.3. Host issues a Read Command to CmdQue

Host needs to check and make sure CmdQue read data is ready before issuing read command to CmdQue. The procedure is the same as described in section 4.3.1.3.

1.   Host/eDP source performs I^2C-over-AUX writes with two bytes of data, 0xabcd, CmdQue address. TC358860XBG interprets this 2-byte as address offset, similar to I^2C operation.

{CMD, 12'b0, 1'b0, 7-bit Slave Addr}, {Length Byte = 0x1},

{0xAB, 0xCD}

a.   CMD = 4'b0_0_00 indicates I^2C, 1-transaction, write operation {I2C_MOT_Write}

b.   Slave Address == TC358860XBG I^2C Slave Address, indicating access to TC358860XBG internal register address space

c.   Length Byte = 0x1 indicates there are (1 + 1) bytes of data in this AUX transaction

d.   0xABCD is latched into an internal (address) offset register, which is used as the starting read address when an I^2C-over-AUX Read command comes. Please note address 0xabcd will Not auto increment when more than 4-byte of data is read

2.   Host issues read command (to offset is set to CmdQue address, 0xabcd)

{CMD, 12'b0, 1'b0, 7-bit Slave Addr}, {Length Byte = 0x3}

a.   CMD = 4'b0_0_01 indicates I^2C, 1-transaction, read operation {I2C_MOT_Read}

b.   Slave Address == TC358860XBG I^2C Slave Address, indicating access to TC358860XBG internal register address space

c.   Length Byte = 0x3 indicates there are (3 + 1) bytes of data in this AUX transaction

4.4.3.4. TC358860XBG returns 4-bytes of read data to host

{I2C_ACK, AUX_ACK, 4'b00, PStatus_Data0, PStatus_Data1, PStatus_Data2, PStatus_Data3}

a.   I2C_ACK = 2'b00, AUX_ACK = 2'b00

b.   4 bytes of data start from address 0xabcd = PStatus_Data[31:0]

4.5. Dual DSI Links Support

DSI host can split a long line of video data into two (streams of) DSI video packets, one (stream of) video packet per DSI link. The splitting of one (line of) video stream is performed by left and right halves. Left half data is sent to link0, DSI0, while the right one is routed to link1, DSI1. Figure 4-15 Combination of Dual DSI link function shows combination of dual DSI link function using Dummy pixel, Overlap pixel and DSI port swap.
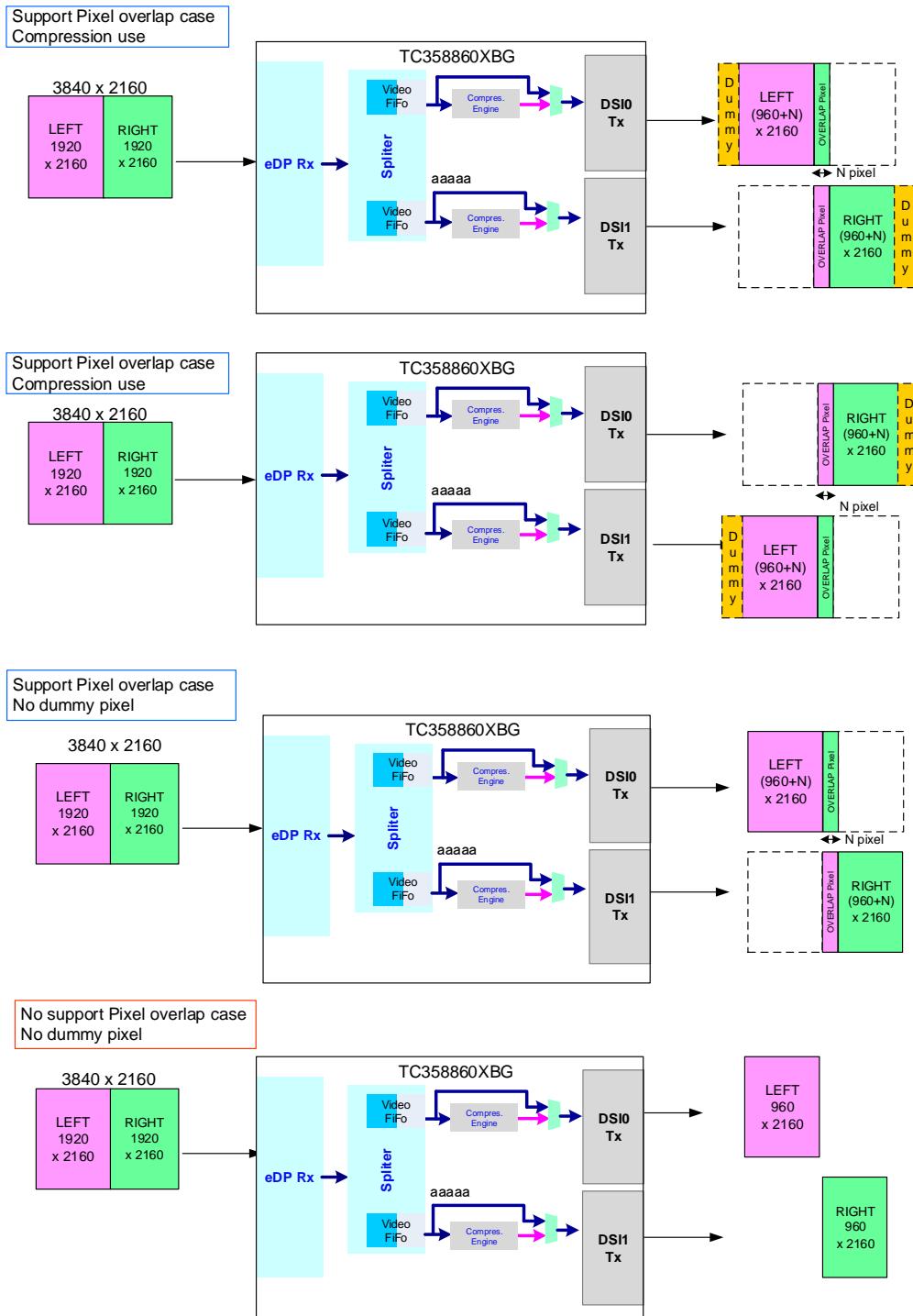
Figure 4-15   Combination of Dual DSI link function

4.5.1. Dual Links Features

1. DSI0 (the link carries left half of data) can be assigned/programmed to either of the two DSITx ports

2. The skew between DSI0 and DSI1 can be programmed by register (DSI0VSDelay/DSI1VSDelay and DSI0HBPR/DSI1HBPR shown in Figure 4-17)

3. By default, the DSI commands are sent via DSI0 link. It can be switched to send via DSI1 link in order to support panels using two independent DSI Tx LCD controllers. In addition, user can program TC358860XBG to send commands to both DSI links simultaneously.

    a. This feature is used to prevent panel refresh skew when a panel exhibits two DSI Tx LCD controllers and dynamical panel refresh update is required.

4. The maximum length of each half is limited to 2048-pixel at 24bpp due to the 4Gbps D-PHY link speed per lane

5. The splitting is shown graphically in Figure 4-16.

6. Please note there is 2-line time delay between eDP Rx input and MIPI-Tx output in general. It becomes 3-line time delay if compression engine is used.

7. Overlapped splitting shown in Figure 4-19 is also supported.

    a. The number of pixels overlapped (and dummy) can be programmed from 0 to 32 pixels.

        i.   0-pixel means no overlapping.

        ii. Only even pixel number is allowed.

    b. The color of dummy pixels can be user programmable.

    c. TC358860XBG has an option for not sending the dummy pixels.
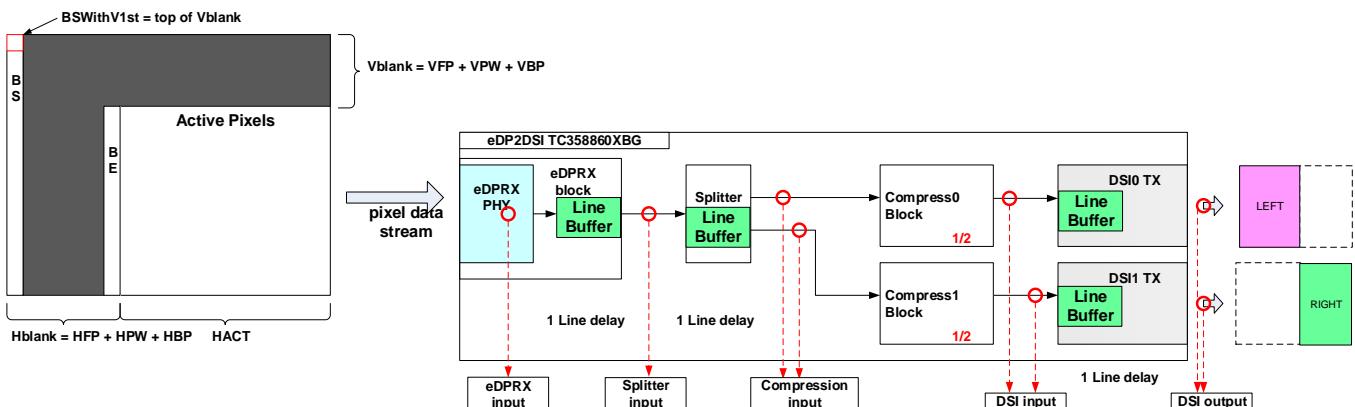
Figure 4-16   Pixel data flow
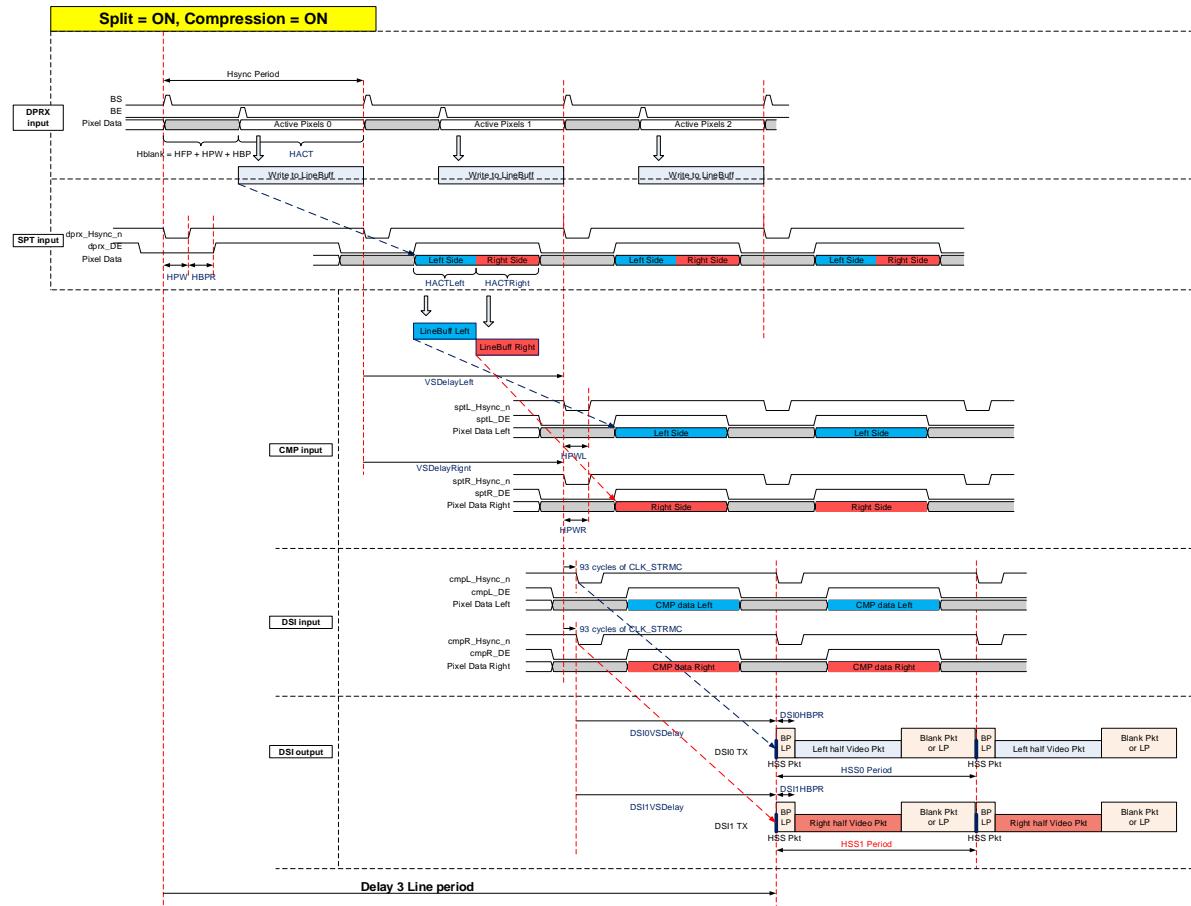
Figure 4-17 **Pixel data flow for Dual DSI Link with Compression**
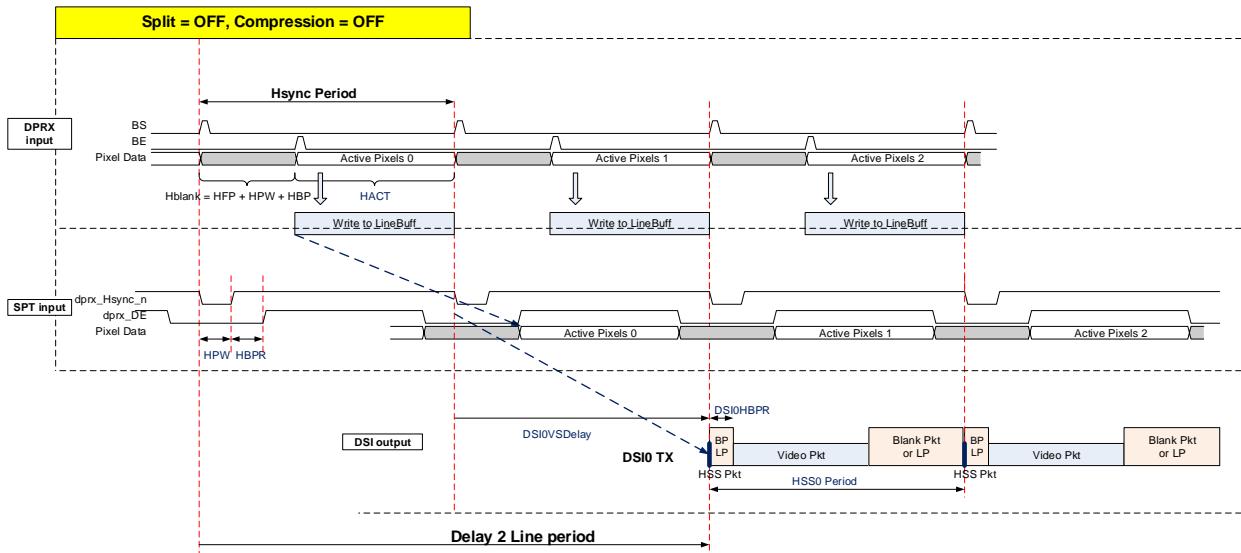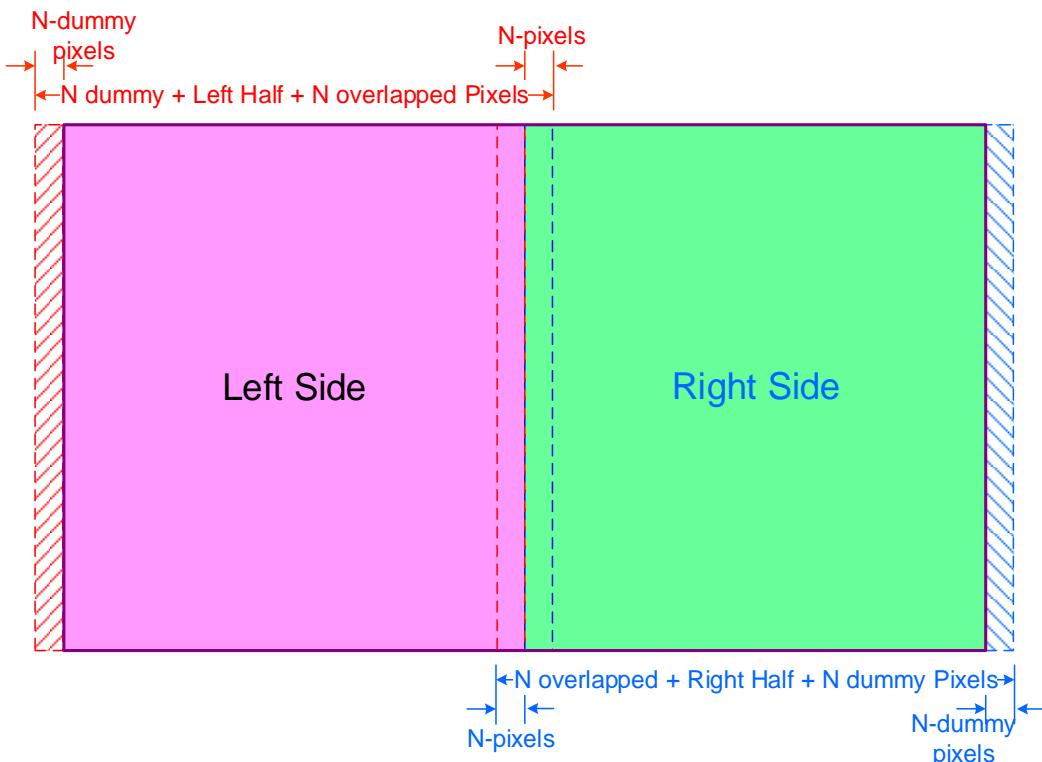
Figure 4-18 **Pixel data flow for Single DSI Link without Compression**

N-dummy pixels

N-pixels

N dummy + Left Half + N overlapped Pixels

Left Side

Right Side

N overlapped + Right Half + N dummy Pixels

N-pixels

N-dummy pixels

There is option not to transfer dummy pixels and overlap pixels

Figure 4-19   Line Overlap Splitting in Dual DSI Link

4.5.2. Synchronous Video Timing

TC358860XBG synchronizes its video timing with that of eDP host's line-by-line. It locks DSI line VSS/HSS (Vertical/Horizontal Sync Start) packets to the leading edge of eDP Rx recovered/generated V/HSyn pulses. By tracking/locking to the leading edge of V/HSync, TC358860XBG assures <Link0 HSS_0 period> = <Link1 HSS_1 period> = <eDP Hsync period> as shown in Figure 4-18.

4.6. Video stream

4.6.1. Compression Operation

The bandwidth (BW) requirement for a 4K 24-bit video stream @60fps is around 12Gbps. TC358860XBG with 4 eDP Rx main links running at 5.4Gbps/link should be able to receive the 4K video stream. However, the output bandwidth of dual DSI links is only 8Gbps, which is not sufficient to carry the 4K video stream @60fps. To overcome this 8Gbps bandwidth limitation, a 2-to-1 compression engine is provided to compress one line of video data into one half of its original size.

The 2-to-1 compressed 4K video streams can be easily fitted into dual DSI links' 8Gbps BW. The compressed video is expected to be decompressed by panel's LCD controller before displaying. The 2-to-1 compressed/de-compressed algorithm can produce visual lossless video stream.
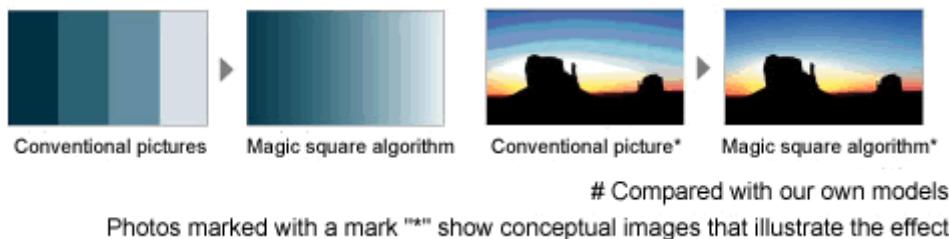
4.6.2. Magic Square Algorithm

When the display panel's color depth capability is less than that of the input data, say sending RGB888 data to 18-bit display panel, the number of bits of display need to be reduced. With the Toshiba Magic Square algorithm, an RGB666 18-bit LCD panel can produce a display quality almost equivalent to that of an RGB888 24-bit LCD panel.

For example, when Magic Square algorithm is enabled the red component of the RGB666 output becomes either "R [7:2]" or "R [7:2] + 1". The ratio of these two values depends on the horizontal and vertical position and the

display timing. With this changing pixel value, human eye senses the red color component as "R [7:2]", "R [7:2] + 0.25", "R [7:2] + 0.5" and "R [7:2] + 0.75". Therefore, the color depth for the human eye becomes almost those of RGB888 data.

By employing Toshiba's Magic Square algorithm the color graduation is increased significantly compared to 18-bit RGB666 data. The following figure shows 2 conceptual examples of the effect from the Magic Square algorithm.

Conventional pictures   Magic square algorithm   Conventional picture*   Magic square algorithm*

\# Compared with our own models.

Photos marked with a mark "*" show conceptual images that illustrate the effect.
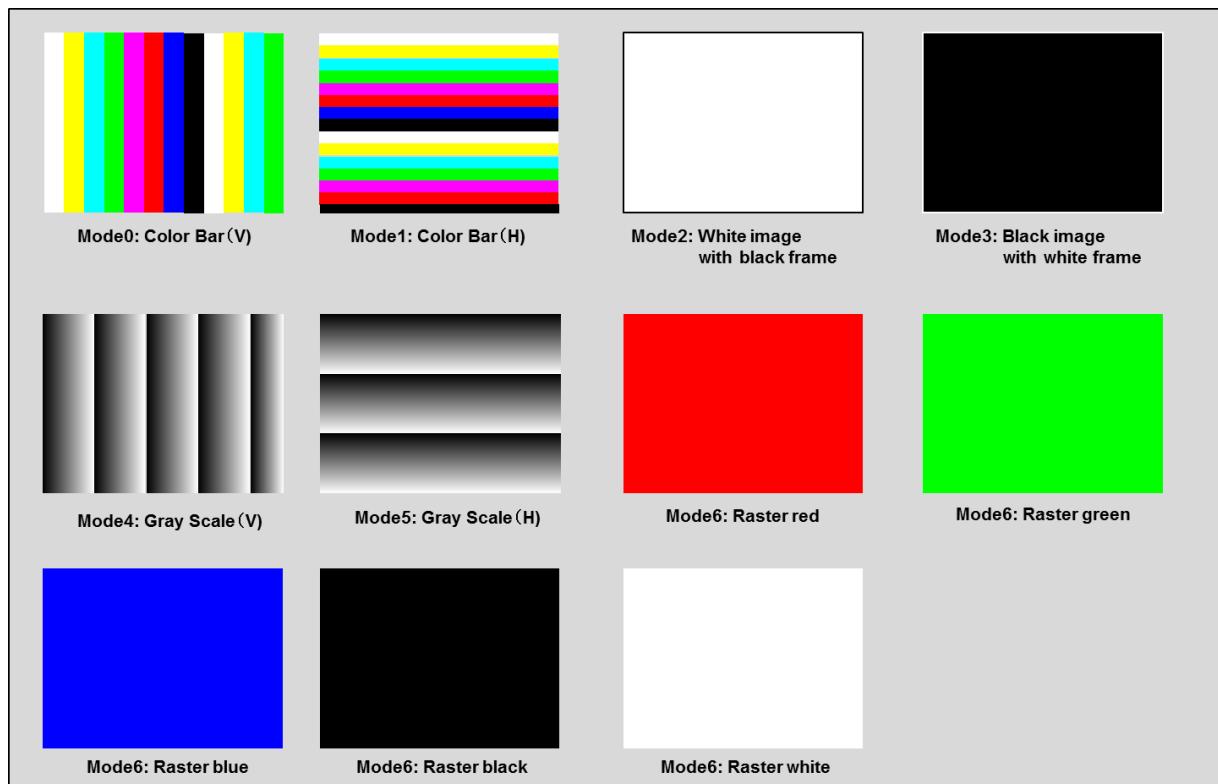
Figure 4-20   Magic Square Algorithm Effect

Thus, Magic Square algorithm may be enabled when the chip drives the DSI output in RGB666 format.

4.6.3. Color bar

TC358860XBG has several color bar output function which is for mainly debug purpose. Without input data from eDP-RX, TC358860XBG generate color bar output by setting several registers (Common registers CBR1*_**** : 0x0400 to 0x0510).

Following color bar image is example.

Figure 4-21　Color bar output (Example)

4.7. GPIO

TC358860XBG supports 4 GPIO pins that are individually configurable as either input or output and Pull-Up/Down.

- Host configure the direction of GPIO pins by writing to "**GPIOC(Address 0x0080)**" register. By default all GPIOs are in input mode.
- Host configure Pull-Up/Down of GPIO pins by writing to **"IOB_CTRL2.GPIO*_P" (address 0x0804)** register. By default the GPIOs are in input mode.

Table 4.4   Transmit and Driver disable state control of GPIO

OEN (GPIOC.GPIO*_oe)	Driver disable control		DIN	Output I/O
	P[1]	P[0]		
0	-	-	0	0
			1	1
1(default)	0	0	-	Z (Normal)
	0	1	-	Pull-Up
	1	0	-	Pull-Down(Default)
	1	1	-	Repeater

- Host configure Drive strength of GPIO when configured output direction by writing to **"IOB_CTRL2.GPIO*_E"** register. BY default the GPIO are using 4mA drive strength.

Table 4.5   Output drive strength control of GPIO

Output Drive Strength		Output Drive Strength
E[1]	E[0]	
0	0	2 mA
0	1	4 mA (Default)
1	0	8 mA
1	1	12 mA

- Host configure slew rate control by writing to **"IOB_CTRL2.GPIO*_SR"** register, By default the GPIO are in slow rate(0).
- As input, the logic state on the GPIO pins are reflected in the "**GPIOI**" register which Host can read.
- When configured as output, the GPIO pins are driven by the state of "**GPIOO**" register which Host can write to.
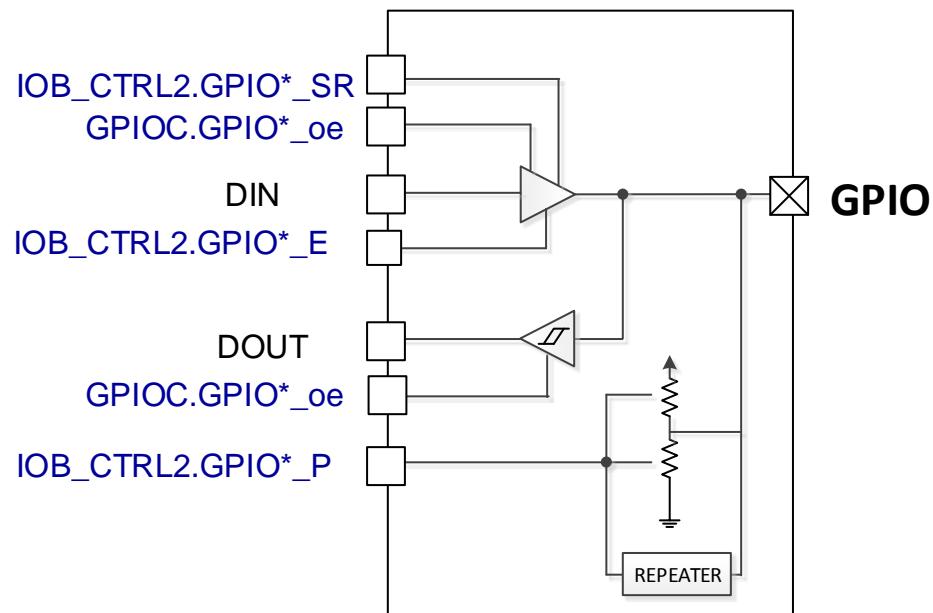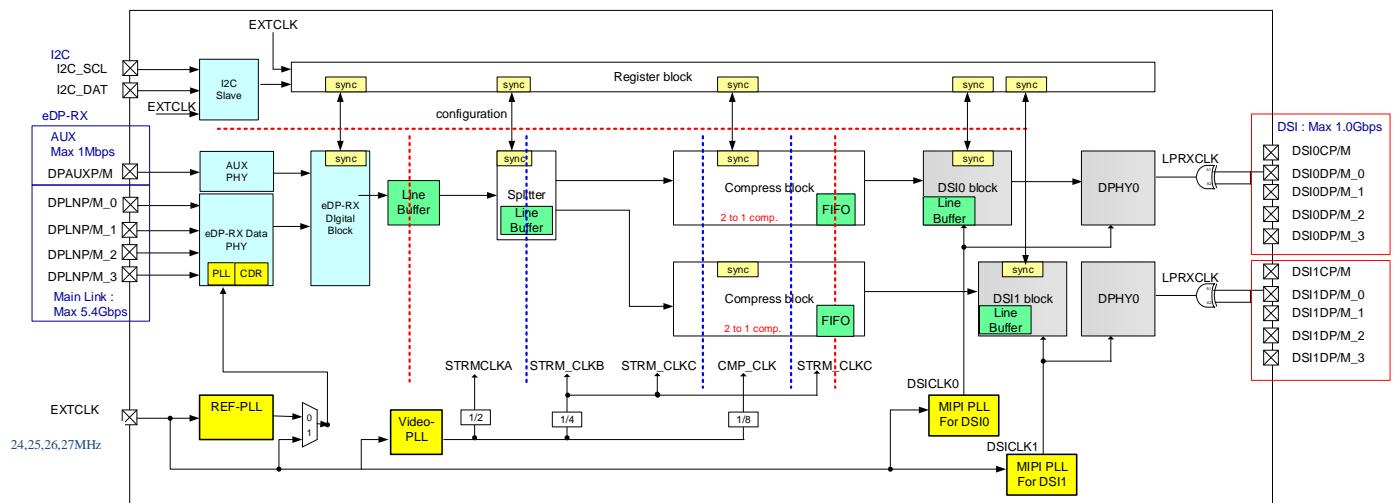
Figure 4-22   GPIO configuration

5. Clock Structure, Interrupt and Power Management

5.1. Clock Source and Structure

5.2. Power On Sequence

The following sequence should happen before TC358860XBG is able to operate properly:

1. Provide voltage and clock sources to TC358860XBG.
   - Please keep all the input signals at either "Hi-z" or "logic low" state before powering on TC358860XBG.
2. For core and I/O voltage supply sequence, there are two ways: first it turn on core power VDDC(1.1V) source, then VDDIO (1.8V/3.3V) power secondary. Another way is that it turns on VDDIO(1.8V/3.3V)power source first and VDDC(1.1V) power secondary. In this case internal Power-on logic disable to output driver.
3. It turn on Analog PHY(1.8V/1.2V) for both eDP and DPHY.
4. REFCLK clock source can be used 24,25,26 and 27MHz.
5. De-assert RESET_N after t2 timing
6. HPD from TC358860XBG become from Low to High which compliant to eDP spec
7. The timing parameters for Figure 5-1are tabulated in Table 5.1.
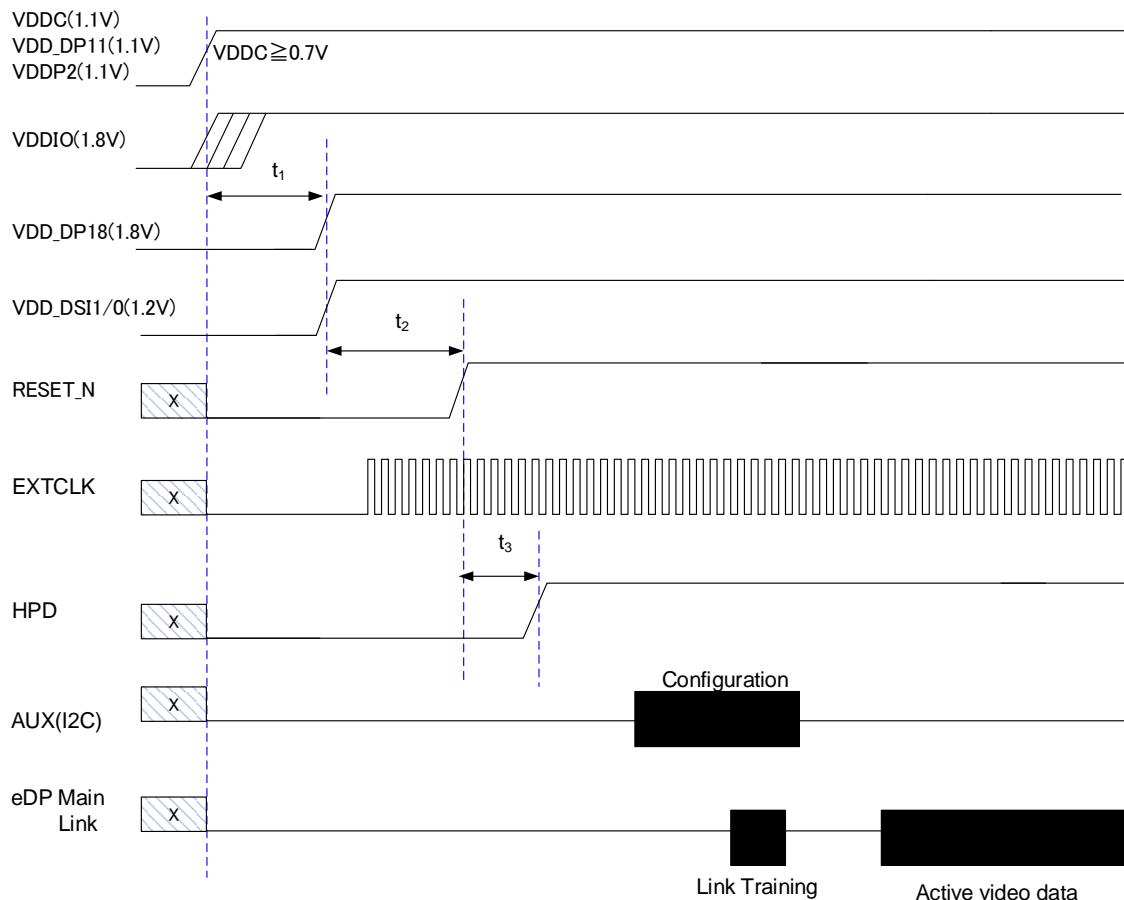
Figure 5-1   Power on Sequence

Table 5.1   Power On Sequence Timing

Parameters	Description	Min.	Typ.	Max.	Units
EXTCLK	External clock frequency	24	--	27	MHz
t_1	Delay from VDDC to VDD_DP18, VDD_DSI1/0	0	-	-	μs
t_2	Delay from VDD_DSI1/0 to RESET_N	100	-	-	μs
t_3	Delay from RESET_N to HPD	-	-	200	μs

5.3. <mark>Power Off Sequence</mark>

The following sequence should happen before TC358860XBG is able to operate properly:
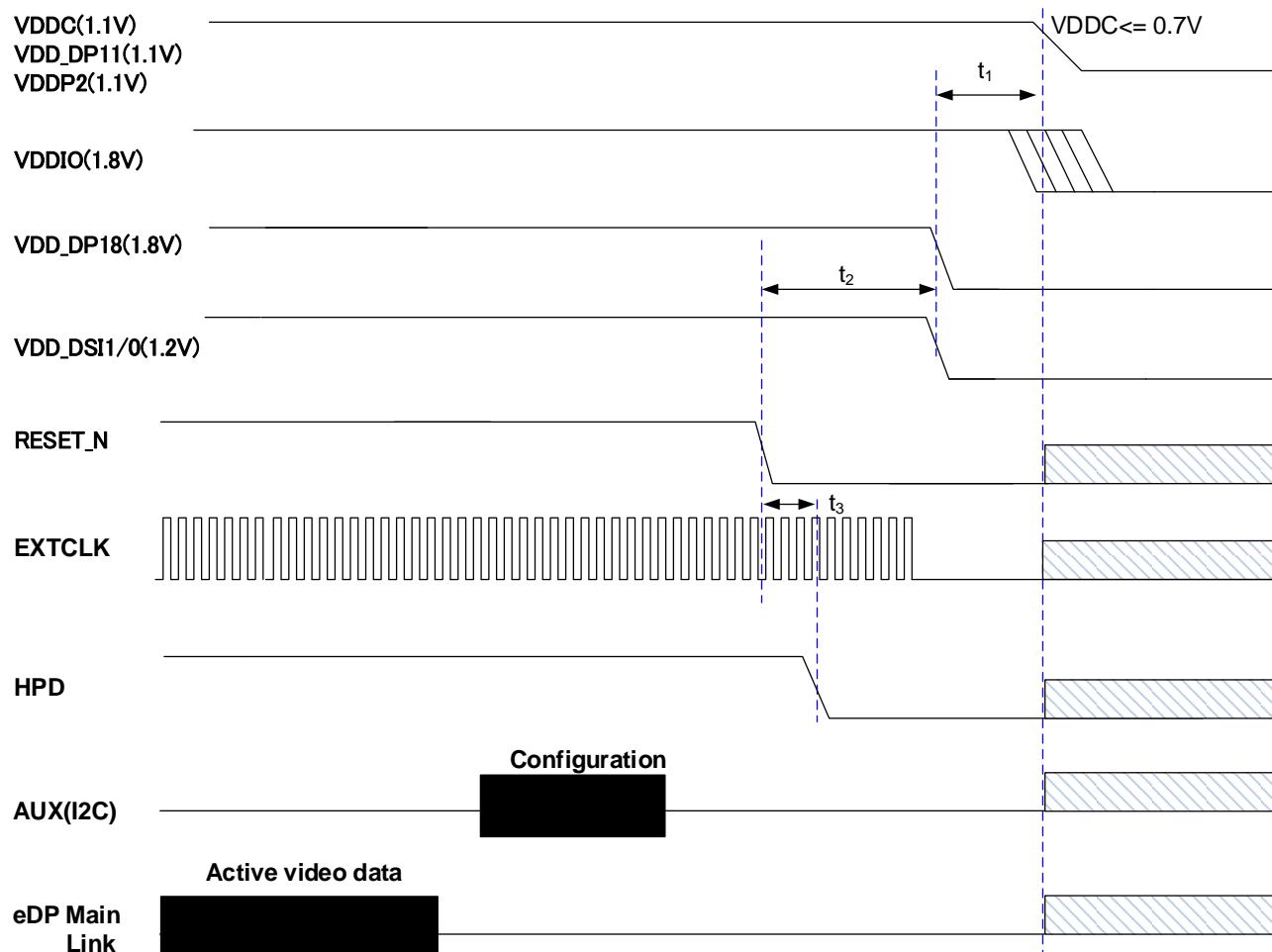
Figure 5-2　Power off Sequence

Table 5.2　Power Off Sequence Timing

Parameters	Description	Min.	Typ.	Max.	Units
t_1	Delay from VDDC to VDD_DP18, VDD_DSI1/0	0	-	-	µs
t_2	Delay from VDD_DSI1/0 to RESET_N	100	-	-	µs
t_3	Delay from RESET_N to HPD	4	-	8	EXTCLK

6. Registers

6.1. Register Map

Table 6.1   Global Register Map

Segment Address	Block
0x0000 – 0x0FFF	Common Registers (System and Video block)
0x1000 – 0x1FFF	Boot Registers
0x2000 – 0x21FF	DSITx0 Registers
0x2200 – 0x23FF	DSITx0 Command Queue Registers
0x2400 – 0x27FF	Reserved
0x2800 – 0x2FFF	DSITx0 Common Registers
0x3000 – 0x31FF	DSITx1 Registers
0x3200 – 0x33FF	DSITx1 Command Queue Registers
0x3400 – 0x37FF	Reserved
0x3800 – 0x3FFF	DSITx1 Common Registers
0x4000 – 0x41FF	DSITx Global Registers
0x4200 – 0x43FF	DSITx Global command queue Registers
0x4400 – 0x4FFF	Reserved
0x5000 – 0x5FFF	IC Test Registers
0x6000 – 0x6FFF	Reserved
0x7000 – 0x7FFF	eDPRX Port Common registers
0x8000 – 0xAFFF	eDPRX DPCD registers
0xB000 – 0xB1FF	eDPRX Common registers
0xB200 – 0xB3FF	eDPRX Link registers
0xB400 – 0xB5FF	eDPRX ALMP registers
0xB600 – 0xB7FF	eDPRX PHY1 registers
0xB800 – 0xBFCB	eDPRX PHY2 registers
0xBFCC–0xBFFF	eDPRX test registers

Following table gives a summary of the address map in terms of main modules.

Table 6.2   Detail Register Map

Group	Address	Register	Initial	Description
Common registers	0x0000	REFClockSel	0x0000_0000	PLL reference clock select
	0x0004	DPREFPLLCTRL0	0x0000_0180	eDPRX PLL test register
	0x0008	DPREFPLLCTRL1	0x0000_0000	eDPRX PLL charge pump parameter
	0x000C	DPREFPLLCTRL2	0x0000_0000	eDPRX PLL parameter register
	0x0010	DPREFPLLCTRL3	0x0000_0000	eDPRX PLL clock enable
	0x0014	ClockSel	0x0000_0003	Internal clock select
	0x0018	ClockEN	0x0000_0000	Internal clock enable
	0x001C	SoftReset	0x0000_0001	Internal software reset
	0x0020	SRAMPG	0x0000_0000	SRAM power gating
	0x0024	ROMPG	0x0000_0000	ROM power gating
	0x0028 – 0x007F	Reserved	-	-
	0x0080	GPIOC	0x0000_0000	GPIO direction control
	0x0084	GPIOO	0x0000_0000	GPIO output data
	0x0088	GPIOI	0x0000_0000	GPIO input data
	0x008C	GPIOOUTMODE	0x0000_0000	GPIO test register
	0x0090 – 0x009F	Reserved	-	-
	0x00A0	IntEn	0x0000_0000	Interrupt enable
	0x00A4	IntMon	0x0000_0000	Interrupt monitor
	0x00A8	IntMonRAW	0x0000_0000	Interrupt raw data
	0x00AC	Reserved	-	-
	0x00B0	I2CMD_SEL	0x0000_0000	I2C mode select
	0x00B4 – 0x00FF	Reserved	-	-
	0x0100	VIDEOMODE	0x0F01_0000	Video mode select
	0x0104	SPTPIX_LEFT	0x0000_0000	Overlap/Dummy pixel setting register (left side)
	0x0108	VPCTRL_LEFT	0x0000_0000	Video path control (left side)
	0x010C	HTIM1_LEFT	0x0000_0004	Horizontal Timing control (left side)
	0x0110	HTIM2_LEFT	0x0000_0800	Horizontal Timing control (left side)
	0x0114	VTIM1_LEFT	0x0000_0004	Vertical timing control (left side)
	0x0118	SPTPIX_RIGHT	0x0000_0000	Overlap/Dummy pixel setting register (right side)
	0x011C	VPCTRL_RIGHT	0x0000_0000	Video path control (right side)
	0x0120	HTIM1_RIGHT	0x0000_0004	Horizontal Timing control (right side)
	0x0124	HTIM2_RIGHT	0x0000_0800	Horizontal Timing control (right side)
	0x0128	VTIM1_RIGHT	0x0000_0004	Vertical timing control (right side)
	0x012C – 0x013B	Reserved	-	-
	0x013C	SPTDUMMY_COLOR	0x0000_0000	Dummy pixel color setting
	0x0140	DPRXMode	0x0000_0000	Sync timing control

Group	Address	Register	Initial	Description
	0x0144	DPRX_HTIM1	0x0050_0002	eDPRX Horizontal timing control
	0x0148	DPRX_HTIM2	0x0000_1000	eDPRX Horizontal timing control
	0x014C	DPRX_VTIM1	0x0000_0002	eDPRX Vertical timing control
	0x0150	DPRX_VTIM2	0x0010_0000	eDPRX Vertical timing control
	0x0154	DPRXVideoEn	0x0000_0000	eDPRX Video transmission start register
	0x0158 – 0x017F	Reserved	-	-
	0x0180	ChipInfo	0x0860_0000	Chip ID and Revision ID
	0x0184 – 0x01FF	Reserved	-	-
	0x0200	I2CSetting0	0x0080_0001	I2C test register
	0x0204	I2CDPSetting0	0x0080_0001	I2C test register
	0x0208 – 0x027F	Reserved	-	-
	0x0280	CMP0_COMP_TEST	0x0000_0000	Compressor test register
	0x0284	CMP0_PRE_SWAP	0x0054_3210	Compressor test register
	0x0288	CMP0_POST_SWAP	0x7654_3210	Compressor test register
	0x028C	Reserved	-	-
	0x0290	CMP1_COMP_TEST	0x0000_0000	Compressor test register
	0x0294	CMP1_PRE_SWAP	0x0054_3210	Compressor test register
	0x0298	CMP1_POST_SWAP	0x7654_3210	Compressor test register
	0x029C – 0x02FF	Reserved	-	-
Common registers	0x0300	CBR00_HTIM1	0x0020_0004	Color bar generator00 horizontal timing control (for debug)
	0x0304	CBR00_HTIM2	0x0020_1000	Color bar generator00 horizontal timing control (for debug)
	0x0308	CBR00_VTIM1	0x0004_0004	Color bar generator00 vertical timing control (for debug)
	0x030C	CBR00_VTIM2	0x0004_0800	Color bar generator00 vertical timing control (for debug)
	0x0310	CBR00_MODE	0x0000_0000	Color bar generator00 image data select (for debug)
	0x0314	CBR00_COLOR	0x0000_0000	Color bar generator00 raster color data setting (for debug)
	0x0318	CBR00_ENABLE	0x0000_0000	Color bar generator00 enable register (for debug)
	0x031C	CBR00_START	0x0000_0000	Color bar generator00 transmission start register (for debug)
	0x0320 – 0x03FF	Reserved	-	-
	0x0400	CBR10_HTIM1	0x0020_0004	Color bar generator10 horizontal timing control (for debug)
	0x0404	CBR10_HTIM2	0x0020_1000	Color bar generator10 horizontal timing control (for debug)

Group	Address	Register	Initial	Description
	0x0408	CBR10_VTIM1	0x0004_0004	Color bar generator10 vertical timing control (for debug)
	0x040C	CBR10_VTIM2	0x0004_0800	Color bar generator10 vertical timing control (for debug)
	0x0410	CBR10_MODE	0x0000_0000	Color bar generator10 image data select (for debug)
	0x0414	CBR10_COLOR	0x0000_0000	Color bar generator10 raster color data setting (for debug)
	0x0418	CBR10_ENABLE	0x0000_0000	Color bar generator10 enable register (for debug)
	0x041C	CBR10_START	0x0000_0000	Color bar generator10 transmission start register (for debug)
	0x0420 – 0x04FF	Reserved	-	-
	0x0500	CBR11_HTIM1	0x0020_0004	Color bar generator11 horizontal timing control (for debug)
	0x0504	CBR11_HTIM2	0x0020_1000	Color bar generator11 horizontal timing control (for debug)
	0x0508	CBR11_VTIM1	0x0004_0004	Color bar generator11 vertical timing control (for debug)
Common registers	0x050C	CBR11_VTIM2	0x0004_0800	Color bar generator11 vertical timing control (for debug)
	0x0510	CBR11_MODE	0x0000_0000	Color bar generator11 image data select (for debug)
	0x0514	CBR11_COLOR	0x0000_0000	Color bar generator11 raster color data setting (for debug)
	0x0518	CBR11_ENABLE	0x0000_0000	Color bar generator11 enable register (for debug)
	0x051C	CBR11_START	0x0000_0000	Color bar generator11 transmission start register (for debug)
	0x0520 – 0x06FF	Reserved	-	-
	0x0600	CFGSoftReset	0x0000_0003	I2C test register
	0x0604 – 0x07FF	Reserved	-	-
	0x0800	IOB_CTRL1	0x0000_0000	VDDIO voltage select
	0x0804	IOB_CTRL2	0x0606_0606	GPIO pins control
	0x0808	IOB_CTRL3	0x0004_0404	Pins control for DSI_ASSR, INT, HPD
	0x080C – 0x08FB	Reserved	-	-
	0x08FC	EFUSE_STATUS	0x0000_000X	IC test register
	0x0900 – 0x097F	EFUSE_DATA_MON	0xXXXX_XXXX	IC test register
	0x0980 – 0x0FFF	Reserved	-	-
Boot registers	0x1000	BootWaitCnt	0x61A8_61A8	Boot wait time count
	0x1004	BootSet0	0x0002_0B09	Boot setting register
	0x1008	BootSet1	0x0000_0004	Boot setting register

Group	Address	Register	Initial	Description
Boot registers	0x100C	BootSet2	0x2300_0000	Boot setting register
	0x1010	BootSet3	0x0010_0002	Boot setting register
	0x1014	BootCtrl	0x0000_0006	Boot control register
	0x1018	BootStatus	0x0000_0000	Boot status register
	0x101C	BootInterrupt	0x0000_0000	Boot Interrupt clear
	0x1020 – 0x1FFF	Reserved	-	-
DSITx0 Registers	0x2000	Reserved	-	-
	0x2004	DSI0_ADDRESS_CONFIG	0x0000_0000	IC test register
	0x2008	DSI0_DSITX_CLKEN	0x0000_0000	DSITx0 clock enable
	0x200C	DSI0_DSITX_CLKSEL	0x0000_0000	DSITx0 clock select
	0x2010	DSI0_MODE_CONFIG	0x0000_0000	DSITx0 mode setting
	0x2014	DSI0_DSITX_SYSTEM_INIT	0x0000_0000	DSITx0 system initialization
	0x2018	DSI0_LANE_ENABLE	0x0000_0000	DSITx0 lane enable
	0x201C	DSI0_DSITX_START	0x0000_0000	DSITx0 transmission start register
	0x2020	DSI0_LINE_INIT_COUNT	0x0000_FFFF	DSITx0 line wait counter
	0x2024	DSI0_HSTX_TO_COUNT	0xFFFF_FFFF	DSITx0 HS time out counter
	0x2028	DSI0_FUNC_ENABLE	0x0000_0000	DSITx0 function enable
	0x202C	DSI0_LPTX_MODE	0x0000_0000	DSITx0 test register
	0x2030	DSI0_TATO_COUNT	0xFFFF_FFFF	DSITx0 TA time out counter
	0x2034	DSI0_PRESP_BTA_COUNT	0xFFFF_FFFF	DSITx0 peripheral response time out counter for BTA
	0x2038	DSI0_PRESP_LPR_COUNT	0xFFFF_FFFF	DSITx0 peripheral response time out counter for LPDT read
	0x203C	DSI0_PRESP_LPW_COUNT	0xFFFF_FFFF	DSITx0 peripheral response time out counter for LPDT write
	0x2040	DSI0_PRESP_HSR_COUNT	0xFFFF_FFFF	DSITx0 peripheral response time out counter for HS read
	0x2044	DSI0_PRESP_HSW_COUNT	0xFFFF_FFFF	DSITx0 peripheral response time out counter for HS write
	0x2048	DSI0_PR_TO_COUNT	0xFFFF_FFFF	DSITx0 peripheral reset time out counter
	0x204C	DSI0_LRX-H_TO_COUNT	0xFFFF_FFFF	DSITx0 LPRX time out counter
	0x2050	DSI0_FUNC_MODE	0x0000_0000	DSITx0 function mode register
	0x2054	DSI0_DSIRX_VC_ENABLE	0x0000_0000	DSITx0 LPRX Virtual channel enable
	0x2058	DSI0_IND_TO_COUNT	0xFFFF_FFFF	DSITx0 sync independent interface time out counter
	0x205C	Reserved	-	-
	0x2060	DSI0_INIT_INT_STAT	0x0000_0000	DSITx0 interrupt status
	0x2064	DSI0_INIT_INT_MASK	0x0000_0000	DSITx0 interrupt mask
	0x2068	DSI0_HSYNC_STOP_COUNT	0x0000_0000	DSITx0 hsync counter
	0x206C	Reserved	-	-
	0x2070	DSI0_APF_VDELAYCNT	0x0000_0008	DSITx0 transmission of complete line data delay counter
	0x2074	DSI0_APF_HDELAYCNT	0x0000_0008	IC test regster
	0x2078	DSI0_APF_VC_CONFIG	0x0000_0000	DSITx0 virtual channel configuration
	0x207C	DSI0_DSITX_MODE	0x0000_0000	DSITx0 mode register
	0x2080	Reserved	-	-

Group	Address	Register	Initial	Description
	0x2084	Reserved	-	-
	0x2088	Reserved	-	-
	0x208C	DSI0_HSYNC_WIDTH	0x0000_0001	DSITx0 hsync width
	0x2090	DSI0_HBPR	0x0000_0001	DSITx0 horizontal back porch
	0x2094	DSI0_VFHSYNCMASK	0x0000_0000	DSITx0 hsync mask
	0x2098	Reserved	-	-
	0x209C	Reserved	-	-
	0x20A0	DSI0_RX_STATE_INT_STAT	0x0000_0000	DSITx0 LPRX interrupt status
	0x20A4	DSI0_RX_STATE_INT_MASK	0x0000_0003	DSITx0 LPRX interrupt mask
	0x20A8	DSI0_RXTRIG_INT_STAT	0x0000_0000	DSITx0 Rx Trigger interrupt status
	0x20AC	DSI0_RXTRIG_INT_MASK	0x0000_000F	DSITx0 Rx Trigger interrupt mask
	0x20B0	DSI0_DSITX_INTERNAL_STAT	0x0000_0000	DSITx0 internal status
	0x20B4	DSI0_ACKERROR	0x0000_0000	DSITx0 acknowledge error
	0x20B8	DSI0_RXFIFO	0x0000_0000	DSITx0 Rx data
	0x20BC	DSI0_RX_HEADER	0x0000_0000	DSITx0 Rx data id
	0x20C0	DSI0_LPRX_THRESH_COUNT	0x0000_0000	DSITx0 LPRX threshold counter
	0x20C4	DSI0_LPRX_FIFO_LEVEL	0x0000_0000	DSITx0 Rx FIFO level
	0x20C8-0x20FF	Reserved	-	-
	0x2100	Reserved	-	-
	0x2104	DSI0_ADDRESS_CONFIG	0x0000_0000	IC test register
DSITx0 Registers	0x2108	DSI0_PRTO_INT_STAT	0x0000_0000	DSITx0 error interrupt status
	0x210C	DSI0_PRTO_INT_MASK	0x0000_0000	DSITx0 error interrupt mask
	0x2110	DSI0_APP_SIDE_ERR_INT_STAT	0x0000_0000	DSITx0 error interrupt status
	0x2114	DSI0_APP_SIDE_ERR_INT_MASK	0xFFFF_FFFF	DSITx0 error interrupt mask
	0x2118	DSI0_RX_ERR_INT_STAT	0x0000_0000	DSITx0 error interrupt status
	0x211C	DSI0_RX_ERR_INT_MASK	0xFFFF_FFFF	DSITx0 error interrupt mask
	0x2120	DSI0_LPTX_INT_STAT	0x0000_0000	DSITx0 LPTX interrupt status
	0x2124	DSI0_LPTX_INT_MASK	0x0000_0301	DSITx0 LPTX interrupt mask
	0x2128	DSI0_LPTX_REQ	0x0000_0000	DSITx0 LP transmit request
	0x212C	DSI0_LPTX_TYPE	0x0000_0000	DSITx0 LPTX control
	0x2130	DSI0_LPTX_PKT_HDR	0x0000_0000	DSITx0 LPTX packet data
	0x2134	DSI0_LPTX_PAYLOAD0	0x0000_0000	DSITx0 LPTX payload
	0x2138	DSI0_LPTX_PAYLOAD1	0x0000_0000	DSITx0 LPTX payload
	0x213C	Reserved	-	-
	0x2140	DSI0_PPI_DPHY_DLYCNTRL	0x0000_0000	DSITx0 DPHY control
	0x2144-0x214F	Reserved	-	-
	0x2150	DSI0_PPI_DPHY_MON	0x0000_0000	DSITx0 DPHY control
	0x2154	DSI0_PPI_DPHY_LPTXTIMECNT	0x0000_0000	DSITx0 DPHY control
	0x2158	DSI0_PPI_DPHY_TCLK_HEADERCNT	0x0000_0000	DSITx0 DPHY control
	0x215C	DSI0_PPI_DPHY_TCLK_TRAILCNT	0x0000_0000	DSITx0 DPHY control
	0x2160	DSI0_PPI_DPHY_THS_HEADERCNT	0x0000_0000	DSITx0 DPHY control

Group	Address	Register	Initial	Description
DSITx0 Registers	0x2164	DSI0_PPI_DPHY_TWAKEUPCNT	0x0000_0000	DSITx0 DPHY control
	0x2168	DSI0_PPI_DPHY_TCLK_POSTCNT	0x0000_0000	DSITx0 DPHY control
	0x216C	DSI0_PPI_DPHY_THSTRAILCNT	0x0000_0000	DSITx0 DPHY control
	0x2170	DSI0_PPI_DPHY_HSTXVREGCNT	0x0000_0000	DSITx0 DPHY control
	0x2174	DSI0_PPI_DPHY_HSTXVREGEN	0x0000_0000	DSITx0 DPHY control
	0x2178	DSI0_PPI_DSI_BTA_COUNT	0x0000_0000	DSITx0 DPHY control
	0x217C	Reserved	-	-
	0x2180	DSI0_PPI_PR_DPHY_LPTRM	0x1555_5555	DSITx0 DPHY test register
	0x2184	Reserved	-	-
	0x2188	Reserved	-	-
	0x218C	DSI0_PPI_PR_DPHY_HSTRM	0x0006_6666	DSITx0 DPHY test register
	0x2190	DSI0_PPI_PR_DPHY_PISO	0x0000_0000	DSITx0 DPHY control
	0x2194	Reserved	-	-
	0x2198	Reserved	-	-
	0x219C	DSI0_LANE_STATUS_HS	0x0000_0000	DSITx0 HS lane status
	0x21A0	DSI0_LANE_STATUS_LP	0x0000_008F	DSITx0 LP lane status
	0x21A4	DSI0_MIPI_PLL_CTRL	0x0000_0000	DSITx0 PLL control
	0x21A8	DSI0_MIPI_PLL_LOCKCNT	0x0000_FFFF	DSITx0 PLL lock counter
	0x21AC	DSI0_MIPI_PLL_LOCK	0x0000_0000	DSITx0 PLL Lock indication
	0x21B0	DSI0_MIPI_PLL_CONF	0x0000_2200	DSITx0 PLL parameter
	0x21B4	DSI0_MIPI_PLL_DEBUG	0x0000_0000	DSITx0 PLL test register
	0x21B8	DSI0_MIPI_PR_PLL_CTRL	0x0000_0000	DSITx0 PLL control
	0x21BC	DSI0_MIPI_PR_PLL_PARA	0x0000_0000	DSITx0 PLL parameter
	0x21C0	DSI0_MIPI_PR_PLL_FIX	0x0000_0000	DSITx0 PLL control
	0x21C4	Reserved	-	-
	0x21C8	DSI0_DSI_DEBUG1	0x0000_0000	DSITx0 test register
	0x21CC	DSI0_DSI_DEBUG2	0x0000_0000	DSITx0 test register
	0x21D0	DSI0_PPI_DEBUG1	0x0000_0000	DSITx0 test register
	0x21D4	DSI0_PPI_DEBUG2	0x0000_0000	DSITx0 test register
	0x21D8-0x21FF	Reserved	-	-
DSITx0 Command Queue Registers	0x2200	DSI0_CQ_STATUS	0x0000_0000	DSITx0 CQ status
	0x2204	DSI0_CQ_INTERRUPT	0x0000_0000	DSITx0 CQ error interrupt
	0x2208-0x23FB	Reserved	-	-
	0x22FC	DSI0_CQ_HEADER	0x0000_0000	DSITx0 CQ packet data
	0x2300-0x23FC	DSI0_CQ_PAYLOAD	0x0000_0000	DSITx0 CQ payload
DSITx0 Common Registers	0x2800	DSI0_FORCE_ENABLE	0x0000_010F	DSITx0 test register
	0x2804-0x28FF	Reserved	-	-
	0x2900	DSI0_PIC_COM_VC_A	0x0000_0000	DSITx0 Virtual Channel
	0x2904	DSI0_PIC_COM_VDELAYSTRCOUNT_A	0x0000_0384	DSITx0 test register
	0x2908	DSI0_PIC_COM_VDELAYENDCOUNT_A	0x0000_0000	DSITx0 test register
	0x290C	DSI0_PIC_COM_MAXFCNT_A	0x0000_0000	DSITx0 test register
	0x2910	DSI0_PIC_COM_INTERLACED_A	0x0000_0000	DSITx0 test register

Group	Address	Register	Initial	Description
DSITx0 Common Registers	0x2914	DSI0_PIC_COM_3D_EN_A	0x0000_0000	DSITx0 test register
	0x2918	DSI0_PIC_COM_3DCM_A	0x0000_0000	DSITx0 test register
	0x2920	DSI0_PIC_SYN_PKT_A	0x3E0B_0C00	DSITx0 packet data type
	0x2924	DSI0_PIC_SYN_LINEPKT_A	0x0000_0000	DSITx0 test register
	0x2928	DSI0_PIC_SYN_LINEPKT_A	0x0000_0000	DSITx0 test register
	0x292C	DSI0_PIC_SYN_BLANKPKTEN _A	0x0000_0000	DSITx0 test register
	0x2930	DSI0_PIC_COM_STOP_BY_FS _A	0x0000_0001	DSITx0 test register
	0x2934-0x29FF	Reserved	-	-
	0x2A00	DSI0_TXColorMode	0x0000_0003	DSITx0 color mode register
	0x2A04	DSI0_TXSTART	0x0000_0000	DSITx0 video transmission start register
	0x2A08	DSI0_TXUPDATE	0x0000_0000	DSITx0 test register
	0x2A0C	DSI0_TXFORCEUPDATE	0x0000_0000	DSITx0 test register
	0x2A10	DSI0_CQMODE	0x0004_0010	DSITx0 CQ mode
	0x2A14-0x2FFF	Reserved	-	-
DSITx1 registers	0x3000	Reserved	-	-
	0x3004	DSI1_ADDRESS_CONFIG	0x0000_0000	IC test register
	0x3008	DSI1_DSITX_CLKEN	0x0000_0000	DSITx1 clock enable
	0x300C	DSI1_DSITX_CLKSEL	0x0000_0000	DSITx1 clock select
	0x3010	DSI1_MODE_CONFIG	0x0000_0000	DSITx1 mode setting
	0x3014	DSI1_DSITX_SYSTEM_INIT	0x0000_0000	DSITx1 system initialization
	0x3018	DSI1_LANE_ENABLE	0x0000_0000	DSITx1 lane enable
	0x301C	DSI1_DSITX_START	0x0000_0000	DSITx1 transmission start register
	0x3020	DSI1_LINE_INIT_COUNT	0x0000_FFFF	DSITx1 line wait counter
	0x3024	DSI1_HSTX_TO_COUNT	0xFFFF_FFFF	DSITx1 HS time out counter
	0x3028	DSI1_FUNC_ENABLE	0x0000_0000	DSITx1 function enable
	0x302C	DSI1_LPTX_MODE	0x0000_0000	DSITx1 test register
	0x3030	DSI1_TATO_COUNT	0xFFFF_FFFF	DSITx1 TA time out counter
	0x3034	DSI1_PRESP_BTA_COUNT	0xFFFF_FFFF	DSITx1 peripheral response time out counter for BTA
	0x3038	DSI1_PRESP_LPR_COUNT	0xFFFF_FFFF	DSITx1 peripheral response time out counter for LPDT read
	0x303C	DSI1_PRESP_LPW_COUNT	0xFFFF_FFFF	DSITx1 peripheral response time out counter for LPDT write
	0x3040	DSI1_PRESP_HSR_COUNT	0xFFFF_FFFF	DSITx1 peripheral response time out counter for HS read
	0x3044	DSI1_PRESP_HSW_COUNT	0xFFFF_FFFF	DSITx1 peripheral response time out counter for HS write
	0x3048	DSI1_PR_TO_COUNT	0xFFFF_FFFF	DSITx1 peripheral reset time out counter
	0x304C	DSI1_LRX-H_TO_COUNT	0xFFFF_FFFF	DSITx1 LPRX time out counter
	0x3050	DSI1_FUNC_MODE	0x0000_0000	DSITx1 function mode register
	0x3054	DSI1_DSIRX_VC_ENABLE	0x0000_0000	DSITx1 LPRX Virtual channel enable

Group	Address	Register	Initial	Description
	0x3058	DSI1_IND_TO_COUNT	0xFFFF_FFFF	DSITx1 sync independent interface time out counter
	0x305C	Reserved	-	-
	0x3060	DSI1_INIT_INT_STAT	0x0000_0000	DSITx1 interrupt status
	0x3064	DSI1_INIT_INT_MASK	0x0000_0000	DSITx1 interrupt mask
	0x3068	DSI1_HSYNC_STOP_COUNT	0x0000_0000	DSITx1 hsync counter
	0x306C	Reserved	-	-
	0x3070	DSI1_APF_VDELAYCNT	0x0000_0008	DSITx1 transmission of complete line data delay counter
	0x3074	DSI1_APF_HDELAYCNT	0x0000_0008	IC test regster
	0x3078	DSI1_APF_VC_CONFIG	0x0000_0000	DSITx1 virtual channel configuration
	0x307C	DSI1_DSITX_MODE	0x0000_0000	DSITx1 mode register
	0x3080	Reserved	-	-
	0x3084	Reserved	-	-
	0x3088	Reserved	-	-
	0x308C	DSI1_HSYNC_WIDTH	0x0000_0001	DSITx1 hsync width
	0x3090	DSI1_HBPR	0x0000_0001	DSITx1 horizontal back porch
	0x3094	DSI1_VFHSYNCMASK	0x0000_0000	DSITx1 hsync mask
	0x3098	Reserved	-	-
	0x309C	Reserved	-	-
DSITx1 registers	0x30A0	DSI1_RX_STATE_INT_STAT	0x0000_008F	DSITx1 LPRX interrupt status
	0x30A4	DSI1_RX_STATE_INT_MASK	0x0000_0003	DSITx1 LPRX interrupt mask
	0x30A8	DSI1_RXTRIG_INT_STAT	0x0000_0000	DSITx1 Rx Trigger interrupt status
	0x30AC	DSI1_RXTRIG_INT_MASK	0x0000_000F	DSITx1 Rx Trigger interrupt mask
	0x30B0	DSI1_DSITX_INTERNAL_STAT	0x0000_0000	DSITx1 internal status
	0x30B4	DSI1_ACKERROR	0x0000_0000	DSITx1 acknowledge error
	0x30B8	DSI1_RXFIFO	0x0000_0000	DSITx1 Rx data
	0x30BC	DSI1_RX_HEADER	0x0000_0000	DSITx1 Rx data id
	0x30C0	DSI1_LPRX_THRESH_COUNT	0x0000_0000	DSITx1 LPRX threshold counter
	0x30C4	DSI1_LPRX_FIFO_LEVEL	0x0000_0000	DSITx1 Rx FIFO level
	0x30C8-0x30FF	Reserved	-	-
	0x3100	Reserved	-	-
	0x3104	DSI1_ADDRESS_CONFIG	0x0000_0000	IC test register
	0x3108	DSI1_PRTO_INT_STAT	0x0000_0000	DSITx1 error interrupt status
	0x310C	DSI1_PRTO_INT_MASK	0x0000_0000	DSITx1 error interrupt mask
	0x3110	DSI1_APP_SIDE_ERR_INT_STAT	0x0000_0000	DSITx1 error interrupt status
	0x3114	DSI1_APP_SIDE_ERR_INT_MASK	0xFFFF_FFFF	DSITx1 error interrupt mask
	0x3118	DSI1_RX_ERR_INT_STAT	0x0000_0000	DSITx1 error interrupt status
	0x311C	DSI1_RX_ERR_INT_MASK	0xFFFF_FFFF	DSITx1 error interrupt mask

Group	Address	Register	Initial	Description
DSITx1 registers	0x3120	DSI1_LPTX_INT_STAT	0x0000_0000	DSITx1 LPTX interrupt status
	0x3124	DSI1_LPTX_INT_MASK	0x0000_0301	DSITx1 LPTX interrupt mask
	0x3128	DSI1_LPTX_REQ	0x0000_0000	DSITx1 LP transmit request
	0x312C	DSI1_LPTX_TYPE	0x0000_0000	DSITx1 LPTX control
	0x3130	DSI1_LPTX_PKT_HDR	0x0000_0000	DSITx1 LPTX packet data
	0x3134	DSI1_LPTX_PAYLOAD0	0x0000_0000	DSITx1 LPTX payload
	0x3138	DSI1_LPTX_PAYLOAD1	0x0000_0000	DSITx1 LPTX payload
	0x313C	Reserved	-	-
	0x3140	DSI1_PPI_DPHY_DLYCNTRL	0x0000_0000	DSITx1 DPHY control
	0x3144-0x314F	Reserved	-	-
	0x3150	DSI1_PPI_DPHY_MON	0x0000_0000	DSITx1 DPHY control
	0x3154	DSI1_PPI_DPHY_LPTXTIMECNT	0x0000_0000	DSITx1 DPHY control
	0x3158	DSI1_PPI_DPHY_TCLK_HEADERCNT	0x0000_0000	DSITx1 DPHY control
	0x315C	DSI1_PPI_DPHY_TCLK_TRAILCNT	0x0000_0000	DSITx1 DPHY control
	0x3160	DSI1_PPI_DPHY_THS_HEADERCNT	0x0000_0000	DSITx1 DPHY control
	0x3164	DSI1_PPI_DPHY_TWAKEUPCNT	0x0000_0000	DSITx1 DPHY control
	0x3168	DSI1_PPI_DPHY_TCLK_POSTCNT	0x0000_0000	DSITx1 DPHY control
	0x316C	DSI1_PPI_DPHY_THSTRAILCNT	0x0000_0000	DSITx1 DPHY control
	0x3170	DSI1_PPI_DPHY_HSTXVREGCNT	0x0000_0000	DSITx1 DPHY control
	0x3174	DSI1_PPI_DPHY_HSTXVREGEN	0x0000_0000	DSITx1 DPHY control
	0x3178	DSI1_PPI_DSI_BTA_COUNT	0x0000_0000	DSITx1 DPHY control
	0x317C	Reserved	-	-
	0x3180	DSI1_PPI_PR_DPHY_LPTRM	0x1555_5555	DSITx1 DPHY test register
	0x3184	Reserved	-	-
	0x3188	Reserved	-	-
	0x318C	DSI1_PPI_PR_DPHY_HSTRM	0x0006_6666	DSITx1 DPHY test register
	0x3190	DSI1_PPI_PR_DPHY_PISO	0x0000_0000	DSITx1 DPHY control
	0x3194	Reserved	-	-
	0x3198	Reserved	-	-
	0x319C	DSI1_LANE_STATUS_HS	0x0000_0000	DSITx1 HS lane status
	0x31A0	DSI1_LANE_STATUS_LP	0x0000_0000	DSITx1 LP lane status
	0x31A4	DSI1_MIPI_PLL_CTRL	0x0000_0000	DSITx1 PLL control
	0x31A8	DSI1_MIPI_PLL_LOCKCNT	0x0000_FFFF	DSITx1 PLL lock counter
	0x31AC	DSI1_MIPI_PLL_LOCK	0x0000_0000	DSITx1 PLL Lock indication
	0x31B0	DSI1_MIPI_PLL_CONF	0x0000_2200	DSITx1 PLL parameter
	0x31B4	DSI1_MIPI_PLL_DEBUG	0x0000_0000	DSITx1 PLL test register
	0x31B8	DSI1_MIPI_PR_PLL_CTRL	0x0000_0000	DSITx1 PLL control
	0x31BC	DSI1_MIPI_PR_PLL_PARA	0x0000_0000	DSITx1 PLL parameter

...

TOSHIBA

Group	Address	Register	Initial	Description
DSITx1 registers	0x31C0	DSI1_MIPI_PR_PLL_FIX	0x0000_0000	DSITx1 PLL control
	0x31C4	Reserved	-	-
	0x31C8	DSI1_DSI_DEBUG1	0x0000_0000	DSITx1 test register
	0x31CC	DSI1_DSI_DEBUG2	0x0000_0000	DSITx1 test register
	0x31D0	DSI1_PPI_DEBUG1	0x0000_0000	DSITx1 test register
	0x31D4	DSI1_PPI_DEBUG2	0x0000_0000	DSITx1 test register
	0x31D8-0x31FF	Reserved	-	-
DSITx1 Command Queue registers	0x3200	DSI1_CQ_STATUS	0x0000_0000	DSITx1 CQ status
	0x3204	DSI1_CQ_INTERRUPT	0x0000_0000	DSITx1 CQ error interrupt
	0x3208-0x32FB	Reserved	-	-
	0x32FC	DSI1_CQ_HEADER	0x0000_0000	DSITx1 CQ packet data
	0x3300-0x33FC	DSI1_CQ_PAYLOAD	0x0000_0000	DSITx1 CQ payload
DSITx1 Common Registers	0x3800	DSI1_FORCE_ENABLE	0x0000_010F	DSITx1 test register
	0x3804-0x38FF	Reserved	-	-
	0x3900	DSI1_PIC_COM_VC_A	0x0000_0000	DSITx1 Virtual Channel port A.
	0x3904	DSI1_PIC_COM_VDELAYSTRCOUNT_A	0x0000_0384	DSITx1 test register
	0x3908	DSI1_PIC_COM_VDELAYENDCOUNT_A	0x0000_0000	DSITx1 test register
	0x390C	DSI1_PIC_COM_MAXFCNT_A	0x0000_0000	DSITx1 test register
	0x3910	DSI1_PIC_COM_INTERLACED_A	0x0000_0000	DSITx1 test register
	0x3914	DSI1_PIC_COM_3D_EN_A	0x0000_0000	DSITx1 test register
	0x3918	DSI1_PIC_COM_3DCM_A	0x0000_0000	DSITx1 test register
	0x391C	DSI1_PIC_SYN_HDELAYCOUNT_A	0x0000_0000	DSITx1 test register
	0x3920	DSI1_PIC_SYN_PKT_A	0x3E0B_0C00	DSITx1 packet data type
	0x3924	DSI1_PIC_SYN_LINEPKT_A	0x0000_0000	DSITx1 test register
	0x3928	DSI1_PIC_SYN_LINEPKT_A	0x0000_0000	DSITx1 test register
	0x392C	DSI1_PIC_SYN_BLANKPKTEN_A	0x0000_0000	DSITx1 test register
	0x3930	DSI1_PIC_COM_STOP_BY_FS_A	0x0000_0001	DSITx1 test register
	0x3934-0x39FF	Reserved	-	-
	0x3A00	DSI1_TXColorMode	0x0000_0003	DSITx1 color mode register
	0x3A04	DSI1_TXSTART	0x0000_0000	DSITx1 video transmission start register
	0x3A08	DSI1_TXUPDATE	0x0000_0000	DSITx1 test register
	0x3A0C	DSI1_TXFORCEUPDATE	0x0000_0000	DSITx1 test register
	0x3A10	DSI1_CQMODE	0x0004_0010	DSITx1 CQ mode
	0x3A14-0x3FFF	Reserved	-	-
DSITx Global Registers	0x4000	Reserved	-	-
	0x4004	DSI_ADDRESS_CONFIG	0x0000_0000	IC test register
	0x4008	DSI_DSITX_CLKEN	0x0000_0000	DSITx Global clock enable
	0x400C	DSI_DSITX_CLKSEL	0x0000_0000	DSITx Global clock select

Group	Address	Register	Initial	Description
DSITx Global Registers	0x4010	DSI_MODE_CONFIG	0x0000_0000	DSITx Global mode setting
	0x4014	DSI_DSITX_SYSTEM_INIT	0x0000_0000	DSITx Global system initialization
	0x4018	DSI_LANE_ENABLE	0x0000_0000	DSITx Global lane enable
	0x401C	DSI_DSITX_START	0x0000_0000	DSITx Global transmission start register
	0x4020	DSI_LINE_INIT_COUNT	0x0000_FFFF	DSITx Global line wait counter
	0x4024	DSI_HSTX_TO_COUNT	0xFFFF_FFFF	DSITx Global HS time out counter
	0x4028	DSI_FUNC_ENABLE	0x0000_0000	DSITx Global function enable
	0x402C	DSI_LPTX_MODE	0x0000_0000	DSITx test register
	0x4030	DSI_TATO_COUNT	0xFFFF_FFFF	DSITx Global TA time out counter
	0x4034	DSI_PRESP_BTA_COUNT	0xFFFF_FFFF	DSITx Global peripheral response time out counter for BTA
	0x4038	DSI_PRESP_LPR_COUNT	0xFFFF_FFFF	DSITx Global peripheral response time out counter for LPDT read
	0x403C	DSI_PRESP_LPW_COUNT	0xFFFF_FFFF	DSITx Global peripheral response time out counter for LPDT write
	0x4040	DSI_PRESP_HSR_COUNT	0xFFFF_FFFF	DSITx Global peripheral response time out counter for HS read
	0x4044	DSI_PRESP_HSW_COUNT	0xFFFF_FFFF	DSITx Global peripheral response time out counter for HS write
	0x4048	DSI_PR_TO_COUNT	0xFFFF_FFFF	DSITx Global peripheral reset time out counter
	0x404C	DSI_LRX-H_TO_COUNT	0xFFFF_FFFF	DSITx Global LPRX time out counter
	0x4050	DSI_FUNC_MODE	0x0000_0000	DSITx Global function mode register
	0x4054	DSI_DSIRX_VC_ENABLE	0x0000_0000	DSITx Global LPRX Virtual channel enable
	0x4058	DSI_IND_TO_COUNT	0xFFFF_FFFF	DSITx Global sync independent interface time out counter
	0x405C	Reserved	-	-
	0x4060	DSI_INIT_INT_STAT	0x0000_0000	DSITx Global interrupt status
	0x4064	DSI_INIT_INT_MASK	0x0000_0000	DSITx Global interrupt mask
	0x4068	DSI_HSYNC_STOP_COUNT	0x0000_0000	DSITx Global hsync counter
	0x406C	Reserved	-	-
	0x4070	DSI_APF_VDELAYCNT	0x0000_0008	DSITx Global transmission of complete line data delay counter
	0x4074	DSI_APF_HDELAYCNT	0x0000_0008	IC test regster
	0x4078	DSI_APF_VC_CONFIG	0x0000_0000	DSITx Global virtual channel configuration
	0x407C	DSI_DSITX_MODE	0x0000_0000	DSITx Global mode register
	0x4080	Reserved	-	-

Group	Address	Register	Initial	Description
	0x4084	Reserved	-	-
	0x4088	Reserved	-	-
	0x408C	DSI_HSYNC_WIDTH	0x0000_0001	DSITx Global hsync width
	0x4090	DSI_HBPR	0x0000_0001	DSITx Global horizontal back porch
	0x4094	DSI_VFHSYNCMASK	0x0000_0000	DSITx Global hsync mask
	0x4098	Reserved	-	-
	0x409C	Reserved	-	-
	0x40A0	DSI_RX_STATE_INT_STAT	0x0000_0000	DSITx Global LPRX interrupt status
	0x40A4	DSI_RX_STATE_INT_MASK	0x0000_0003	DSITx Global LPRX interrupt mask
	0x40A8	DSI_RXTRIG_INT_STAT	0x0000_0000	DSITx Global Rx Trigger interrupt status
	0x40AC	DSI_RXTRIG_INT_MASK	0x0000_000F	DSITx Global Rx Trigger interrupt mask
	0x40B0	DSI_DSITX_INTERNAL_STAT	0x0000_0000	DSITx Global internal status
	0x40B4	DSI_ACKERROR	0x0000_0000	DSITx Global acknowledge error
	0x40B8	DSI_RXFIFO	0x0000_0000	DSITx Global Rx data
	0x40BC	DSI_RX_HEADER	0x0000_0000	DSITx Global Rx data id
	0x40C0	DSI_LPRX_THRESH_COUNT	0x0000_0000	DSITx Global LPRX threshold counter
	0x40C4	DSI_LPRX_FIFO_LEVEL	0x0000_0000	DSITx Global Rx FIFO level
DSITx Global Registers	0x40C8-0x40FF	Reserved	-	-
	0x4100	Reserved	-	-
	0x4104	DSI_ADDRESS_CONFIG	0x0000_0000	IC test register
	0x4108	DSI_PRTO_INT_STAT	0x0000_0000	DSITx Global error interrupt status
	0x410C	DSI_PRTO_INT_MASK	0x0000_0000	DSITx Global error interrupt mask
	0x4110	DSI_APP_SIDE_ERR_INT_STAT	0x0000_0000	DSITx Global error interrupt status
	0x4114	DSI_APP_SIDE_ERR_INT_MASK	0xFFFF_FFFF	DSITx Global error interrupt mask
	0x4118	DSI_RX_ERR_INT_STAT	0x0000_0000	DSITx Global error interrupt status
	0x411C	DSI_RX_ERR_INT_MASK	0xFFFF_FFFF	DSITx Global error interrupt mask
	0x4120	DSI_LPTX_INT_STAT	0x0000_0000	DSITx Global LPTX interrupt status
	0x4124	DSI_LPTX_INT_MASK	0x0000_0301	DSITx Global LPTX interrupt mask
	0x4128	DSI_LPTX_REQ	0x0000_0000	DSITx Global LP transmit request
	0x412C	DSI_LPTX_TYPE	0x0000_0000	DSITx Global LPTX control
	0x4130	DSI_LPTX_PKT_HDR	0x0000_0000	DSITx Global LPTX packet data
	0x4134	DSI_LPTX_PAYLOAD0	0x0000_0000	DSITx Global LPTX payload
	0x4138	DSI_LPTX_PAYLOAD1	0x0000_0000	DSITx Global LPTX payload
	0x413C	Reserved	-	-

Group	Address	Register	Initial	Description
DSITx Global Registers	0x4140	DSI_PPI_DPHY_DLYCNTRL	0x0000_0000	DSITx Global DPHY control
	0x4144-0x414F	Reserved	-	-
	0x4150	DSI_PPI_DPHY_MON	0x0000_0000	DSITx Global DPHY control
	0x4154	DSI_PPI_DPHY_LPTXTIMECNT	0x0000_0000	DSITx Global DPHY control
	0x4158	DSI_PPI_DPHY_TCLK_HEADERCNT	0x0000_0000	DSITx Global DPHY control
	0x415C	DSI_PPI_DPHY_TCLK_TRAILCNT	0x0000_0000	DSITx Global DPHY control
	0x4160	DSI_PPI_DPHY_THS_HEADERCNT	0x0000_0000	DSITx Global DPHY control
	0x4164	DSI_PPI_DPHY_TWAKEUPCNT	0x0000_0000	DSITx Global DPHY control
	0x4168	DSI_PPI_DPHY_TCLK_POSTCNT	0x0000_0000	DSITx Global DPHY control
	0x416C	DSI_PPI_DPHY_THSTRAILCNT	0x0000_0000	DSITx Global DPHY control
	0x4170	DSI_PPI_DPHY_HSTXVREGCNT	0x0000_0000	DSITx Global DPHY control
	0x4174	DSI_PPI_DPHY_HSTXVREGEN	0x0000_0000	DSITx Global DPHY control
	0x4178	DSI_PPI_DSI_BTA_COUNT	0x0000_0000	DSITx Global DPHY control
	0x417C	Reserved	-	-
	0x4180	DSI_PPI_PR_DPHY_LPTRM	0x1555_5555	DSITx Global DPHY test register
	0x4184	Reserved	-	-
	0x4188	Reserved	-	-
	0x418C	DSI_PPI_PR_DPHY_HSTRM	0x0006_6666	DSITx Global DPHY test register
	0x4190	DSI_PPI_PR_DPHY_PISO	0x0000_0000	DSITx Global DPHY control
	0x4194	Reserved	-	-
	0x4198	Reserved	-	-
	0x419C	DSI_LANE_STATUS_HS	0x0000_0000	DSITx Global HS lane status
	0x41A0	DSI_LANE_STATUS_LP	0x0000_008F	DSITx Global LP lane status
	0x41A4	DSI_MIPI_PLL_CTRL	0x0000_0000	DSITx Global PLL control
	0x41A8	DSI_MIPI_PLL_LOCKCNT	0x0000_FFFF	DSITx Global PLL lock counter
	0x41AC	DSI_MIPI_PLL_LOCK	0x0000_0000	DSITx Global PLL Lock indication
	0x41B0	DSI_MIPI_PLL_CONF	0x0000_2200	DSITx Global PLL parameter
	0x41B4	DSI_MIPI_PLL_DEBUG	0x0000_0000	DSITx Global PLL test register
	0x41B8	DSI_MIPI_PR_PLL_CTRL	0x0000_0000	DSITx Global PLL control
	0x41BC	DSI_MIPI_PR_PLL_PARA	0x0000_0000	DSITx Global PLL parameter
	0x41C0	DSI_MIPI_PR_PLL_FIX	0x0000_0000	DSITx Global PLL control
	0x41C4	Reserved	-	-
	0x41C8	DSI_DSI_DEBUG1	0x0000_0000	DSITx Global test register
	0x41CC	DSI_DSI_DEBUG2	0x0000_0000	DSITx Global test register
	0x41D0	DSI_PPI_DEBUG1	0x0000_0000	DSITx Global test register
	0x41D4	DSI_PPI_DEBUG2	0x0000_0000	DSITx Global test register

Group	Address	Register	Initial	Description
DSITx Global Registers	0x41D8-0x41FF	Reserved	-	-
DSITx Global Command Queue registers	0x4200	DSI_CQ_STATUS	0x0000_0000	DSITx Global CQ status
	0x4204	DSI_CQ_INTERRUPT	0x0000_0000	DSITx Global CQ error interrupt
	0x4208-0x42FB	Reserved	-	-
	0x42FC	DSI_CQ_HEADER	0x0000_0000	DSITx Global CQ packet data
	0x4300-0x43FC	DSI_CQ_PAYLOAD	0x0000_0000	DSITx Global CQ payload
eDPRx port Common registers	0x7000	IPDPRX_MODE	0x0000_1F01	eDPRx test register
	0x7004	IPDPRX_FUSE_IN0	0x0000_0000	eDPRx test register
	0x7008	IPDPRX_FUSE_IN1	0x0000_0000	eDPRx test register
	0x700C	IPDPRX_FUSE_IN_OVERRIDE	0x0000_0000	eDPRx test register
	0x7010-0x7FFF	Reserved	-	-
eDPRx DPCD registers (Receiver Capability Field)	0x8000	DPCD_REV	0x13	eDPRx DPCD Register
	0x8001	MAX_LINK_RATE	0x00	eDPRx DPCD Register
	0x8002	MAX_LANE_COUNT	0xC4	eDPRx DPCD Register
	0x8003	MAX_DOWNSPREAD	0x41	eDPRx DPCD Register
	0x8004	NORP & DP_PWR_VOLTAGE_CAP	0x00	eDPRx DPCD Register
	0x8005	DOWNSTREAMPORT_PRESENT	0x07	eDPRx DPCD Register
	0x8006	MAIN_LINK_CHANNEL_CODING	0x01	eDPRx DPCD Register
	0x8007	DOWN_STREAM_PORT_COUNT	0x01	eDPRx DPCD Register
	0x8008	RECEIVE_PORT0_CAP_0	0x00	eDPRx DPCD Register
	0x8009	RECEIVE_PORT0_CAP_1	0x23	eDPRx DPCD Register
	0x800A	RECEIVE_PORT1_CAP_0	0x00	eDPRx DPCD Register
	0x800B	RECEIVE_PORT1_CAP_1	0x00	eDPRx DPCD Register
	0x800C	I2C_speed_control_capabilities_bit_map	0x00	eDPRx DPCD Register
	0x800D	eDP_CONFIGURATION_CAP	0x01	eDPRx DPCD Register
	0x800E	TRAINING_AUX_RD_INTERVAL	0x01	eDPRx DPCD Register
	0x800F	ADAPTER_CAP	0x00	eDPRx DPCD Register
	0x8010	SUPPORTED_LINK_RATES0	0xA4	eDPRx DPCD Register
	0x8011	SUPPORTED_LINK_RATES1	0x1F	eDPRx DPCD Register
	0x8012	SUPPORTED_LINK_RATES2	0x30	eDPRx DPCD Register
	0x8013	SUPPORTED_LINK_RATES3	0x2A	eDPRx DPCD Register
	0x8014	SUPPORTED_LINK_RATES4	0x76	eDPRx DPCD Register
	0x8015	SUPPORTED_LINK_RATES5	0x2F	eDPRx DPCD Register
	0x8016	SUPPORTED_LINK_RATES6	0xBC	eDPRx DPCD Register
	0x8017	SUPPORTED_LINK_RATES7	0x34	eDPRx DPCD Register
	0x8018	SUPPORTED_LINK_RATES8	0x48	eDPRx DPCD Register
	0x8019	SUPPORTED_LINK_RATES9	0x3F	eDPRx DPCD Register
	0x801A	SUPPORTED_LINK_RATES10	0x60	eDPRx DPCD Register
	0x801B	SUPPORTED_LINK_RATES11	0x54	eDPRx DPCD Register
	0x801C	SUPPORTED_LINK_RATES12	0xEC	eDPRx DPCD Register
	0x801D	SUPPORTED_LINK_RATES13	0x5E	eDPRx DPCD Register
	0x801E	SUPPORTED_LINK_RATES14	0x78	eDPRx DPCD Register
	0x801F	SUPPORTED_LINK_RATES15	0x69	eDPRx DPCD Register

Group	Address	Register	Initial	Description
eDPRx DPCD registers (Receiver Capability Field)	0x8020	FAUX_CAP	0x00	eDPRx DPCD Register
	0x8021	MSTM_CAP	0x00	eDPRx DPCD Register
	0x8022	NUMBER_OF_AUDIO_ENDPOINTS	0x00	eDPRx DPCD Register
	0x8023	AV_GRANULARITY	0x11	eDPRx DPCD Register
	0x8024	AUD_DEC_LAT_7_0	0x00	eDPRx DPCD Register
	0x8025	AUD_DEC_LAT_15_8	0x00	eDPRx DPCD Register
	0x8026	AUD_PP_LAT_7_0	0x00	eDPRx DPCD Register
	0x8027	AUD_PP_LAT_15_8	0x00	eDPRx DPCD Register
	0x8028	VID_INTER_LAT_7_0	0x01	eDPRx DPCD Register
	0x8029	VID_PROG_LAT_7_0	0x01	eDPRx DPCD Register
	0x802A	REP_LAT_7_0	0x0A	eDPRx DPCD Register
	0x802B	AUD_DEL_INS_7_0	0x00	eDPRx DPCD Register
	0x802C	AUD_DEL_INS_15_8	0x00	eDPRx DPCD Register
	0x802D	AUD_DEL_INS_23_16	0x00	eDPRx DPCD Register
	0x802E	RECEIVER ADVANCED LINK POWER MANAGEMENT CAPABILITIES	0x01	eDPRx DPCD Register
	0x802F	SINK DEVICE AUX_FRAME_SYNC CAPABILITY	0x00	eDPRx DPCD Register
	0x8030	GUID0	0x00	eDPRx DPCD Register
	0x8031	GUID1	0x00	eDPRx DPCD Register
	0x8032	GUID2	0x00	eDPRx DPCD Register
	0x8033	GUID3	0x00	eDPRx DPCD Register
	0x8034	GUID4	0x00	eDPRx DPCD Register
	0x8035	GUID5	0x00	eDPRx DPCD Register
	0x8036	GUID6	0x00	eDPRx DPCD Register
	0x8037	GUID7	0x00	eDPRx DPCD Register
	0x8038	GUID8	0x00	eDPRx DPCD Register
	0x8039	GUID9	0x00	eDPRx DPCD Register
	0x803A	GUID10	0x00	eDPRx DPCD Register
	0x803B	GUID11	0x00	eDPRx DPCD Register
	0x803C	GUID12	0x00	eDPRx DPCD Register
	0x803D	GUID13	0x00	eDPRx DPCD Register
	0x803E	GUID14	0x00	eDPRx DPCD Register
	0x803F	GUID15	0x00	eDPRx DPCD Register
	0x8040-0x8053	Reserved	-	-
	0x8054	RX_GTC_VALUE7_0	0x00	eDPRx DPCD Register
	0x8055	RX_GTC_VALUE15_8	0x00	eDPRx DPCD Register
	0x8056	RX_GTC_VALUE23_16	0x00	eDPRx DPCD Register
	0x8057	RX_GTC_VALUE31_24	0x00	eDPRx DPCD Register
	0x8058	RX_GTC_MSTR_REQ	0x00	eDPRx DPCD Register
	0x8059	RX_GTC_FREQ_LOCK_DONE	0x00	eDPRx DPCD Register
	0x805A	RX_GTC_PHASE_SKEW_OFFSET7_0	0x00	eDPRx DPCD Register
	0x805B	RX_GTC_PHASE_SKEW_OFFSET15_8	0x00	eDPRx DPCD Register
	0x805C-0x805F	Reserved	-	-
	0x8060	eDP COMPRESSION ALGORIGHM REVISION	0x00	eDPRx DPCD Register
	0x8061	RECEIVER DECOMPRESSION CAPABILITIES	0x00	eDPRx DPCD Register

2015-10-05

Group	Address	Register	Initial	Description
eDPRx DPCD registers (Receiver Capability Field)	0x8062	DECOMPRESSOR BUFFER SIZE	0x00	eDPRx DPCD Register
	0x8063-0x806F	Reserved	-	-
	0x8070	PANEL_SELF_REFRESH_CAPABILITY_SUPPORTED_AND_VERSION	0x00	eDPRx DPCD Register
	0x8071	PANEL_SELF_REFRESH_CAPBILITIES	0x00	eDPRx DPCD Register
	0x8072-0x807F	Reserved	-	-
	0x8080	DWN_STRM_PORT0_CAP_Byte0	0x04	eDPRx DPCD Register
	0x8081	Byte_1_for_DWN_STRM_PORT0	0x00	eDPRx DPCD Register
	0x8082	Byte_2_for_DWN_STRM_PORT0	0x00	eDPRx DPCD Register
	0x8083	Byte_3_for_DWN_STRM_PORT0	0x00	eDPRx DPCD Register
	0x8084	DWN_STRM_PORT1_CAP_Byte0	0x04	eDPRx DPCD Register
	0x8085	Byte_1_for_DWN_STRM_PORT1	0x00	eDPRx DPCD Register
	0x8086	Byte_2_for_DWN_STRM_PORT1	0x00	eDPRx DPCD Register
	0x8087	Byte_3_for_DWN_STRM_PORT1	0x00	eDPRx DPCD Register
	0x8088	DWN_STRM_PORT2_CAP_Byte0	0x04	eDPRx DPCD Register
	0x8089	Byte_1_for_DWN_STRM_PORT2	0x00	eDPRx DPCD Register
	0x808A	Byte_2_for_DWN_STRM_PORT2	0x00	eDPRx DPCD Register
	0x808B	Byte_3_for_DWN_STRM_PORT2	0x00	eDPRx DPCD Register
	0x808C	DWN_STRM_PORT3_CAP_Byte0	0x04	eDPRx DPCD Register
	0x808D	Byte_1_for_DWN_STRM_PORT3	0x00	eDPRx DPCD Register
	0x808E	Byte_2_for_DWN_STRM_PORT3	0x00	eDPRx DPCD Register
	0x808F	Byte_3_for_DWN_STRM_PORT3	0x00	eDPRx DPCD Register
	0x8090-0x80FF	Reserved	-	-
eDPRx DPCD registers (Link Configuration Field)	0x8100	LINK_BW_SET	0x06	eDPRx DPCD Register
	0x8101	LANE_COUNT_SET	0x01	eDPRx DPCD Register
	0x8102	TRAINING_PATTERN_SET	0x00	eDPRx DPCD Register
	0x8103	TRAINING_LANE0_SET	0x00	eDPRx DPCD Register
	0x8104	TRAINING_LANE1_SET	0x00	eDPRx DPCD Register
	0x8105	TRAINING_LANE2_SET	0x00	eDPRx DPCD Register
	0x8106	TRAINING_LANE3_SET	0x00	eDPRx DPCD Register
	0x8107	DOWNSPREAD_CTRL	0x00	eDPRx DPCD Register
	0x8108	MAIN_LINK_CHANNEL_CODING_SET	0x01	eDPRx DPCD Register

Group	Address	Register	Initial	Description
	0x8109	I2C_speed_control_status_bit_map	0x00	eDPRx DPCD Register
	0x810A	eDP_CONFIGURATION_SET	0x00	eDPRx DPCD Register
	0x810B	LINK_QUAL_LANE0_SET	0x00	eDPRx DPCD Register
	0x810C	LINK_QUAL_LANE1_SET	0x00	eDPRx DPCD Register
	0x810D	LINK_QUAL_LANE2_SET	0x00	eDPRx DPCD Register
	0x810E	LINK_QUAL_LANE3_SET	0x00	eDPRx DPCD Register
	0x810F	TRAINING_LANE0_1_SET2	0x00	eDPRx DPCD Register
	0x8110	TRAINING_LANE2_3_SET2	0x00	eDPRx DPCD Register
	0x8111	MSTM_CTRL	0x00	eDPRx DPCD Register
	0x8112	AUDIO_DELAY_7_0	0x00	eDPRx DPCD Register
	0x8113	AUDIO_DELAY_15_8	0x00	eDPRx DPCD Register
	0x8114	AUDIO_DELAY_23_16	0x00	eDPRx DPCD Register
	0x8115	LINK_RATE_SET	0x00	eDPRx DPCD Register
	0x8116	RECIVER ADVANCED LINK POWR MANAGEMENT CONFGURATION	0x00	eDPRx DPCD Register
	0x8117	SINK DEVICE AUX_FRAME_SYNC CONFIGURATION	0x00	eDPRx DPCD Register
	0x8118	UPSTREAM_DEVICE_DP_PWR_NEED	0x00	eDPRx DPCD Register
	0x8119-0x811F	Reserved	-	-
eDPRx DPCD registers (Link Configuration Field)	0x8120	FAUX_MODE_CTRL	0x00	eDPRx DPCD Register
	0x8121	FAUX_ FORWARD_CHANNEL_DRIVE _SET	0x00	eDPRx DPCD Register
	0x8122	FAUX_BACK_CHANNEL_STATUS	0x00	eDPRx DPCD Register
	0x8123	FAUX_ BACK_CHANNEL_SYMBOL_ERROR_COUNT0	0x00	eDPRx DPCD Register
	0x8124	FAUX_ BACK_CHANNEL_SYMBOL_ERROR_COUNT1	0x00	eDPRx DPCD Register
	0x8125	FAUX_BACK_CHANNEL_TRAINING_PATTERN_TIME	0x00	eDPRx DPCD Register
	0x8126-0x8153	Reserved	-	-
	0x8154	TX_GTC_VALUE7:0	0x00	eDPRx DPCD Register
	0x8155	TX_GTC_VALUE15:8	0x00	eDPRx DPCD Register
	0x8156	TX_GTC_VALUE23:16	0x00	eDPRx DPCD Register
	0x8157	TX_GTC_VALUE31:24	0x00	eDPRx DPCD Register
	0x8158	RX_GTC_VALUE_PHASE_SKEW_E	0x00	eDPRx DPCD Register
	0x8159	TX_GTC_FREQ_LOCK_DONE	0x00	eDPRx DPCD Register
	0x815A-0x815B	Reserved	-	-
	0x815C	AUX_FRAME_SYNC_VALUE	0x00	eDPRx DPCD Register
	0x815D		0x00	eDPRx DPCD Register
	0x815E		0x00	eDPRx DPCD Register
	0x815F		0x00	eDPRx DPCD Register
	0x8160	RECEIVER DECOMPRESSION CONFIGURATION	0x00	eDPRx DPCD Register

Group	Address	Register	Initial	Description
eDPRx DPCD registers (Link Configuration Field)	0x8161-0x816F	Reserved	-	-
	0x8170	PANEL_SELF_REFRESH_CONFIGURAION	0x00	eDPRx DPCD Register
	0x8171-0x819F	Reserved	-	-
	0x81A0	ADAPTER_CTRL	0x00	eDPRx DPCD Register
	0x81A1	BRANCH_DEVICE_CTRL	0x00	eDPRx DPCD Register
	0x81A2-0x81BF	Reserved	-	-
	0x81C0	PAYLOAD_ALLOCATE_SET	0x00	eDPRx DPCD Register
	0x81C1	PAYLOAD_ALLOCATE_START_TIME_SLOT	0x00	eDPRx DPCD Register
	0x81C2	PAYLOAD_ALLOCATE_TIME_SLOT_COUNT	0x00	eDPRx DPCD Register
	0x81C3-0x81FF	Reserved	-	-
eDPRX DPCD registers (Link/Sink Status Field)	0x8200	SINK_COUNT	0x00	eDPRx DPCD Register
	0x8201	DEVICE_SERVICE_IRQ_VECTOR	0x00	eDPRx DPCD Register
	0x8202	LANE0_1_STATUS	0x00	eDPRx DPCD Register
	0x8203	LANE2_3_STATUS	0x00	eDPRx DPCD Register
	0x8204	LANE_ALIGN__STATUS_UPDATED	0x00	eDPRx DPCD Register
	0x8205	SINK_STATUS	0x00	eDPRx DPCD Register
	0x8206	ADJUST_REQUEST_LANE0_1	0x00	eDPRx DPCD Register
	0x8207	ADJUST_REQUEST_LANE2_3	0x00	eDPRx DPCD Register
	0x8208	TRAINING_SCORE_LANE0	0x00	eDPRx DPCD Register
	0x8209	TRAINING_SCORE_LANE1	0x00	eDPRx DPCD Register
	0x820A	TRAINING_SCORE_LANE2	0x00	eDPRx DPCD Register
	0x820B	TRAINING_SCORE_LANE3	0x00	eDPRx DPCD Register
	0x820C	ADJUST_REQUEST_POST_CURSOR2	0x00	eDPRx DPCD Register
	0x820D	FAUX_FORWARD_CHANNEL_SYMBOL_ERROR_COUNT0	0x00	eDPRx DPCD Register
	0x820E	FAUX_FORWARD_CHANNEL_SYMBOL_ERROR_COUNT1	0x00	eDPRx DPCD Register
	0x820F	DECOMPRESSION_STATUS_REGISTER	0x00	eDPRx DPCD Register
	0x8210	SYMBOL_ERROR_COUNT_LANE0_0	0x00	eDPRx DPCD Register
	0x8211	SYMBOL_ERROR_COUNT_LANE0_1	0x00	eDPRx DPCD Register
	0x8212	SYMBOL_ERROR_COUNT_LANE1_0	0x00	eDPRx DPCD Register
	0x8213	SYMBOL_ERROR_COUNT_LANE1_1	0x00	eDPRx DPCD Register
	0x8214	SYMBOL_ERROR_COUNT_LANE2_0	0x00	eDPRx DPCD Register
	0x8215	SYMBOL_ERROR_COUNT_LANE2_1	0x00	eDPRx DPCD Register
	0x8216	SYMBOL_ERROR_COUNT_LANE3_0	0x00	eDPRx DPCD Register
	0x8217	SYMBOL_ERROR_COUNT_LANE3_1	0x00	eDPRx DPCD Register

Group	Address	Register	Initial	Description
	0x8218-0x827F	Reserved	-	-
	0x8280	FAUX_FORWARD_CHANNEL_STATUS	0x00	eDPRx DPCD Register
	0x8281	FAUX_BACK_CHANNEL_DRIVE_SET	0x00	eDPRx DPCD Register
	0x8282	FAUX_BACK_CHANNEL_SYMBOL_ERROR_COUNT_CONTROL	0x00	eDPRx DPCD Register
	0x8283-0x82BF	Reserved	-	-
	0x82C0	PAYLOAD_TABLE_UPDATE_STATUS	0x00	eDPRx DPCD Register
	0x82C1	VC_PAYLOAD_ID_SLOT_1	0x00	eDPRx DPCD Register
	0x82C2	VC_PAYLOAD_ID_SLOT_2	0x00	eDPRx DPCD Register
	0x82C3	VC_PAYLOAD_ID_SLOT_3	0x00	eDPRx DPCD Register
	0x82C4	VC_PAYLOAD_ID_SLOT_4	0x00	eDPRx DPCD Register
	0x82C5	VC_PAYLOAD_ID_SLOT_5	0x00	eDPRx DPCD Register
	0x82C6	VC_PAYLOAD_ID_SLOT_6	0x00	eDPRx DPCD Register
	0x82C7	VC_PAYLOAD_ID_SLOT_7	0x00	eDPRx DPCD Register
	0x82C8	VC_PAYLOAD_ID_SLOT_8	0x00	eDPRx DPCD Register
	0x82C9	VC_PAYLOAD_ID_SLOT_9	0x00	eDPRx DPCD Register
	0x82CA	VC_PAYLOAD_ID_SLOT_10	0x00	eDPRx DPCD Register
	0x82CB	VC_PAYLOAD_ID_SLOT_11	0x00	eDPRx DPCD Register
	0x82CC	VC_PAYLOAD_ID_SLOT_12	0x00	eDPRx DPCD Register
eDPRX DPCD registers (Automated Testing Sub-Field)	0x82CD	VC_PAYLOAD_ID_SLOT_13	0x00	eDPRx DPCD Register
	0x82CE	VC_PAYLOAD_ID_SLOT_14	0x00	eDPRx DPCD Register
	0x82CF	VC_PAYLOAD_ID_SLOT_15	0x00	eDPRx DPCD Register
	0x82D0	VC_PAYLOAD_ID_SLOT_16	0x00	eDPRx DPCD Register
	0x82D1	VC_PAYLOAD_ID_SLOT_17	0x00	eDPRx DPCD Register
	0x82D2	VC_PAYLOAD_ID_SLOT_18	0x00	eDPRx DPCD Register
	0x82D3	VC_PAYLOAD_ID_SLOT_19	0x00	eDPRx DPCD Register
	0x82D4	VC_PAYLOAD_ID_SLOT_20	0x00	eDPRx DPCD Register
	0x82D5	VC_PAYLOAD_ID_SLOT_21	0x00	eDPRx DPCD Register
	0x82D6	VC_PAYLOAD_ID_SLOT_22	0x00	eDPRx DPCD Register
	0x82D7	VC_PAYLOAD_ID_SLOT_23	0x00	eDPRx DPCD Register
	0x82D8	VC_PAYLOAD_ID_SLOT_24	0x00	eDPRx DPCD Register
	0x82D9	VC_PAYLOAD_ID_SLOT_25	0x00	eDPRx DPCD Register
	0x82DA	VC_PAYLOAD_ID_SLOT_26	0x00	eDPRx DPCD Register
	0x82DB	VC_PAYLOAD_ID_SLOT_27	0x00	eDPRx DPCD Register
	0x82DC	VC_PAYLOAD_ID_SLOT_28	0x00	eDPRx DPCD Register
	0x82DD	VC_PAYLOAD_ID_SLOT_29	0x00	eDPRx DPCD Register
	0x82DE	VC_PAYLOAD_ID_SLOT_30	0x00	eDPRx DPCD Register
	0x82DF	VC_PAYLOAD_ID_SLOT_31	0x00	eDPRx DPCD Register
	0x82E0	VC_PAYLOAD_ID_SLOT_32	0x00	eDPRx DPCD Register
	0x82E1	VC_PAYLOAD_ID_SLOT_33	0x00	eDPRx DPCD Register
	0x82E2	VC_PAYLOAD_ID_SLOT_34	0x00	eDPRx DPCD Register
	0x82E3	VC_PAYLOAD_ID_SLOT_35	0x00	eDPRx DPCD Register
	0x82E4	VC_PAYLOAD_ID_SLOT_36	0x00	eDPRx DPCD Register
	0x82E5	VC_PAYLOAD_ID_SLOT_37	0x00	eDPRx DPCD Register
	0x82E6	VC_PAYLOAD_ID_SLOT_38	0x00	eDPRx DPCD Register
	0x82E7	VC_PAYLOAD_ID_SLOT_39	0x00	eDPRx DPCD Register
	0x82E8	VC_PAYLOAD_ID_SLOT_40	0x00	eDPRx DPCD Register
	0x82E9	VC_PAYLOAD_ID_SLOT_41	0x00	eDPRx DPCD Register
	0x82EA	VC_PAYLOAD_ID_SLOT_42	0x00	eDPRx DPCD Register

Group	Address	Register	Initial	Description
eDPRX DPCD registers (Automated Testing Sub-Field)	0x82EB	VC_PAYLOAD_ID_SLOT_43	0x00	eDPRx DPCD Register
	0x82EC	VC_PAYLOAD_ID_SLOT_44	0x00	eDPRx DPCD Register
	0x82ED	VC_PAYLOAD_ID_SLOT_45	0x00	eDPRx DPCD Register
	0x82EE	VC_PAYLOAD_ID_SLOT_46	0x00	eDPRx DPCD Register
	0x82EF	VC_PAYLOAD_ID_SLOT_47	0x00	eDPRx DPCD Register
	0x82F0	VC_PAYLOAD_ID_SLOT_48	0x00	eDPRx DPCD Register
	0x82F1	VC_PAYLOAD_ID_SLOT_49	0x00	eDPRx DPCD Register
	0x82F2	VC_PAYLOAD_ID_SLOT_50	0x00	eDPRx DPCD Register
	0x82F3	VC_PAYLOAD_ID_SLOT_51	0x00	eDPRx DPCD Register
	0x82F4	VC_PAYLOAD_ID_SLOT_52	0x00	eDPRx DPCD Register
	0x82F5	VC_PAYLOAD_ID_SLOT_53	0x00	eDPRx DPCD Register
	0x82F6	VC_PAYLOAD_ID_SLOT_54	0x00	eDPRx DPCD Register
	0x82F7	VC_PAYLOAD_ID_SLOT_55	0x00	eDPRx DPCD Register
	0x82F8	VC_PAYLOAD_ID_SLOT_56	0x00	eDPRx DPCD Register
	0x82F9	VC_PAYLOAD_ID_SLOT_57	0x00	eDPRx DPCD Register
	0x82FA	VC_PAYLOAD_ID_SLOT_58	0x00	eDPRx DPCD Register
	0x82FB	VC_PAYLOAD_ID_SLOT_59	0x00	eDPRx DPCD Register
	0x82FC	VC_PAYLOAD_ID_SLOT_60	0x00	eDPRx DPCD Register
	0x82FD	VC_PAYLOAD_ID_SLOT_61	0x00	eDPRx DPCD Register
	0x82FE	VC_PAYLOAD_ID_SLOT_62	0x00	eDPRx DPCD Register
	0x82FF	VC_PAYLOAD_ID_SLOT_63	0x00	eDPRx DPCD Register
eDPRx DPCD registers (Source Device-Specific Field)	0x8300	IEEE_OUI_first_two_hex_digits _Source	0x00	eDPRx DPCD Register
	0x8301	IEEE_OUI_second_two_hex_digits_Source	0x00	eDPRx DPCD Register
	0x8302	IEEE_OUI_third_two_hex_digits _Source	0x00	eDPRx DPCD Register
	0x8303	Device_Identification_String_Source0	0x00	eDPRx DPCD Register
	0x8304	Device_Identification_String_Source1	0x00	eDPRx DPCD Register
	0x8305	Device_Identification_String_Source2	0x00	eDPRx DPCD Register
	0x8306	Device_Identification_String_Source3	0x00	eDPRx DPCD Register
	0x8307	Device_Identification_String_Source4	0x00	eDPRx DPCD Register
	0x8308	Device_Identification_String_Source5	0x00	eDPRx DPCD Register
	0x8309	Hardware_revision_Source	0x00	eDPRx DPCD Register
	0x830A	Firmware_software_major_revision_Source	0x00	eDPRx DPCD Register
	0x830B	Firmware_software_minor_revision_Source	0x00	eDPRx DPCD Register
	0x830C-0x83FF	Reserved	-	-
eDPRx DPCD registers (Sink Device-Specific Field)	0x8400	IEEE_OUI_first_two_hex_digits _Source	0x00	eDPRx DPCD Register
	0x8401	IEEE_OUI_second_two_hex_digits_Source	0x00	eDPRx DPCD Register
	0x8402	IEEE_OUI_third_two_hex_digits _Source	0x00	eDPRx DPCD Register
	0x8403	Device_Identification_String_Source0	0x00	eDPRx DPCD Register
	0x8404	Device_Identification_String_Source1	0x00	eDPRx DPCD Register

Group	Address	Register	Initial	Description
eDPRx DPCD registers (Sink Device-Specific Field)	0x8405	Device_Identification_String_Source2	0x00	eDPRx DPCD Register
	0x8406	Device_Identification_String_Source3	0x00	eDPRx DPCD Register
	0x8407	Device_Identification_String_Source4	0x00	eDPRx DPCD Register
	0x8408	Device_Identification_String_Source5	0x00	eDPRx DPCD Register
	0x8409	Hardware_revision_Source	0x00	eDPRx DPCD Register
	0x840A	Firmware_software_major_revision_Source	0x00	eDPRx DPCD Register
	0x840B	Firmware_software_minor_revision_Source	0x00	eDPRx DPCD Register
	0x840C-0x84FF	Reserved	-	-
eDPRx DPCD registers (Branch Device-Specific Field)	0x8500	IEEE_OUI_first_two_hex_digits_Branch	0x00	eDPRx DPCD Register
	0x8501	IEEE_OUI_second_two_hex_digits_Branch	0x00	eDPRx DPCD Register
	0x8502	IEEE_OUI_third_two_hex_digits_Branch	0x00	eDPRx DPCD Register
	0x8503	Device_Identification_String_Branch0	0x00	eDPRx DPCD Register
	0x8504	Device_Identification_String_Branch1	0x00	eDPRx DPCD Register
	0x8505	Device_Identification_String_Branch2	0x00	eDPRx DPCD Register
	0x8506	Device_Identification_String_Branch3	0x00	eDPRx DPCD Register
	0x8507	Device_Identification_String_Branch4	0x00	eDPRx DPCD Register
	0x8508	Device_Identification_String_Branch5	0x00	eDPRx DPCD Register
	0x8509	Hardware_revision_Branch	0x00	eDPRx DPCD Register
	0x850A	Firmware_software_major_revision_Branch	0x00	eDPRx DPCD Register
	0x850B	Firmware_software_minor_revision_Branch	0x00	eDPRx DPCD Register
	0x850C-0x85FF	Reserved	-	-
eDPRx DPCD registers (Sink Control Field)	0x8600	SET_POWER_AND_SET_DP_PWR_VOLTAGE	0x01	eDPRx DPCD Register
	0x8601-0x86FF	Reserved	-	-
eDPRx DPCD registers (Display Control Registers)	0x8700	EDP_DPCD_REV	0x03	eDPRx DPCD Register (0x8700to 0x 87FF. when DPCD_DISPLAY_CONTROL_CAPABLE=1, these register is enabled)
	0x8701	EDP_BACKLIGHT_ADJUSTMENT_CAPABILITIES_REGISTER	0x00	eDPRx DPCD Register
	0x8702	EDP_GENERAL_CAPABILITY_REGISTER_1	0x00	eDPRx DPCD Register
	0x8703	EDP_GENERAL_CAPABILITY_REGISTER_2	0x00	eDPRx DPCD Register

Group	Address	Register	Initial	Description
eDPRx DPCD registers (Display Control Registers)	0x8704	EDP_GENERAL_CAPABILITY_REGISTER_3	0x00	eDPRx DPCD Register
	0x8705-0x871F	Reserved	-	-
	0x8720	EDP_DISPLAY_CONTROL_REGISTER	0x00	eDPRx DPCD Register
	0x8721	EDP_BACKLIGHT_MODE_SET_REGISTER	0x01	eDPRx DPCD Register
	0x8722	EDP_BACKLIGHT_BRIGHTNESS_MSB	0x00	eDPRx DPCD Register
	0x8723	EDP_BACKLIGHT_BRIGHTNESS_LSB	0x00	eDPRx DPCD Register
	0x8724	EDP_PWMGEN_BIT_COUNT	0x00	eDPRx DPCD Register
	0x8725	EDP_PWMGEN_BIT_COUNT_CAP_MIN	0x01	eDPRx DPCD Register
	0x8726	EDP_PWMGEN_BIT_COUNT_CAP_MAX	0x01	eDPRx DPCD Register
	0x8727	EDP_BACKLIGHT_CONTROL_STATUS	0x00	eDPRx DPCD Register
	0x8728	EDP_BACKLIGHT_FREQ_SET	0x00	eDPRx DPCD Register
	0x8729	Reserved	-	-
	0x872A	EDP_BACKLIGHT_FREQ_CAP_MIN_MSB	0x00	eDPRx DPCD Register
	0x872B	EDP_BACKLIGHT_FREQ_CAP_MIN_MID	0x00	eDPRx DPCD Register
	0x872C	EDP_BACKLIGHT_FREQ_CAP_MIN_LSB	0x00	eDPRx DPCD Register
	0x872D	EDP_BACKLIGHT_FREQ_CAP_MAX_MSB	0x00	eDPRx DPCD Register
	0x872E	EDP_BACKLIGHT_FREQ_CAP_MAX_MID	0x00	eDPRx DPCD Register
	0x872F	EDP_BACKLIGHT_FREQ_CAP_MAX_LSB	0x00	eDPRx DPCD Register
	0x8730-0x8731	Reserved	-	-
	0x8732	EDP_DBC_MINIMUM_BRIGHTNESS_SET	0x00	eDPRx DPCD Register
	0x8733	EDP_DBC_MAXIMUM_BRIGHTNESS_SET	0x00	eDPRx DPCD Register
	0x8734-0x873F	Reserved	-	-
	0x8740	REGIONAL_BACKLIGHT_BASE	0x00	eDPRx DPCD Register
	0x8741	REGIONAL_BACKLIGHT_BRIGHTNESS_0	0x00	eDPRx DPCD Register
	0x8742	REGIONAL_BACKLIGHT_BRIGHTNESS_1	0x00	eDPRx DPCD Register
	0x8743	REGIONAL_BACKLIGHT_BRIGHTNESS_2	0x00	eDPRx DPCD Register
	0x8744	REGIONAL_BACKLIGHT_BRIGHTNESS_3	0x00	eDPRx DPCD Register
	0x8745	REGIONAL_BACKLIGHT_BRIGHTNESS_4	0x00	eDPRx DPCD Register
	0x8746	REGIONAL_BACKLIGHT_BRIGHTNESS_5	0x00	eDPRx DPCD Register
	0x8747	REGIONAL_BACKLIGHT_BRIGHTNESS_6	0x00	eDPRx DPCD Register

Group	Address	Register	Initial	Description
eDPRx DPCD registers (Display Control Registers)	0x8748	REGIONAL_BACKLIGHT_BRIGHTNESS_7	0x00	eDPRx DPCD Register
	0x8749	REGIONAL_BACKLIGHT_BRIGHTNESS_8	0x00	eDPRx DPCD Register
	0x874A	REGIONAL_BACKLIGHT_BRIGHTNESS_9	0x00	eDPRx DPCD Register
	0x874B	REGIONAL_BACKLIGHT_BRIGHTNESS_10	0x00	eDPRx DPCD Register
	0x874C	REGIONAL_BACKLIGHT_BRIGHTNESS_11	0x00	eDPRx DPCD Register
	0x874D	REGIONAL_BACKLIGHT_BRIGHTNESS_12	0x00	eDPRx DPCD Register
	0x874E	REGIONAL_BACKLIGHT_BRIGHTNESS_13	0x00	eDPRx DPCD Register
	0x874F	REGIONAL_BACKLIGHT_BRIGHTNESS_14	0x00	eDPRx DPCD Register
	0x8750-0x87FF	Reserved	-	-
eDPRx DPCD registers (Reserved)	0x8800-0x8FFF	Reserved	-	-
eDPRx DPCD registers (Sideband MSG Buffers)	0x9000-0x9FFF	Reserved	-	-
eDPRx DPCD registers (ESI :Event Status Indicator Field)	0xA000-0xA001	Reserved	-	-
	0xA002	SINK_COUNT_ESI	0x00	eDPRx DPCD Register
	0xA003	DEVICE_SERVICE_IRQ_VECTOR_ESI0	0x00	eDPRx DPCD Register
	0xA004	DEVICE_SERVICE_IRQ_VECTOR_ESI1	0x00	eDPRx DPCD Register
	0xA005	LINK_SERVICE_IRQ_VECTOR_ESI0	0x00	eDPRx DPCD Register
eDPRx DPCD registers (PSR Status Field)	0xA006	SU_PSR_ERROR_STATUS	0x00	eDPRx DPCD Register
	0xA007	SU_PSR_EVENT_STATUS_INDICATOR	0x00	eDPRx DPCD Register
	0xA008	SINK_DEVICE_PANEL_SELF_REFRESH_STATUS	0x00	eDPRx DPCD Register
	0xA009	DEBUG_REGISTER_0	0x00	eDPRx DPCD Register
	0xA00A	DEBUG_REGISTER_1	0x00	eDPRx DPCD Register
	0xA00B	RECEIVER_ADVANCED_LINK_POWER_MANAGEMENT_STATUS	0x00	eDPRx DPCD Register
	0xA00C	SINK_DEVICE_AUX_FRAME_SYNC_STATUS	0x00	eDPRx DPCD Register
	0xA00D	DECOMPRESSION_STATUS_REGISTER	0x00	eDPRx DPCD Register
	0xA00E	LANE_ALIGN__STATUS_UPDATED_ESI	0x00	eDPRx DPCD Register
	0xA00F	SINK_STATUS_ESI	0x00	eDPRx DPCD Register
	0xA010-0xAFFF	Reserved	-	-

Group	Address	Register	Initial	Description
eDPRx Common registers	0xB000	CG_CLOCK_CTRL0	0x06	eDPRx Clock control
	0xB001	CG_CLOCK_CTRL1	0x00	eDPRx Clock control
	0xB002	CG_CLOCK_CTRL2	0x00	eDPRx test register
	0xB003	CG_DEBUG_CTRL	0x00	eDPRx test register
	0xB004	CG_VIDPLL_CTRL0	0x00	eDPRx PLL control
	0xB005	CG_VIDPLL_CTRL1	0x00	eDPRx PLL control
	0xB006	CG_VIDPLL_CTRL2	0x00	eDPRx PLL PRDIV
	0xB007	CG_VIDPLL_CTRL3	0x00	eDPRx PLL FBDIV LSB
	0xB008	CG_VIDPLL_CTRL4	0x00	eDPRx PLL FBDIV MSB
	0xB009	CG_VIDPLL_CTRL5	0x00	eDPRx PLL LBWS LFR
	0xB00A	CG_VIDPLL_CTRL6	0x00	eDPRx PLL BCP
	0xB00B	CG_VIDPLL_CTRL7	0x00	eDPRx PLL test register
	0xB00C	CG_VIDPLL_STS	0x00	eDPRx PLL test register
	0xB00D-0xB00E	Reserved	-	-
	0xB00F	MLRESETB	0x01	eDPRx main link reset register
	0xB010	HPD_CTRL	0x01	eDPRx HPD control
	0xB011	HPD_LOW	0x16	eDPRx HPD low time counter
	0xB012	HPD_CMD	0x00	eDPRx HPD command
	0xB013-0xB1FF	Reserved	-	-
eDPRx Link registers	0xB200	AUX_RES_TIMEOUT0	0x5B	eDPRx AUX response time out counter LSB
	0xB201	AUX_RES_TIMEOUT1	0x18	eDPRx AUX response time out counter MSB
	0xB202	AUX_REQ_TIMEOUT0	0x4C	eDPRx AUX request time out counter LSB
	0xB203	AUX_REQ_TIMEOUT1	0x4C	eDPRx AUX request time out counter MSB
	0xB204	AUX_I2C_MASTER_CTL	0x05	eDPRx AUX master control
	0xB205	AUX_I2C_FUNC_SEL	0x00	eDPRx AUX I2C function select
	0xB206	AUX_MODE_CTRL	0x00	eDPRx AUX mode control
	0xB207-0xB20F	Reserved	-	-
	0xB210	MAINLINK_MODE_CTRL	0x80	eDPRx MainLink mode control
	0xB211	VIDEO_CONTROL	0x00	eDPRx video control
	0xB212	DDA_VID0_SET	0x05	eDPRx test register
	0xB213	DDA_VID1_SET	0x01	eDPRx test register
	0xB214	DDA_VID2_SET	0x00	eDPRx test register
	0xB215	ALIGN_DECREMENT	0x20	eDPRx alignment decrement register
	0xB216	ALIGN_THRESHOLD	0x02	eDPRx alignment threshold register
	0xB217-0xB21F	Reserved	-	-
	0xB220	VIDEO_STATUS	0x02	eDPRx video status register
	0xB221	VB_ID	0x19	eDPRx vertical blanking ID
	0xB222	MSA0	0x00	eDPRx MSA monitor
	0xB223	MSA1	0x00	eDPRx MSA monitor
	0xB224	MSA2	0x00	eDPRx MSA monitor
	0xB225	MSA3	0x00	eDPRx MSA monitor
	0xB226	MSA4	0x00	eDPRx MSA monitor

Group	Address	Register	Initial	Description
	0xB227	MSA5	0x00	eDPRx MSA monitor
	0xB228	MSA6	0x00	eDPRx MSA monitor
	0xB229	MSA7	0x00	eDPRx MSA monitor
	0xB22A	MSA8	0x00	eDPRx MSA monitor
	0xB22B	MSA9	0x00	eDPRx MSA monitor
	0xB22C	MSA10	0x00	eDPRx MSA monitor
	0xB22D	MSA11	0x00	eDPRx MSA monitor
	0xB22E	MSA12	0x00	eDPRx MSA monitor
	0xB22F	MSA13	0x00	eDPRx MSA monitor
	0xB230	MSA14	0x00	eDPRx MSA monitor
	0xB231	MSA15	0x00	eDPRx MSA monitor
	0xB232	MSA16	0x00	eDPRx MSA monitor
	0xB233	MSA17	0x00	eDPRx MSA monitor
	0xB234	MSA18	0x00	eDPRx MSA monitor
	0xB235	MSA19	0x00	eDPRx MSA monitor
	0xB236	MSA20	0x00	eDPRx MSA monitor
	0xB237	MSA21	0x00	eDPRx MSA monitor
	0xB238	MSA22	0x00	eDPRx MSA monitor
	0xB239	MSA23	0x00	eDPRx MSA monitor
	0xB23A-0xB23F	Reserved	-	-
eDPRx Link registers	0xB240	SDP_CONTROL	0x00	eDPRx SDP control
	0xB241	SDP_RECEIVE0	0x00	eDPRx SDP receive status
	0xB242	SDP_RECEIVE1	0x00	eDPRx SDP receive status
	0xB243	SDP_CHANGE0	0x00	eDPRx SDP change status
	0xB244	SDP_CHANGE1	0x00	eDPRx SDP change status
	0xB245	SDP_CLEAR0	0x00	eDPRx SDP condition clear
	0xB246	SDP_CLEAR1	0x00	eDPRx SDP condition clear
	0xB247	EN_IRQ_SDP_RECEIVE0	0x00	eDPRx SDP receive interrupt enable
	0xB248	EN_IRQ_SDP_RECEIVE1	0x00	eDPRx SDP receive interrupt enable
	0xB249	EN_IRQ_SDP_CHANGE0	0x00	eDPRx SDP change interrupt enable
	0xB24A	EN_IRQ_SDP_CHANGE1	0x00	eDPRx SDP change interrupt enable
	0xB24B	EN_IRQ_SDP_CLEAR0	0x00	eDPRx SDP condition clear interrupt enable
	0xB24C	EN_IRQ_SDP_CLEAR1	0x00	eDPRx SDP condition clear interrupt enable
	0xB24D	SDP_PKCLR0	0x00	eDPRx SDP packet auto clear enable
	0xB24E	SDP_PKCLR1	0x00	eDPRx SDP packet auto clear enable
	0xB24F	SDP_CLR_CMD0	0x00	eDPRx SDP packet clear
	0xB250	SDP_CLR_CMD1	0x00	eDPRx SDP packet clear
	0xB251	EXTENSION_LIMIT	0x00	eDPRx SDP packet clear limit
	0xB252	ISRC_LIMIT	0x00	eDPRx SDP packet clear limit
	0xB253	VSC_LIMIT	0x00	eDPRx SDP packet clear limit
	0xB254	VS_LIMIT	0x00	eDPRx SDP packet clear limit
	0xB255	AVI_LIMIT	0x00	eDPRx SDP packet clear limit

Group	Address	Register	Initial	Description
eDPRx Link registers	0xB256	SPD_LIMIT	0x00	eDPRx SDP packet clear limit
	0xB257	AUDIO_INFO_LIMIT	0x00	eDPRx SDP packet clear limit
	0xB258	MS_LIMIT	0x00	eDPRx SDP packet clear limit
	0xB259	NTSC_LIMIT	0x00	eDPRx SDP packet clear limit
	0xB25A-0x825F	Reserved	-	-
	0xB260	EXTENSION_ERR_POS	0x00	eDPRx extension error position
	0xB261	EXTENSION_HB0	0x00	eDPRx extension header byte
	0xB262	EXTENSION_HB1	0x00	eDPRx extension header byte
	0xB263	EXTENSION_HB2	0x00	eDPRx extension header byte
	0xB264	EXTENSION_HB3	0x00	eDPRx extension header byte
	0xB265	EXTENSION_DB0	0x00	eDPRx extension data byte
	0xB266	EXTENSION_DB1	0x00	eDPRx extension data byte
	0xB267	EXTENSION_DB2	0x00	eDPRx extension data byte
	0xB268	EXTENSION_DB3	0x00	eDPRx extension data byte
	0xB269	EXTENSION_DB4	0x00	eDPRx extension data byte
	0xB26A	EXTENSION_DB5	0x00	eDPRx extension data byte
	0xB26B	EXTENSION_DB6	0x00	eDPRx extension data byte
	0xB26C	EXTENSION_DB7	0x00	eDPRx extension data byte
	0xB26D	EXTENSION_DB8	0x00	eDPRx extension data byte
	0xB26E	EXTENSION_DB9	0x00	eDPRx extension data byte
	0xB26F	EXTENSION_DB10	0x00	eDPRx extension data byte
	0xB270	EXTENSION_DB11	0x00	eDPRx extension data byte
	0xB271	EXTENSION_DB12	0x00	eDPRx extension data byte
	0xB272	EXTENSION_DB13	0x00	eDPRx extension data byte
	0xB273	EXTENSION_DB14	0x00	eDPRx extension data byte
	0xB274	EXTENSION_DB15	0x00	eDPRx extension data byte
	0xB275	EXTENSION_DB16	0x00	eDPRx extension data byte
	0xB276	EXTENSION_DB17	0x00	eDPRx extension data byte
	0xB277	EXTENSION_DB18	0x00	eDPRx extension data byte
	0xB278	EXTENSION_DB19	0x00	eDPRx extension data byte
	0xB279	EXTENSION_DB20	0x00	eDPRx extension data byte
	0xB27A	EXTENSION_DB21	0x00	eDPRx extension data byte
	0xB27B	EXTENSION_DB22	0x00	eDPRx extension data byte
	0xB27C	EXTENSION_DB23	0x00	eDPRx extension data byte
	0xB27D	EXTENSION_DB24	0x00	eDPRx extension data byte
	0xB27E	EXTENSION_DB25	0x00	eDPRx extension data byte
	0xB27F	EXTENSION_DB26	0x00	eDPRx extension data byte
	0xB280	EXTENSION_DB27	0x00	eDPRx extension data byte
	0xB281	EXTENSION_DB28	0x00	eDPRx extension data byte
	0xB282	EXTENSION_DB29	0x00	eDPRx extension data byte
	0xB283	EXTENSION_DB30	0x00	eDPRx extension data byte
	0xB284	EXTENSION_DB31	0x00	eDPRx extension data byte
	0xB285-0xB28F	Reserved	-	-
	0xB290	ISRC_ERR_POS	0x00	eDPRx ISRC error position

Group	Address	Register	Initial	Description
	0xB291	ISRC_HB0	0x00	eDPRx ISRC header byte
	0xB292	ISRC_HB1	0x00	eDPRx ISRC header byte
	0xB293	ISRC_HB2	0x00	eDPRx ISRC header byte
	0xB294	ISRC_HB3	0x00	eDPRx ISRC header byte
	0xB295	ISRC_DB0	0x00	eDPRx ISRC data byte
	0xB296	ISRC_DB1	0x00	eDPRx ISRC data byte
	0xB297	ISRC_DB2	0x00	eDPRx ISRC data byte
	0xB298	ISRC_DB3	0x00	eDPRx ISRC data byte
	0xB299	ISRC_DB4	0x00	eDPRx ISRC data byte
	0xB29A	ISRC_DB5	0x00	eDPRx ISRC data byte
	0xB29B	ISRC_DB6	0x00	eDPRx ISRC data byte
	0xB29C	ISRC_DB7	0x00	eDPRx ISRC data byte
	0xB29D	ISRC_DB8	0x00	eDPRx ISRC data byte
	0xB29E	ISRC_DB9	0x00	eDPRx ISRC data byte
	0xB29F	ISRC_DB10	0x00	eDPRx ISRC data byte
	0xB2A0	ISRC_DB11	0x00	eDPRx ISRC data byte
	0xB2A1	ISRC_DB12	0x00	eDPRx ISRC data byte
	0xB2A2	ISRC_DB13	0x00	eDPRx ISRC data byte
	0xB2A3	ISRC_DB14	0x00	eDPRx ISRC data byte
	0xB2A4	ISRC_DB15	0x00	eDPRx ISRC data byte
	0xB2A5-0xB2AF	Reserved	-	-
	0xB2B0	VSC_ERR_POS	0x00	eDPRx VSC error position
	0xB2B1	VSC_HB0	0x00	eDPRx VSC header byte
	0xB2B2	VSC_HB1	0x00	eDPRx VSC header byte
	0xB2B3	VSC_HB2	0x00	eDPRx VSC header byte
eDPRx	0xB2B4	VSC_HB3	0x00	eDPRx VSC header byte
Link	0xB2B5	VSC_DB0	0x00	eDPRx VSC data byte
registers	0xB2B6	VSC_DB1	0x00	eDPRx VSC data byte
	0xB2B7	VSC_DB2	0x00	eDPRx VSC data byte
	0xB2B8	VSC_DB3	0x00	eDPRx VSC data byte
	0xB2B9	VSC_DB4	0x00	eDPRx VSC data byte
	0xB2BA	VSC_DB5	0x00	eDPRx VSC data byte
	0xB2BB	VSC_DB6	0x00	eDPRx VSC data byte
	0xB2BC	VSC_DB7	0x00	eDPRx VSC data byte
	0xB2BD	VSC_DB8	0x00	eDPRx VSC data byte
	0xB2BE	VSC_DB9	0x00	eDPRx VSC data byte
	0xB2BF	VSC_DB10	0x00	eDPRx VSC data byte
	0xB2C0	VSC_DB11	0x00	eDPRx VSC data byte
	0xB2C1	VSC_DB12	0x00	eDPRx VSC data byte
	0xB2C2	VSC_DB13	0x00	eDPRx VSC data byte
	0xB2C3	VSC_DB14	0x00	eDPRx VSC data byte
	0xB2C4	VSC_DB15	0x00	eDPRx VSC data byte
	0xB2C5	VSC_DB16	0x00	eDPRx VSC data byte
	0xB2C6	VSC_DB17	0x00	eDPRx VSC data byte
	0xB2C7	VSC_DB18	0x00	eDPRx VSC data byte
	0xB2C8	VSC_DB19	0x00	eDPRx VSC data byte
	0xB2C9	VSC_DB20	0x00	eDPRx VSC data byte
	0xB2CA	VSC_DB21	0x00	eDPRx VSC data byte
	0xB2CB	VSC_DB22	0x00	eDPRx VSC data byte
	0xB2CC	VSC_DB23	0x00	eDPRx VSC data byte
	0xB2CD	VSC_DB24	0x00	eDPRx VSC data byte
	0xB2CE	VSC_DB25	0x00	eDPRx VSC data byte
	0xB2CF	VSC_DB26	0x00	eDPRx VSC data byte
	0xB2D0	VSC_DB27	0x00	eDPRx VSC data byte

2015-10-05

Group	Address	Register	Initial	Description
	0xB2D1	VSC_DB28	0x00	eDPRx VSC data byte
	0xB2D2	VSC_DB29	0x00	eDPRx VSC data byte
	0xB2D3	VSC_DB30	0x00	eDPRx VSC data byte
	0xB2D4	VSC_DB31	0x00	eDPRx VSC data byte
	0xB2D5- 0xB2DF	Reserved	-	-
	0xB2E0	VS_ERR_POS	0x00	eDPRx VS error position
	0xB2E1	VS_HB0	0x00	eDPRx VS header byte
	0xB2E2	VS_HB1	0x00	eDPRx VS header byte
	0xB2E3	VS_HB2	0x00	eDPRx VS header byte
	0xB2E4	VS_HB3	0x00	eDPRx VS header byte
	0xB2E5	VS_DB0	0x00	eDPRx VS data byte
	0xB2E6	VS_DB1	0x00	eDPRx VS data byte
	0xB2E7	VS_DB2	0x00	eDPRx VS data byte
	0xB2E8	VS_DB3	0x00	eDPRx VS data byte
	0xB2E9	VS_DB4	0x00	eDPRx VS data byte
	0xB2EA	VS_DB5	0x00	eDPRx VS data byte
	0xB2EB	VS_DB6	0x00	eDPRx VS data byte
	0xB2EC	VS_DB7	0x00	eDPRx VS data byte
	0xB2ED	VS_DB8	0x00	eDPRx VS data byte
	0xB2EE	VS_DB9	0x00	eDPRx VS data byte
	0xB2EF	VS_DB10	0x00	eDPRx VS data byte
	0xB2F0	VS_DB11	0x00	eDPRx VS data byte
	0xB2F1	VS_DB12	0x00	eDPRx VS data byte
	0xB2F2	VS_DB13	0x00	eDPRx VS data byte
	0xB2F3	VS_DB14	0x00	eDPRx VS data byte
eDPRx Link registers	0xB2F4	VS_DB15	0x00	eDPRx VS data byte
	0xB2F5	VS_DB16	0x00	eDPRx VS data byte
	0xB2F6	VS_DB17	0x00	eDPRx VS data byte
	0xB2F7	VS_DB18	0x00	eDPRx VS data byte
	0xB2F8	VS_DB19	0x00	eDPRx VS data byte
	0xB2F9	VS_DB20	0x00	eDPRx VS data byte
	0xB2FA	VS_DB21	0x00	eDPRx VS data byte
	0xB2FB	VS_DB22	0x00	eDPRx VS data byte
	0xB2FC	VS_DB23	0x00	eDPRx VS data byte
	0xB2FD	VS_DB24	0x00	eDPRx VS data byte
	0xB2FE	VS_DB25	0x00	eDPRx VS data byte
	0xB2FF	VS_DB26	0x00	eDPRx VS data byte
	0xB300	VS_DB27	0x00	eDPRx VS data byte
	0xB301- 0xB30F	Reserved	-	-
	0xB310	AVI_ERR_POS	0x00	eDPRx AVI error position
	0xB311	AVI_HB0	0x00	eDPRx AVI header byte
	0xB312	AVI_HB1	0x00	eDPRx AVI header byte
	0xB313	AVI_HB2	0x00	eDPRx AVI header byte
	0xB314	AVI_HB3	0x00	eDPRx AVI header byte
	0xB315	AVI_DB0	0x00	eDPRx AVI data byte
	0xB316	AVI_DB1	0x00	eDPRx AVI data byte
	0xB317	AVI_DB2	0x00	eDPRx AVI data byte
	0xB318	AVI_DB3	0x00	eDPRx AVI data byte
	0xB319	AVI_DB4	0x00	eDPRx AVI data byte
	0xB31A	AVI_DB5	0x00	eDPRx AVI data byte
	0xB31B	AVI_DB6	0x00	eDPRx AVI data byte
	0xB31C	AVI_DB7	0x00	eDPRx AVI data byte
	0xB31D	AVI_DB8	0x00	eDPRx AVI data byte

2015-10-05

Group	Address	Register	Initial	Description
	0xB31E	AVI_DB9	0x00	eDPRx AVI data byte
	0xB31F	AVI_DB10	0x00	eDPRx AVI data byte
	0xB320	AVI_DB11	0x00	eDPRx AVI data byte
	0xB321	AVI_DB12	0x00	eDPRx AVI data byte
	0xB322	AVI_DB13	0x00	eDPRx AVI data byte
	0xB323	AVI_DB14	0x00	eDPRx AVI data byte
	0xB324	AVI_DB15	0x00	eDPRx AVI data byte
	0xB325	AVI_DB16	0x00	eDPRx AVI data byte
	0xB326	AVI_DB17	0x00	eDPRx AVI data byte
	0xB327	AVI_DB18	0x00	eDPRx AVI data byte
	0xB328	AVI_DB19	0x00	eDPRx AVI data byte
	0xB329	AVI_DB20	0x00	eDPRx AVI data byte
	0xB32A	AVI_DB21	0x00	eDPRx AVI data byte
	0xB32B	AVI_DB22	0x00	eDPRx AVI data byte
	0xB32C	AVI_DB23	0x00	eDPRx AVI data byte
	0xB32D	AVI_DB24	0x00	eDPRx AVI data byte
	0xB32E	AVI_DB25	0x00	eDPRx AVI data byte
	0xB32F	AVI_DB26	0x00	eDPRx AVI data byte
	0xB330	AVI_DB27	0x00	eDPRx AVI data byte
	0xB331-0xB33F	Reserved	-	-
	0xB340	SPD_ERR_POS	0x00	eDPRx SPD error position
	0xB341	SPD_HB0	0x00	eDPRx SPD header byte
	0xB342	SPD_HB1	0x00	eDPRx SPD header byte
	0xB343	SPD_HB2	0x00	eDPRx SPD header byte
	0xB344	SPD_HB3	0x00	eDPRx SPD header byte
eDPRx	0xB345	SPD_DB0	0x00	eDPRx SPD data byte
Link	0xB346	SPD_DB1	0x00	eDPRx SPD data byte
registers	0xB347	SPD_DB2	0x00	eDPRx SPD data byte
	0xB348	SPD_DB3	0x00	eDPRx SPD data byte
	0xB349	SPD_DB4	0x00	eDPRx SPD data byte
	0xB34A	SPD_DB5	0x00	eDPRx SPD data byte
	0xB34B	SPD_DB6	0x00	eDPRx SPD data byte
	0xB34C	SPD_DB7	0x00	eDPRx SPD data byte
	0xB34D	SPD_DB8	0x00	eDPRx SPD data byte
	0xB34E	SPD_DB9	0x00	eDPRx SPD data byte
	0xB34F	SPD_DB10	0x00	eDPRx SPD data byte
	0xB350	SPD_DB11	0x00	eDPRx SPD data byte
	0xB351	SPD_DB12	0x00	eDPRx SPD data byte
	0xB352	SPD_DB13	0x00	eDPRx SPD data byte
	0xB353	SPD_DB14	0x00	eDPRx SPD data byte
	0xB354	SPD_DB15	0x00	eDPRx SPD data byte
	0xB355	SPD_DB16	0x00	eDPRx SPD data byte
	0xB356	SPD_DB17	0x00	eDPRx SPD data byte
	0xB357	SPD_DB18	0x00	eDPRx SPD data byte
	0xB358	SPD_DB19	0x00	eDPRx SPD data byte
	0xB359	SPD_DB20	0x00	eDPRx SPD data byte
	0xB35A	SPD_DB21	0x00	eDPRx SPD data byte
	0xB35B	SPD_DB22	0x00	eDPRx SPD data byte
	0xB35C	SPD_DB23	0x00	eDPRx SPD data byte
	0xB35D	SPD_DB24	0x00	eDPRx SPD data byte
	0xB35E	SPD_DB25	0x00	eDPRx SPD data byte
	0xB35F	SPD_DB26	0x00	eDPRx SPD data byte
	0xB360	SPD_DB27	0x00	eDPRx SPD data byte

Group	Address	Register	Initial	Description
	0xB361-0xB36F	Reserved	-	-
	0xB370-0xB39F	Reserved	-	-
	0xB3A0	MS_ERR_POS	0x00	eDPRx MS error position
	0xB3A1	MS_HB0	0x00	eDPRx MS header byte
	0xB3A2	MS_HB1	0x00	eDPRx MS header byte
	0xB3A3	MS_HB2	0x00	eDPRx MS header byte
	0xB3A4	MS_HB3	0x00	eDPRx MS header byte
	0xB3A5	MS_DB0	0x00	eDPRx MS data byte
	0xB3A6	MS_DB1	0x00	eDPRx MS data byte
	0xB3A7	MS_DB2	0x00	eDPRx MS data byte
	0xB3A8	MS_DB3	0x00	eDPRx MS data byte
	0xB3A9	MS_DB4	0x00	eDPRx MS data byte
	0xB3AA	MS_DB5	0x00	eDPRx MS data byte
	0xB3AB	MS_DB6	0x00	eDPRx MS data byte
	0xB3AC	MS_DB7	0x00	eDPRx MS data byte
	0xB3AD	MS_DB8	0x00	eDPRx MS data byte
	0xB3AE	MS_DB9	0x00	eDPRx MS data byte
	0xB3AF	MS_DB10	0x00	eDPRx MS data byte
	0xB3B0	MS_DB11	0x00	eDPRx MS data byte
	0xB3B1	MS_DB12	0x00	eDPRx MS data byte
	0xB3B2	MS_DB13	0x00	eDPRx MS data byte
	0xB3B3	MS_DB14	0x00	eDPRx MS data byte
	0xB3B4	MS_DB15	0x00	eDPRx MS data byte
	0xB3B5	MS_DB16	0x00	eDPRx MS data byte
eDPRx	0xB3B6	MS_DB17	0x00	eDPRx MS data byte
Link	0xB3B7	MS_DB18	0x00	eDPRx MS data byte
registers	0xB3B8	MS_DB19	0x00	eDPRx MS data byte
	0xB3B9	MS_DB20	0x00	eDPRx MS data byte
	0xB3BA	MS_DB21	0x00	eDPRx MS data byte
	0xB3BB	MS_DB22	0x00	eDPRx MS data byte
	0xB3BC	MS_DB23	0x00	eDPRx MS data byte
	0xB3BD	MS_DB24	0x00	eDPRx MS data byte
	0xB3BE	MS_DB25	0x00	eDPRx MS data byte
	0xB3BF	MS_DB26	0x00	eDPRx MS data byte
	0xB3C0	MS_DB27	0x00	eDPRx MS data byte
	0xB3C1-0xB3CF	Reserved	-	-
	0xB3D0	NTSC_ERR_POS	0x00	eDPRx NTSC error position
	0xB3D1	NTSC_HB0	0x00	eDPRx NTSC header byte
	0xB3D2	NTSC_HB1	0x00	eDPRx NTSC header byte
	0xB3D3	NTSC_HB2	0x00	eDPRx NTSC header byte
	0xB3D4	NTSC_HB3	0x00	eDPRx NTSC header byte
	0xB3D5	NTSC_DB0	0x00	eDPRx NTSC data byte
	0xB3D6	NTSC_DB1	0x00	eDPRx NTSC data byte
	0xB3D7	NTSC_DB2	0x00	eDPRx NTSC data byte
	0xB3D8	NTSC_DB3	0x00	eDPRx NTSC data byte
	0xB3D9	NTSC_DB4	0x00	eDPRx NTSC data byte
	0xB3DA	NTSC_DB5	0x00	eDPRx NTSC data byte
	0xB3DB	NTSC_DB6	0x00	eDPRx NTSC data byte
	0xB3DC	NTSC_DB7	0x00	eDPRx NTSC data byte
	0xB3DD	NTSC_DB8	0x00	eDPRx NTSC data byte
	0xB3DE	NTSC_DB9	0x00	eDPRx NTSC data byte
	0xB3DF	NTSC_DB10	0x00	eDPRx NTSC data byte

Group	Address	Register	Initial	Description
eDPRx Link registers	0xB3E0	NTSC_DB11	0x00	eDPRx NTSC data byte
	0xB3E1	NTSC_DB12	0x00	eDPRx NTSC data byte
	0xB3E2	NTSC_DB13	0x00	eDPRx NTSC data byte
	0xB3E3	NTSC_DB14	0x00	eDPRx NTSC data byte
	0xB3E4	NTSC_DB15	0x00	eDPRx NTSC data byte
	0xB3E5	NTSC_DB16	0x00	eDPRx NTSC data byte
	0xB3E6	NTSC_DB17	0x00	eDPRx NTSC data byte
	0xB3E7	NTSC_DB18	0x00	eDPRx NTSC data byte
	0xB3E8	NTSC_DB19	0x00	eDPRx NTSC data byte
	0xB3E9	NTSC_DB20	0x00	eDPRx NTSC data byte
	0xB3EA	NTSC_DB21	0x00	eDPRx NTSC data byte
	0xB3EB	NTSC_DB22	0x00	eDPRx NTSC data byte
	0xB3EC	NTSC_DB23	0x00	eDPRx NTSC data byte
	0xB3ED	NTSC_DB24	0x00	eDPRx NTSC data byte
	0xB3EE	NTSC_DB25	0x00	eDPRx NTSC data byte
	0xB3EF	NTSC_DB26	0x00	eDPRx NTSC data byte
	0xB3F0	NTSC_DB27	0x00	eDPRx NTSC data byte
	0xB3F1-0xB3FF	Reserved	-	-
eDPRx ALPM registers	0xB400	AL_MODE_CTRL	0x01	eDPRx ALPM mode control
	0xB401	AL_LNKTRN_CTRL0	0xB0	eDPRx Full Link Training time out setting
	0xB402	AL_LNKTRN_CTRL1	0x1E	eDPRx Full Link Training time out setting
	0xB403	AL_LNKTRN_CTRL2	0x04	eDPRx Full Link Training time out setting
	0xB404	AL_LNKTRN_CTRL3	0x78	eDPRx Fast Link Training time out setting
	0xB405	AL_LNKTRN_CTRL4	0x69	eDPRx Fast Link Training time out setting
	0xB406	AL_LNKTRN_CTRL5	0x00	eDPRx Fast nk Training time out setting
	0xB407	AL_FIFO_CTRL0	0x22	eDPRx test register
	0xB408	AL_FIFO_CTRL1	0x22	eDPRx test register
	0xB409	AL_LOCKTIME_CTRL0	0x24	eDPRx ALPM lock time control
	0xB40A	AL_LOCKTIME_CTRL1	0x1C	eDPRx ALPM lock time control
	0xB40B	AL_LOCKTIME_CTRL2	0x02	eDPRx ALPM lock time control
	0xB40C	AL_ALPM_STS_CLR	0x00	eDPRx ALPM status clear
	0xB40D	AL_ALPM_STS0	0x00	eDPRx ALPM status
	0xB40E	AL_ALPM_STS1	0x00	eDPRx ALPM status
	0xB40F	AL_ERR_STS	0x00	eDPRx ALPM error status
	0xB410	AL_STATE_MON	0x00	eDPRx test register
	0xB411	EN_IRQ_AL_ERR_STS	0x00	eDPRx ALPM interrupt enable
	0xB412-0xB41F	Reserved	-	-
	0xB420	AL_OFFDLY_CTRL0	0x46	eDPRx off delay control
	0xB421	AL_OFFDLY_CTRL1	0x05	eDPRx off delay control
	0xB422	AL_OFFDLY_CTRL2	0x8C	eDPRx off delay control
	0xB423	AL_OFFDLY_CTRL3	0x0A	eDPRx off delay control
	0xB424	AL_OFFDLY_CTRL4	0xD2	eDPRx off delay control
	0xB425	AL_OFFDLY_CTRL5	0x0F	eDPRx off delay control

Group	Address	Register	Initial	Description
eDPRx ALPM registers	0xB426	AL_OFFDLY_CTRL6	0x18	eDPRx off delay control
	0xB427	AL_OFFDLY_CTRL7	0x15	eDPRx off delay control
	0xB428	AL_SLEEPDLY_CTRL0	0x8C	eDPRx sleep delay control
	0xB429	AL_SLEEPDLY_CTRL1	0x0A	eDPRx sleep delay control
	0xB42A	AL_SLEEPDLY_CTRL2	0x18	eDPRx sleep delay control
	0xB42B	AL_SLEEPDLY_CTRL3	0x15	eDPRx sleep delay control
	0xB42C	AL_SLEEPDLY_CTRL4	0xA4	eDPRx sleep delay control
	0xB42D	AL_SLEEPDLY_CTRL5	0x1F	eDPRx sleep delay control
	0xB42E	AL_SLEEPDLY_CTRL6	0x30	eDPRx sleep delay control
	0xB42F	AL_SLEEPDLY_CTRL7	0x2A	eDPRx sleep delay control
	0xB430	AL_ALIGNDONEDLY_CTRL	0x04	eDPRx test register
	0xB431-0xB5FF	Reserved	-	-
eDPRx PHY1 registers	0xB600	PL_AUX_UI_CTRL0	0x08	eDPRx AUX test register
	0xB601	PL_AUX_UI_CTRL1	0x0E	eDPRx AUX test register
	0xB602	PL_AUX_UI_CTRL2	0x1B	eDPRx AUX test register
	0xB603	PL_AUX_UI_STS	0x00	eDPRx AUX test register
	0xB604	PL_AUX_BUSPARK_CTRL0	0x00	eDPRx AUX test register
	0xB605	PL_AUX_BUSPARK_CTRL1	0x00	eDPRx AUX test register
	0xB606	PL_AUX_RESET_CTRL	0x00	eDPRx AUX-CH reset
	0xB607	PL_AUX_STATE_MON	0x00	eDPRx AUX test register
	0xB608	PL_AUX_IO_CTRL0	0x08	eDPRx AUX-CH I/O control
	0xB609	PL_AUX_IO_CTRL1	0x00	eDPRx AUX-CH I/O test register
	0xB60A	PL_AUX_IO_TST_CTR	0x00	eDPRx AUX-CH I/O test register
	0xB60B-0xB60F	Reserved	-	-
	0xB610	PL_AUXTX_MODE_CTRL	0x00	eDPRx AUX-CH test register
	0xB611	PL_AUXTX_PRECHRG_CTRL	0x10	eDPRx AUX-CH test register
	0xB612	PL_AUXTX_EYEPAT_CTRL0	0x00	eDPRx AUX-CH test register
	0xB613	PL_AUXTX_EYEPAT_CTRL1	0x0D	eDPRx AUX-CH test register
	0xB614	PL_AUXTX_EYEPAT_CTRL2	0x20	eDPRx AUX-CH test register
	0xB615	PL_AUXTX_EYEPAT_CTRL3	0x10	eDPRx AUX-CH test register
	0xB616	PL_AUXTX_EYEPAT_CTRL4	0x0D	eDPRx AUX-CH test register
	0xB617	PL_AUXTX_EYEPAT_CTRL5	0x00	eDPRx AUX-CH test register
	0xB618-0xB61F	Reserved	-	-
	0xB620	PL_AUXRX_MODE_CTRL	0x01	eDPRx AUX-CH Rx mode control
	0xB621	PL_AUXRX_SMPL_DLY_CTRL0	0x00	eDPRx AUX-CH Rx Test register
	0xB622	PL_AUXRX_SMPL_DLY_CTRL1	0x00	eDPRx AUX-CH Rx Test register
	0xB623	PL_AUXRX_SMPL_DLY_CTRL2	0x00	eDPRx AUX-CH Rx Test register
	0xB624	PL_AUXRX_SMPL_DLY_CTRL3	0x00	eDPRx AUX-CH Rx Test register
	0xB625	PL_AUXRX_SYNC_CNT_CTRL0	0x0F	eDPRx AUX-CH Rx sync pattern count control
	0xB626	PL_AUXRX_SYNC_CNT_CTRL1	0x07	eDPRx AUX-CH Rx sync pattern count control
	0xB627	PL_AUXRX_SYNC_CNT_STS0	0x00	eDPRx AUX-CH Rx sync pattern count status
	0xB628	PL_AUXRX_SYNC_CNT_STS1	0x00	eDPRx AUX-CH Rx sync pattern count status

Group	Address	Register	Initial	Description
eDPRx PHY1 registers	0xB629	PL_AUXRX_ERR_STS0	0x00	eDPRx AUX-CH Rx error status
	0xB62A	PL_AUXRX_ERR_STS1	0x00	eDPRx AUX-CH Rx error status
	0xB62B	PL_AUXRX_ERR_STS2	0x00	eDPRx AUX-CH Rx error status
	0xB62C	PL_AUXRX_ERR_STS3	0x00	eDPRx AUX-CH Rx error status
	0xB62D	PL_RCOSC_CTRL	0x00	eDPRx Main-Link test register
	0xB62E	PL_RCOSC_STS	0x00	eDPRx Main-Link test register
	0xB62F	PL_RCOSC_MON	0x00	eDPRx Main-Link test register
	0xB630	PL_MAINLINK_RESET_CTRL	0x00	eDPRx Main-Link reset control
	0xB631	PL_MAINLINK_STS	0x00	eDPRx Main-Link PHY status
	0xB632	PL_MAINLINK_REFCLK_CTRL	0x02	eDPRx Main-Link reference clock select
	0xB633	PL_MAINLINK_MODE_CTRL	0x00	eDPRx Main-Link mode control
	0xB634	PL_MAINLINK_AFE_CTRL0	0x20	eDPRx Main-Link AFE control
	0xB635	PL_MAINLINK_AFE_CTRL1	0x00	eDPRx Main-Link test register
	0xB636	PL_MAINLINK_AFE_STS0	0x00	eDPRx Main-Link AFE status
	0xB637	PL_MAINLINK_AFE_STS1	0x00	eDPRx Main-Link AFE status
	0xB638	PL_MAINLINK_AFE_RXEQ_CTRL0	0x00	eDPRx Main-Link AFE equalization control
	0xB639	PL_MAINLINK_AFE_RXEQ_CTRL1	0x00	eDPRx Main-Link AFE equalization control
	0xB63A	PL_MAINLINK_AFE_RXEQ_CTRL2	0x00	eDPRx Main-Link AFE equalization control
	0xB63B	PL_MAINLINK_AFE_RXEQ_CTRL3	0x00	eDPRx Main-Link AFE equalization control
	0xB63C	PL_MAINLINK_AFE_RXEQ_CTRL4	0x00	eDPRx Main-Link AFE equalization control
	0xB63D	PL_MAINLINK_AFE_RXEQ_CTRL5	0x00	eDPRx Main-Link AFE equalization control
	0xB63E	PL_MAINLINK_AFE_RXEQ_CTRL6	0x00	eDPRx Main-Link AFE equalization control
	0xB63F	PL_MAINLINK_AFE_RXEQ_CTRL7	0x00	eDPRx Main-Link AFE equalization control
	0xB640	PL_MAINLINK_AFE_RXEQ_STS0	0x00	eDPRx Main-Link AFE equalization status
	0xB641	PL_MAINLINK_AFE_RXEQ_STS1	0x00	eDPRx Main-Link AFE equalization status
	0xB642	PL_MAINLINK_AFE_RXEQ_STS2	0x00	eDPRx Main-Link AFE equalization status
	0xB643	PL_MAINLINK_AFE_RXEQ_STS3	0x00	eDPRx Main-Link AFE equalization status
	0xB644	PL_MAINLINK_AFE_RXEQ_STS4	0x00	eDPRx Main-Link AFE equalization status

Group	Address	Register	Initial	Description
eDPRx PHY1 registers	0xB645	PL_MAINLINK_AFE_RXEQ_STS5	0x00	eDPRx Main-Link AFE equalization status
	0xB646	PL_MAINLINK_AFE_RXEQ_STS6	0x00	eDPRx Main-Link AFE equalization status
	0xB647	PL_MAINLINK_AFE_RXEQ_STS7	0x00	eDPRx Main-Link AFE equalization status
	0xB648	PL_MAINLINK_AFE_DLY_STS	0x6A	eDPRx Main-Link test reister
	0xB649	Reserved	-	-
	0xB64A	PL_MAINLINK_AFE_ERR_STS	0x00	eDPRx Main-Link AFE error status
	0xB64B	PL_MAINLINK_FIFO_CTRL0	0x55	eDPRx Main-Link FIFO control
	0xB64C	PL_MAINLINK_FIFO_CTRL1	0x55	eDPRx Main-Link FIFO control
	0xB64D	PL_MAINLINK_FIFO_CTRL2	0x00	eDPRx Main-Link FIFO control
	0xB64E	PL_MAINLINK_FIFO_STS	0x00	eDPRx Main-Link FIFO status
	0xB64F	PL_MAINLINK_TSTPAT_CTRL0	0x00	eDPRx Main-Link test pattern control
	0xB650	PL_MAINLINK_TSTPAT_CTRL1	0x00	eDPRx Main-Link test pattern control
	0xB651	PL_MAINLINK_TSTPAT_CTRL2	0x00	eDPRx Main-Link test pattern control
	0xB652	PL_MAINLINK_TSTPAT_CTRL3	0x00	eDPRx Main-Link test pattern control
	0xB653	PL_MAINLINK_TSTPAT_CTRL4	0x00	eDPRx Main-Link test pattern control
	0xB654	PL_MAINLINK_TSTPAT_CTRL5	0x00	eDPRx Main-Link test pattern control
	0xB655	PL_MAINLINK_TSTPAT_CTRL6	0x00	eDPRx Main-Link test pattern control
	0xB656	PL_MAINLINK_TSTPAT_CTRL7	0x00	eDPRx Main-Link test pattern control
	0xB657	PL_MAINLINK_TSTPAT_CTRL8	0x00	eDPRx Main-Link test pattern control
	0xB658	PL_MAINLINK_TSTPAT_CTRL9	0x00	eDPRx Main-Link test pattern control
	0xB659	PL_MAINLINK_TSTPAT_CTRL10	0x00	eDPRx Main-Link test register
	0xB65A	PL_MAINLINK	0x2C	eDPRx Main-Link test register
	0xB65B	PL_MAINLINK_AFE_TST_CTR	0x00	eDPRx Main-Link test register
	0xB65C-0xB65F	Reserved	-	-
	0xB660	EN_IRQ_PL_AUXRX_ERR_STS0	0x00	eDPRx AUX-CH Rx error interrupt enable
	0xB661	EN_IRQ_PL_AUXRX_ERR_STS1	0x00	eDPRx AUX-CH Rx error interrupt enable
	0xB662	EN_IRQ_PL_AUXRX_ERR_STS2	0x00	eDPRx AUX-CH Rx error interrupt enable
	0xB663	EN_IRQ_PL_AUXRX_ERR_STS3	0x00	eDPRx AUX-CH Rx error interrupt enable
	0xB664	EN_IRQ_PL_MAINLINK_AFE_ERR_STS	0x00	eDPRx AUX-CH Rx error interrupt enable

Group	Address	Register	Initial	Description
eDPRx PHY1 registers	0xB665	EN_IRQ_PL_MAINLINK_FIFO_STS	0x00	eDPRx AUX-CH Rx error interrupt enable
	0xB666-0xB7FF	Reserved	-	-
eDPRX PHY2 registers	0xB800	RXPHY_CTRL	0x1E	
	0xB801-0xBFFF	Test only use	0xXX	eDPRx test register
	0xB88E	CR_OPT_WCNT0_AMP_REQ	0x17	TX_AMP_OUT change request Watchdog Timeout
	0xB88F	CR_OPT_WCNT1_AMP_REQ	0x15	
	0xB890-0xB899	Test only use	0xXX	eDPRx test register
	0xB89A	EQ_OPT_WCNT0_POSTREQ	0x17	TX_POST_OUT change request Watchdog Timeout
	0xB89B	EQ_OPT_WCNT1_POSTREQ	0x15	
	0xB89C-0xB8B1	Test only use	0xXX	eDPRx test register
	0xB8B2	RX_EYE_MX_RANGE_CTRL_0	0x57	RX_EYE_MX_RANGE Lookup Table for ch.0
	0xB8B3	RX_EYE_MX_RANGE_CTRL_1	0x45	RX_EYE_MX_RANGE Lookup Table for ch.1
	0xB8B4	RX_EYE_MX_RANGE_CTRL_2	0x57	RX_EYE_MX_RANGE Lookup Table for ch.2
	0xB8B5	RX_EYE_MX_RANGE_CTRL_3	0x45	RX_EYE_MX_RANGE Lookup Table for ch.3
	0xB8B6-0xB8E2	Test only use	0xXX	eDPRx test register
	0xB8E3	EQ control setting3	0x00	
	0xB8E4-0xB8EA	Test only use	0xXX	eDPRx test register
	0xB8EB	EQ control setting4	0x00	
	0xB8EC-0xBB15	Test only use	0xXX	eDPRx test register
	0xBB16	EQ control Enable	0x00	
	0xBB17	EQ control setting1	0x00	
	0xBB18	EQ control setting2	0x00	
	0xBB19-0xBBBF	Test only use	0xXX	eDPRx test register
	0xBBC0	COUNT1_LOWER	0xA6	
	0xBBC1	COUNT2_LOWER	0xD3	
	0xBBC2	COUNT_UPPER	0x70	
	0xBBC3-0xBBC4	Test only use	0xXX	eDPRx test register
	0xBBC5	OVERRIDE_CONTROL	0x00	
	0xBBC6-0xBBCA	Test only use	0xXX	eDPRx test register
	0xBBCB	PLL_FDBK_DIV2_MATCH	0x0C	
eDPRX Test registers	0xBBCC-0xBFFF	Test only use	0xXX	eDPRx test register

7. External connectivity
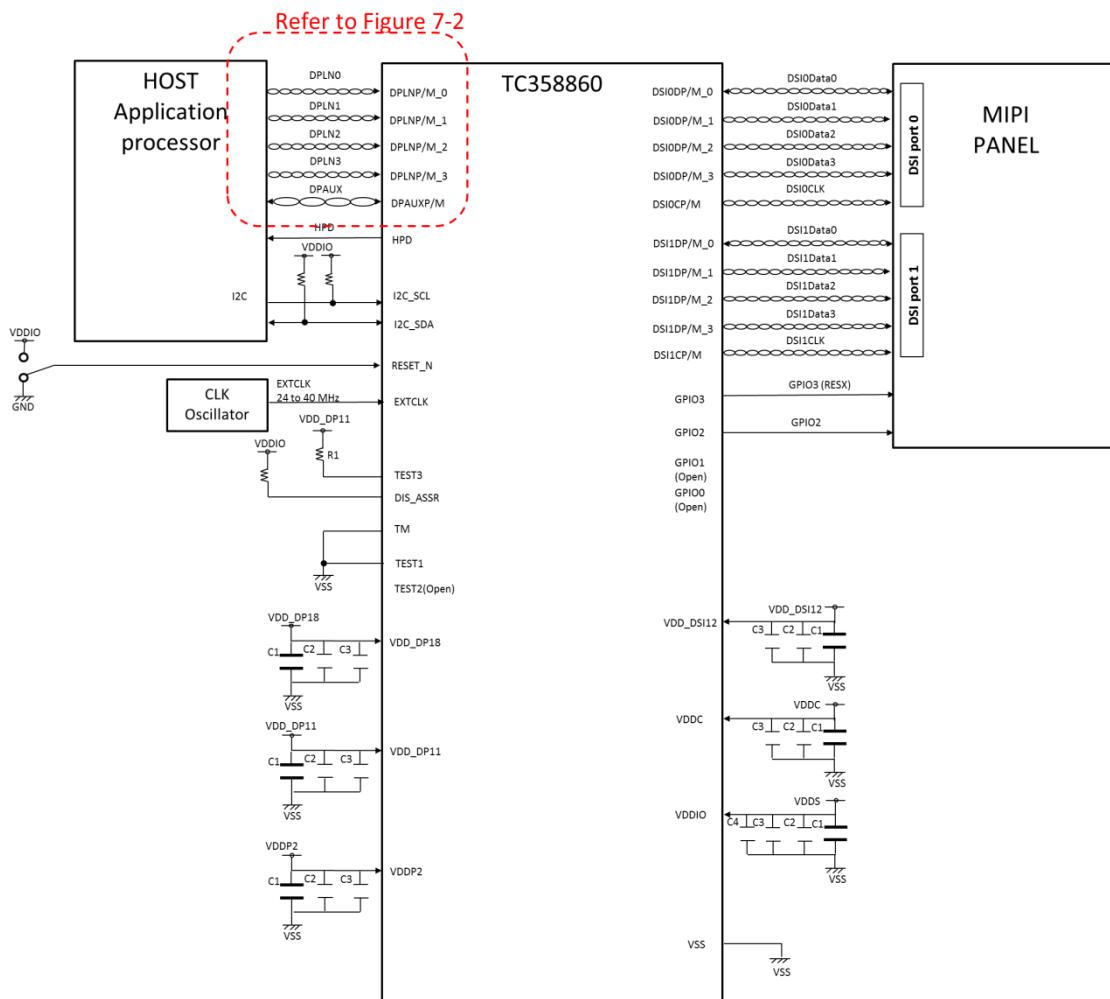
Figure 7-1   External connection of TC358860XBG

Table 7.1   Peripheral parts

Description	Symbol	Min.	Typ.	Max.	Unit
Tantalum capacitor	C1	--	10	--	µF
Ceramic capacitor	C2	--	0.1	--	µF
Ceramic capacitor	C3	--	0.01	--	µF
Ceramic capacitor	C4	--	100	--	pF
Resistor	R1	--	1	--	[kΩ]*1

Note1. Please use R1 resister with +-1% accuracy.
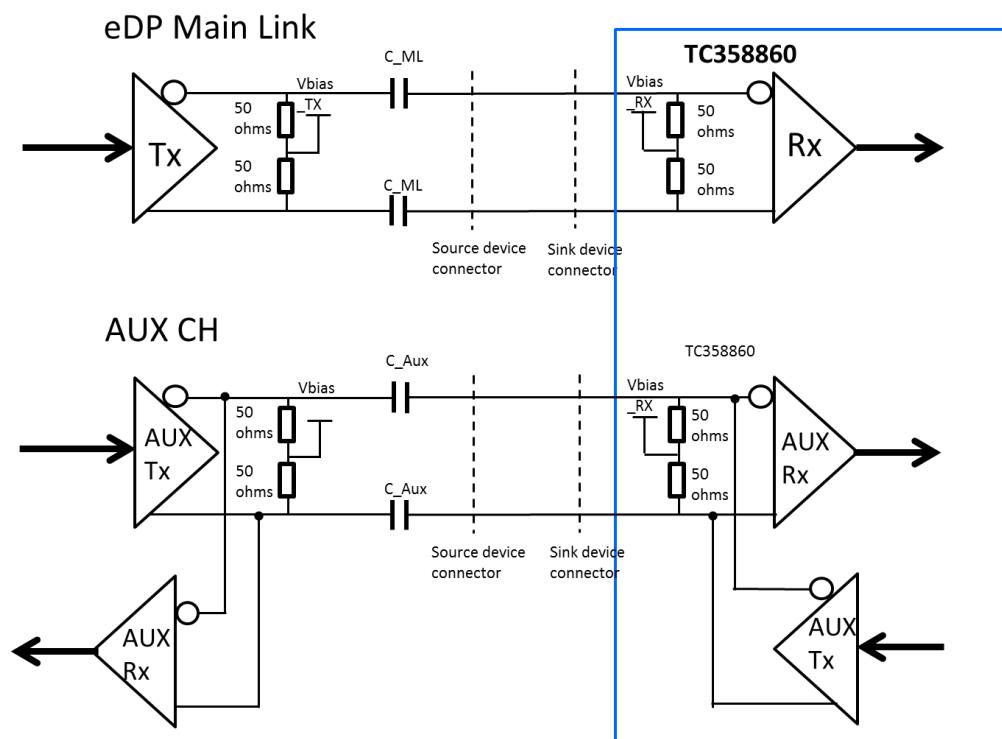
eDP Main Link

AUX CH

Figure 7-2   External connection of eDP main link and AUX CH

8. Package

TC358860XBG housed in a 5.0 mm by 5.0 mm size package with 0.5mm ball pitch. The detailed package drawing is shown below.
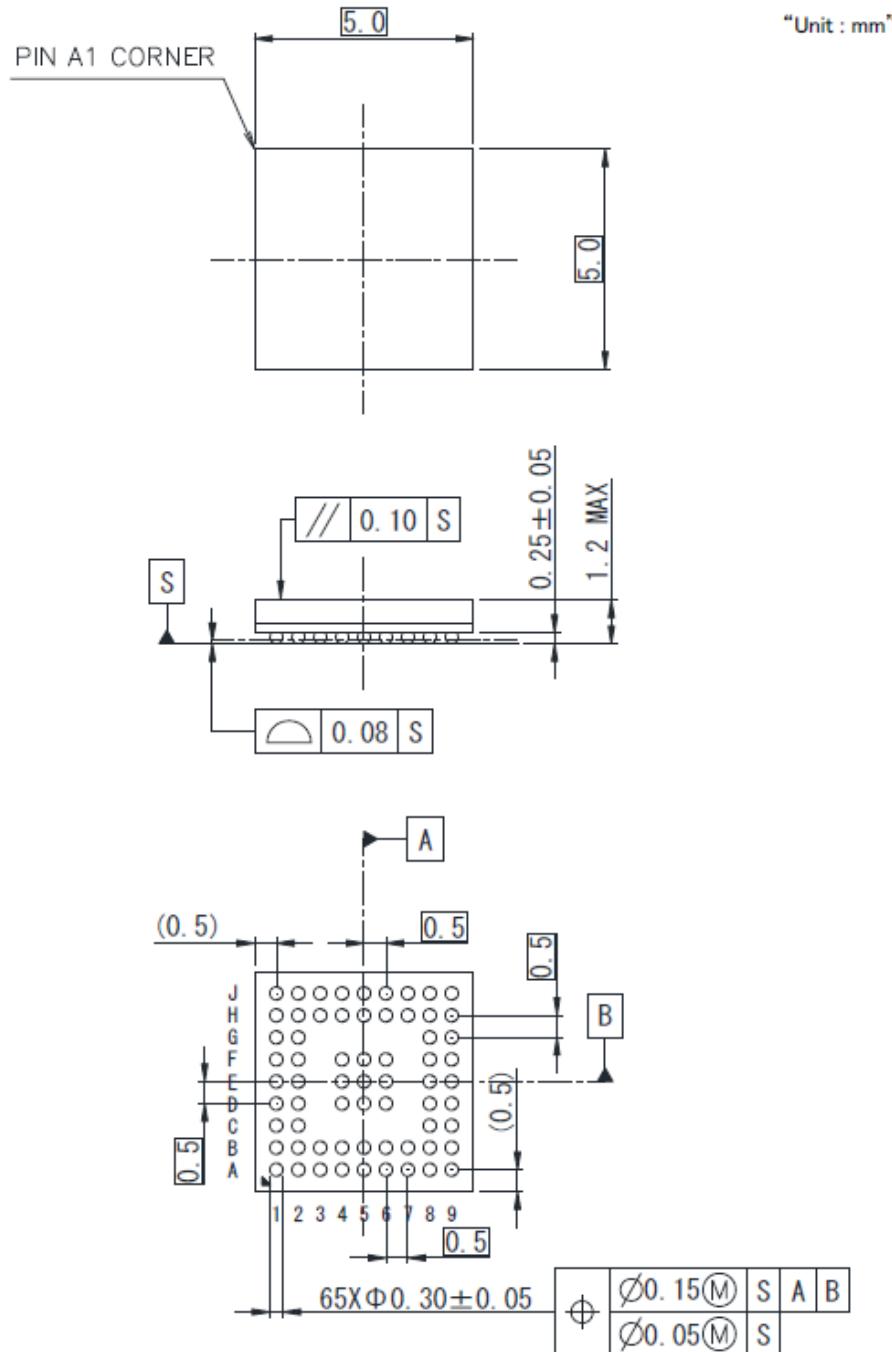
Figure 8-1   Package Dimension

Table 8.1   Package Details

Package	Solder Ball Pitch	Solder Ball Height	Package Dimension	Package Height	Note
65-Pin	0.50 mm	0.25mm	5.0 x 5.0 mm^2	1.2mm Max	

9. Power consumption during Typical Operations

1920x1080@60fps : 126 mW (eDP 1lane@5.4Gbps, Dual DPHY link@1Gbps)
2560x1600@60fps : 199 mW (eDP 2lane@5.4Gbps, Dual DPHY link@1Gbps)
3840x2160@60fps : 288 mW (eDP 4lane@5.4Gbps, Dual DPHY link@1Gbps)

Table 9.1 Power consumption

		VDDC	VDDP2	VDD_DP11	VDD_DP18	VDD_DSI0/1	VDDIO	Total
		1.1V	1,1V	1.1V	1.8V	1.2V	3.3V	[mW]
FHD:1920x1080 @60fps	Power (mW)	43.0	7.8	22.0	13.0	40.0	0.2	126
WQXGA:2560x1600 @60fps	Power (mW)	69.0	7.8	40.0	22.0	60.0 (30+30)	0.2	199
UHD: 3840x2160 @60fps	Power (mW)	113.0	7.8	74.0	33.0	60.0 (30+30)	0.2	288
Power Off1 (RESETN=L EXTCLK=L)	Power (mW)	0.7	0.0	0.4	0.0	0.1	0.0	1.2
Power off2 (RESETN=H, EXTCLK=25MHz, DPPHY disable) *1	Power (mW)	4.3	0.0	0.5	0.0	0.1	0.0	4.9

Note1: this number is measured after setting DPPHY disable

10. Electrical characteristics

10.1. Absolute Maximum Ratings

All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

Table 10.1 Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Supply voltage	(1.8V – Digital IO)	VDDIO	-0.3 to +1.96	V
	(3.3V – Digital IO)		-0.3 to +3.63	
Supply voltage	(1.1V – Digital Core)	VDDC	-0.3 to +1.54	V
Supply voltage	(1.2V – MIPI DSI PHY)	VDD_MIPI	-0.3 to +1.54	V
Supply voltage	(1.2V – PLL)	VDDP2	-0.3 to +1.54	V
Supply voltage	(1.8V – eDP PHY)	VDD_DP18	-0.3 to +1.98	V
Supply voltage	(1.1V – eDP PHY)	VDD_DP11	-0.3 to +1.54	V
Input voltage	(DSI I/O)	V_{IN_DSI}	-0.3 to VDD_MIPI+0.3	V
Output voltage	(DSI I/O)	V_{OUT_DSI}	-0.3 to VDD_MIPI+0.3	V
Input voltage	(Digital IO)	V_{IN_IO}	-0.3 to VDDIO+0.3	V
Output voltage	(Digital IO)	V_{OUT_IO}	-0.3 to VDDIO+0.3	V
Input current		Iin	-10 to +10	mA
Junction temperature		Tj	125	°C
Storage temperature		T_{stg}	-40 to +125	°C

10.2. Recommended Operating Conditions

Table 10.2   Recommended Operating Conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	(1.8V – Digital IO)	VDDIO	1.62	1.80	1.98	V
Supply voltage	(3.3V – Digital IO)	VDDIO	2.97	3.30	3.63	V
Supply voltage	(1.1V – PLL)	VDDP2	1.04	1.10	1.16	V
Supply voltage	(1.1V – Digital Core)	VDDC	1.04	1.10	1.16	V
Supply voltage	(1.1V – eDP PHY)	VDD_DP11	1.04	1.10	1.16	V
Supply voltage	(1.8V – eDP PHY)	VDD_DP18	1.71	1.8	1.89	V
Supply voltage	(1.2V – MIPI-DPHY)	VDD_MIPI0	1.1	1.2	1.25	V
		VDD_MIPI1				
Operating internal frequency		fopr	--	--	300	MHz
Operating temperature (ambient temperature with voltage applied)		T_a	-30	+25	+85	°C
Supply noise voltage		V_{SN}	--	--	100	mV_{pp}

10.3. DC Electrical Specification

All typical values are at normal operating conditions unless otherwise specified.

10.3.1. Normal CMOS I/Os DC Specifications

Table 10.3   Normal CMOS IOs DC Specifications

Parameter – CMOS I/Os	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage, High level Input Note1	V_{IH}	--	0.7 VDDIO	--	VDDIO +0.3V	V
Input voltage, Low level Input Note1	V_{IL}	--	VSS -0.3V	--	0.3 VDDIO	V
Input voltage High level CMOS Schmitt Trigger Note 1,2	V_{IHS}	--	0.7 VDDIO	--	VDDIO	V
Input voltage Low level CMOS Schmitt Trigger Note 1,2	V_{ILS}	--	0	--	0.3 VDDIO	V
Output voltage, High level Note1, 2	V_{OH}	I_{OH} = 1 mA	VDDIO -0.4V	--	VDDIO	V
Output voltage, Low level Note1, 2	V_{OL}	I_{OL} = 2 mA	--	--	0.4	V
Input leakage current, High level without Pull-down I/O pin	I_{ILH1}	V_{IN} = +VDDIO, VDDIO = 3.6 V	--	--	10	µA
Input leakage current, Low level	I_{ILL}	V_{IN} = 0 V, VDDIO = 3.6 V	--	--	10	µA

Notes:

1. Each power source is operating within recommended operating condition.
2. Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

10.3.2. MIPI DSI I/Os DC Specifications

Timing specification below has been ported from MIPI Alliance specification for D-PHY version 01-00-00.
Timing defined in MIPI Alliance specification for D-PHY version 01-00-00 has precedence over timing described in the sections below.
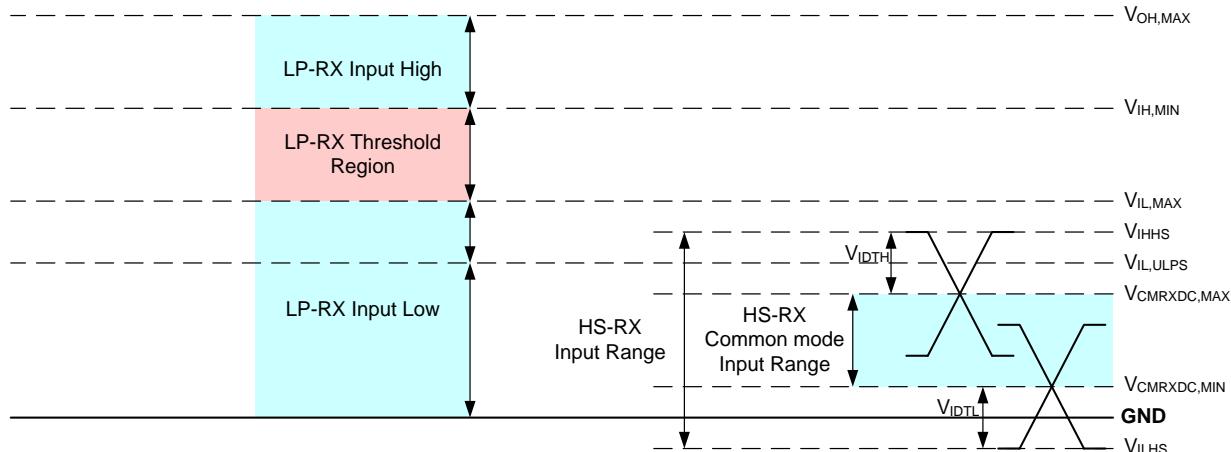

Figure 10-1   Signaling and voltage levels

Table 10.4   MIPI HSTX and LPTX DC specifications

Parameter	Description	Min.	Typ.	Max.	Units	Notes
HS mode						
VCMTX	HS transmit static common mode voltage	150	200	250	mV	1
$|\Delta$VCMTX(1,0)$|$	VCMTX mismatch when output is Differential-1 or Differential-0	--	--	5	mV	2
$|$VOD$|$	HS transmit differential voltage	140	200	270	mV	1
$|\Delta$VOD$|$	VOD mismatch when output is Differential-1 or Differential-0	--	--	14	mV	2
VOHHS	HS output high voltage	--	--	360	mV	
ZOS	Single ended output impedance	40	50	62.5	Ω	
ΔZOS	Single ended output impedance mismatch	--	--	10	%	
LP Mode						
VOH	Thevenin output high level	1.1	1.2	1.25	V	
VOL	Thevenin output low level	-50	--	50	mV	
ZOLP	Output impedance of LP transmitter	110	--	--	Ω	3

Notes:

1. Value when driving into load impedance anywhere in the ZID range.
2. It is recommended the implementer minimize ΔVOD and ΔVCMTX(1,0) in order to minimize radiation and optimize signal integrity.
3. Though no maximum value for ZOLP is specified, the LP transmitter output impedance shall ensure the TRLP/TFLP specification is met.

Table 10.5   LPRX DC Specification

Parameter	Description	Remarks	Min.	Typ.	Max.	Unit
V_{IL}	Input low threshold	Not in ULPS	--	--	550	mV
V_{IL-UPS}	Input low threshold in ULPS		--	--	300	mV
V_{IH}	Output high threshold		880	--	--	mV
V_{HYST}	Input hysteresis		25	--	--	mV

10.4. AC Timing specification

10.4.1. EXTCLK Input Requirement

Parameter	Min.	Typ.	Max.	Unit	Notes
Frequency	24	--	27	MHz	1
Duty Cycle	40	50	60	%	
Jitter	-100	0	100	ppm	

Note:

1. please use EXTCLK 24, 25, 26 and 27MHz

10.4.2. MIPI HSTX AC specification

Table 10.6   MIPI High Speed Tx AC specifications

Parameter	Description	Remarks	Min.	Typ.	Max.	Unit
$\Delta V_{CMTX(HF)}$	V_{CMTX} variation above 450 MHz	RMS value	--	--	15	mV
$\Delta V_{CMTX(LF)}$	V_{CMTX} variation between 50 and 450MHz	Peak value	--	--	25	mV
t_R and t_F	20%-80% rise and fall time	@ ≤ 1Gbps @ > 1Gbps	--	--	0.3	UI
			--	--	0.35	UI
			100	--	--	ps

Note:

1. UI is equal to 1/(2*fh). See section 7.3 for the definition of fh.

10.4.3. MIPI LPTX AC specification

Table 10.7   MIPI Low Power Tx AC characteristics

Parameter	Description		Min.	Typ.	Max.	Units	Notes
TRLP/TFLP	15%-85% rise time and fall time		--	--	25	ns	1
TREOT	30%-85% rise time and fall time		--	--	35	ns	1, 5, 6
	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	--	--	ns	4
		All other pulses	20	--	--	ns	4
TLP-PER-TX	Period of the LP exclusive-OR clock		90	--	--	ns	
δV/δtSR	Slew rate @ CLOAD = 0pF		--	--	500	mV/ns	1,2,3,7
	Slew rate @ CLOAD = 5pF		--	--	300	mV/ns	1,2,3,7
	Slew rate @ CLOAD = 20pF		--	--	250	mV/ns	1,2,3,7
	Slew rate @ CLOAD = 70pF		--	--	150	mV/ns	1,2,3,7
	Slew rate, C_{LOAD} = 0 – 70pF (Falling edge only)		30	--	--	mV/ns	
	Slew rate, C_{LOAD} = 0 – 70pF (Rising edge only, output voltage 400 – 700mV)		30	--	--	mV/ns	
	Slew rate, C_{LOAD} = 0 – 70pF (Rising edge only, output voltage 700 – 930mV, Vx is equal instantaneous output voltage minus 700mV)		30 -0.075* V_x	--	--	mV/ns	
CLOAD	Load capacitance		0	--	70	pF	1

Notes:

1. CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2 ns delay.
2. When the output voltage is between 15% and below 85% of the fully settled LP signal levels.
3. Measured as average across any 50 mV segment of the output signal transition.
4. This parameter value can be lower then TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior.
5. The rise-time of TREOT starts from the HS common-level at the moment the differential amplitude drops below 70 mV, due to stopping the differential drive.
6. With an additional load capacitance CCM between 0-60 pF on the termination center tap at RX side of the Lane.
7. This value represents a corner point in a piecewise linear curve.

10.4.4. MIPI LPRX AC specification
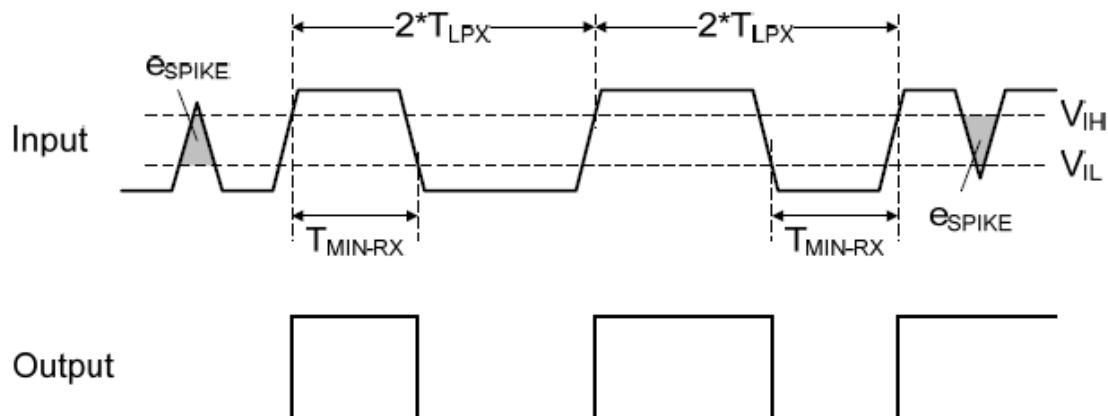
Figure 10-2   Input Glitch Rejection

Table 10.8   LPRX AC Specification

Parameter	Description	Remarks	Min.	Typ.	Max.	Unit
e_{SPIKE}	Input pulse rejection	Add. Digital filter required	--	--	300	V*ps
T_{MIN-RX}	Minimum pulse width response		20	--	--	ns
V_{INT}	Peak interference amplitude		-	--	200	mV
f_{INT}	Interference frequency		450	--	--	MHz

Notes:

1. Time-voltage integration of a spike above V_{IL} when being in LP-0 or below V_{IH} when being in LP-1 state.
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

Table 10.9   LPCD Specification

| Parameter	Description	Remarks	Min.	Typ.	Max.	Unit
SPECIFIcation						
V_{ILCD}	Logic 0 contention threshold		--	--	200	mV
V_{IHCD}	Logic 1 contention threshold		450	--	--	mV
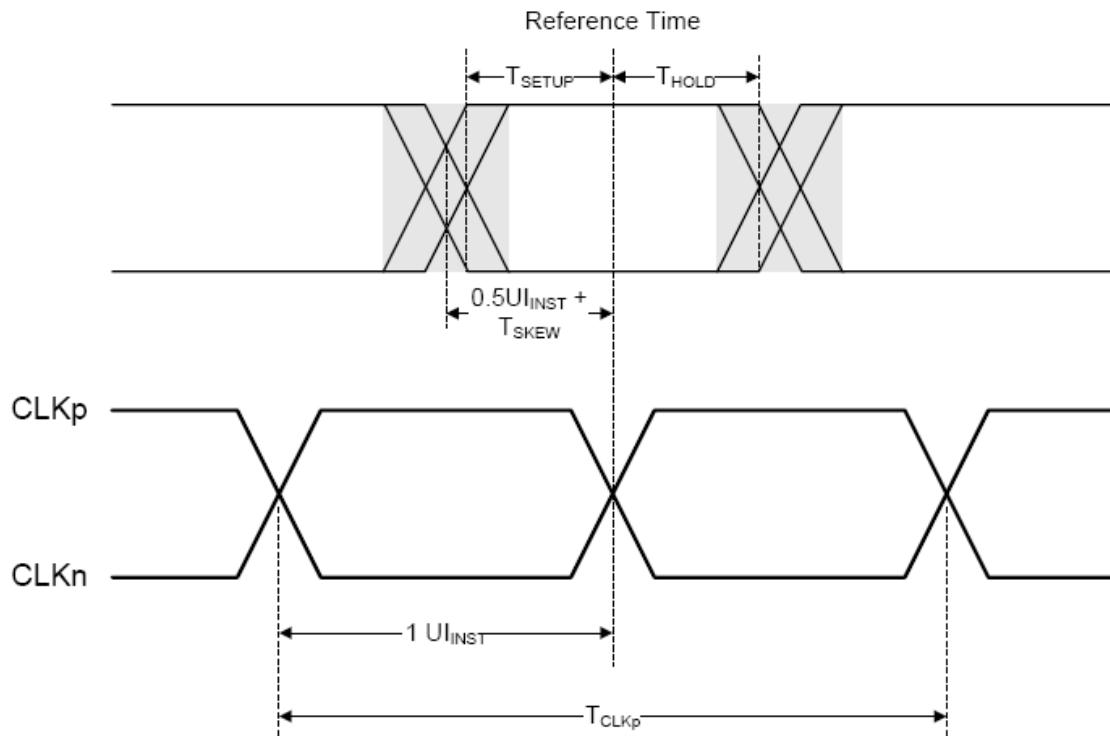
Figure 10-3   Data to clock timing reference

Table 10.10   Data-Clock timing specification

Parameter	Description	Min.	Typ.	Max.	Units	Notes
T_{SKEW}	Data to clock skew measured at the transmitter	-0.15	--	0.15	UI_{INST}	
T_{SETUP}	Data to clock setup time at receiver	0.15	--	--	UI_{INST}	
T_{HOLD}	clock to data hold time at receiver	0.15	--	--	UI_{INST}	
UI_{INST}	1 Data bit time (instantaneous)	--	--	12.5	ns	
T_{CLKp}	Period of dual data rate clock	2	2	2	UI_{INST}	

10.4.5. I²C Timings
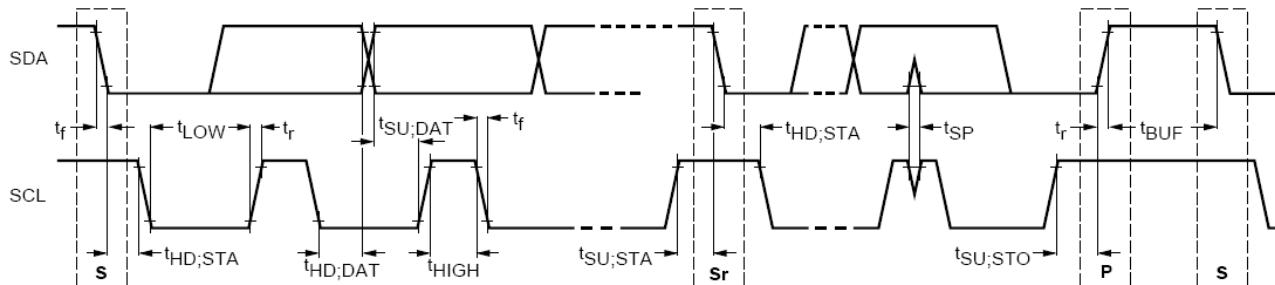
Figure 10-4   I²C Timing Diagram

Table 10.11   I²C timing specification

Item	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	--	µs
LOW period of the SCL clock	t_{LOW}	1.3	--	µs
HIGH period of the SCL clock	t_{HIGH}	0.6	--	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	--	µs
Data hold time: for I²C-bus devices	$t_{HD;DAT}$	0	0.9	µs
Data set-up time	$t_{SU;DAT}$	100	--	ns
Rise time of both SDA and SCL signals	t_r	20+0.1Cb	300	ns
Fall time of both SDA and SCL signals	t_f	20+0.1Cb	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	--	µs
Bus free time between a STOP and START condition	t_{BUF}	1.3	--	µs

Note: Cb = Capacitive load for each bus line (400 pF max.)

11. eDP bitrate and number of lane

Table 11.1   eDP bitrate and number of lane

| Common Video Mode Name | VESA Timing Name (Horizontal xVertical @ Frame Rate) | Pixel Clock Rate (MHz) | 18bpp | | | | 24bpp | | | |
| | | | Stream Bit Rate (Gbps) | Required Number of Main-Link Lanes | | | Stream Bit Rate (Gbps) | Required Number of Main-Link Lanes | | |
				1.62 Gbps/lane	2.7 Gbps/lane	5.4 Gbps/lane		1.62 Gbps/lane	2.7 Gbps/lane	5.4 Gbps/lane
XGA	1024x768 @ 60Hz CVT (Reduced Blanking)	56	1.01	1(P)	1	1	1.34	2	1(P)	1
WXGA	1280x768 @ 60Hz CVT (Reduced Blanking)	68.25	1.23	1(P)	1	1	1.64	2	1(P)	1
WXGA	1280x800 @ 60Hz CVT (Reduced Blanking)	71	1.28	1(P)	1	1	1.7	2	1(P)	1
HD	1366x768 @ 60Hz	85.5	1.54	2	1(P)	1	2.05	2	1(P)	1
WXGA+	1440x900 @ 60Hz CVT (Reduced Blanking)	88.75	1.6	2	1(P)	1	2.13	2	1(P)	1
SXGA+	1400x1050 @ 60Hz CVT (Reduced Blanking)	101	1.82	2	1(P)	1	2.42	2(P)	2	1
HD+	1600x900 @ 60Hz (Reduced Blanking)	108	1.94	2	1(P)	1	2.59	4	2(P)	1
WSXGA+	1680x1050 @ 60Hz CVT (Reduced Blanking)	119	2.12	2	1(P)	1	2.86	4	2(P)	1
UXGA	1600x1200 @ 60Hz CVT (Reduced Blanking)	130.25	2.34	2(P)	2	1	3.13	4	2(P)	1
FHD	1920x1080 @ 60Hz	148.5	2.67	4	2(P)	1	3.56	4	2(P)	1
WUXGA	1920x1200 @ 60Hz CVT (Reduced Blanking)	154	2.77	4	2(P)	1	3.7	4	2(P)	1
WQXGA	2560x1600 @ 60Hz CVT (Reduced Blanking)	268.5	4.83	4(P)	4	2	6.44	N/A	4	2
4K2K	4096x2160@60HZ CVT (Reduceed Blanking v2)	556.75	12.514	N/A	4	2	16.686	N/A	N/A	4
4K2K	3840x2160 @ 60Hz CVT (Reduced Blanking v2)	522.092	11.747	N/A	4	2	15.663	N/A	N/A	4

Notes : (P) denotes the preferred eDP Configuration, when not supporting the 5.4Gbps Main-Link rate.
Absolute maximum pixel rate is 600Mpixel/s.

Format Conversion

OUT / IN	RGB666 18bpp	RGB888 24bpp	RGB666 18bpp 1/2 compressed	RGB888 24bpp 1/2 compressed
RGB666 (18bpp)	OK[1]	OK	NG	OK
RGB888 (24bpp)	OK[2]	OK[1]	NG	OK

Notes:

1: No conversion

2:Dithering process available

12. Revision History

Table 12.1   Revision History

Revision	Date	Description
1.1	2014-09-29	Newly released
1.2	2014-10-30	Section9.1 corrected value of Absolute Maximum Ratings
1.3	12/03/2014	Section6. added Register description Added EXTCLK support 24MHz (from 24 to 40MHz) Corrected Table3-1 and Figure7-1 Modified Table4-1 and Figure4-2 (IRQ_HPD, INT)
1,4	12/10/2014	Corrected default value of some register in Table6-2
1.5	01/13/2014	Modified Table.4.1 Modified Figure1.1 , 1.2, 4.10 and Sec 4.3 (block digagram)
1.6	04/14/2014	modified typo and corrected "unit" description of value EXTCLK supported value changed :24,25,26 and 27MHz Table3-1 modified(Power supply column) Added Section9: Power consumption Remove 4.86, 2.43Gbps spec
1.7	07/15/2015	Modified typo EXTCLK supported value changed :24,25,26 and 27MHz
1.8	10/05/2015	Corrected power-off sequence timing chart -changed description of t3 parameter and Min and Max value.

RESTRICTIONS ON PRODUCT USE

- Toshiba Corporation, and its subsidiaries and affiliates (collectively "TOSHIBA"), reserve the right to make changes to the information in this document, and related hardware, software and systems (collectively "Product") without notice.

- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.

- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**

- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.

- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.

- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.

- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.

- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**

- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.

- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**