Schematic Review Form

Customer/Project

Pin #	Name	Info	Violations	*Description*
79,83,87,89,92	AGND	ok		Analog ground – Ground reference and current return for analog circuitry
82,84,88,95	AVdd	ok		Analog VDD – Power supply for analog circuitry. Nominally 3.3 V
42,41,40	CTL[3:1]	not sure where these go, but connection looks ok		General-purpose control signals – Used for user-defined control. CTL1 is not powered down via PDO
46	DE	ok		Output data enable – Used to indicate time of active video display versus non-active display or blank time. During blank, only HSYNC, VSYNC, and CTL[3:1] are transmitted. During times of active display, or non-blank, only pixel data, QE[23:0], and QO[23:0] are transmitted. High: Active display time Low: Blank time
1	DFO	pull up and pull down may be better so more flexible with multiple displays.		Output clock data format – Controls the output clock (ODCK) format for either TFT or DSTN panel support. For TFT support, the ODCK clock runs continuously. For DSTN support, ODCK only clocks when DE is high; otherwise, ODCK is held low when DE is low. High: DSTN support/ODCK held low when DE = low Low: TFT support/ODCK runs continuously

5,39,68	DGND	ok		Digital ground – Ground reference and current return for digital core
6,38,67	DVdd	ok		Digital VDD – Power supply for digital core. Nominally 3.3 V
96	EXT_RES	ok		Internal impedance matching – The TFP401/401A is internally optimized for impedance matching at 50 Ω. An external resistor tied to this pin has no effect on device performance.
48	HSYNC	ok		Horizontal sync output
99	RSVD	pdown or floating better		RSVD
OVdd	18,28,45,58,76	ok		Output driver ground – Ground reference and current return for digital output drivers
100	OCK_INV	ok		ODCK polarity – Selects ODCK edge on which pixel data (QE[23:0] and QO[23:0]) and control signals (HSYNC, VSYNC, DE, CTL[3:1]) are latched. Normal mode: High: Latches output data on rising ODCK edge Low: Latches output data on falling ODCK edge
2	~PD	ok		Power down – An active-low signal that controls the TFP401/401A power-down state. During power down, all output buffers are switched to a high-impedance

				state. All analog circuits are powered down and all inputs are disabled, except for PD. If PD is left unconnected, an internal pullup defaults the TFP401/401A to normal operation. High : Normal operation Low: Power down
9	~PDO	always on, ok		Output drive power down – An active-low signal that controls the power-down state of the output drivers. During output drive power down, the output drivers (except SCDT and CTL1) are driven to a high-impedance state. When PDO is left unconnected, an internal pullup defaults the TFP401/401A to normal operation. High: Normal operation/output drivers on Low: Output drive power down
98	PGND	ok		PLL GND – Ground reference and current return for internal PLL
4	PIXS	ok		Pixel select – Selects between one- and two-pixels-per-clock output modes. During the 2-pixel/clock mode, both even pixels, QE[23:0], and odd pixels, QO[23:0], are output in tandem on a given clock cycle. During 1-pixel/clock, even and odd pixels are output sequentially, one at a time, with the even pixel first, on the even pixel bus, QE[23:0]. (The first pixel per line is pixel-0, the even pixel. The second pixel per line is pixel-1, the odd pixel).

				High: 2-pixel/clock Low: 1-pixel/clock
97	PVdd	may need additional filtering for very clean PLL		PLL VDD – Power supply for internal PLL
20–27	QE[8:15]	ok		Even green-pixel output – Output for even and odd green pixels when in 1-pixel/clock mode. Output for even-only green pixel when in 2-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QE8/pin 20 MSB: QE15/pin 27
30–37	QE[16:23]	ok		Even red-pixel output – Output for even and odd red pixels when in 1-pixel/clock mode. Output for even-only red pixel when in 2-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QE16/pin 30 MSB: QE23/pin 37
49–56	QO[0:7]	NC		Odd blue-pixel output – Output for odd-only blue pixel when in 2-pixel/clock mode. Not used, and held low, when in 1-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QO0/pin 49 MSB: QO7/pin 56
59–66	QO[8:15]	NC		Odd green-pixel output – Output for odd-only green pixel when in 2-pixel/clock mode. Not used, and held low, when in 1-pixel/clock mode. Output data is synchronized to the output

				data clock, ODCK. LSB: QO8/pin 59 MSB: QO15/pin 66
69–75, 77	QO[16:23]	NC		Odd red-pixel output – Output for odd-only red pixel when in 2-pixel/clock mode. Not used, and held low, when in 1-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QO16/pin 69 MSB: QO23/pin 77
10–17	QE[0:7]	ok		Even blue-pixel output – Output for even and odd blue pixels when in 1-pixel/clock mode. Output for even-only blue pixel when in 2-pixel per clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QE0/pin 10 MSB: QE7/pin 17
93	RxC+	ok	see notes	Clock positive receiver input – Positive side of reference clock. TMDS low-voltage signal differential input pair
94	RxC–	ok	see notes	Clock negative receiver input – Negative side of reference clock. TMDS low-voltage signal differential input pair
90	Rx0+	ok	see notes	Channel-0 positive receiver input – Positive side of channel-0. TMDS low-voltage signal differential input pair. Channel-0 receives blue pixel data in active display and HSYNC, VSYNC control signals in blank.
91	Rx0–	ok	see notes	Channel-0 negative receiver input – Negative side of channel-0. TMDS low-voltage signal differential input pair

85	Rx1+	ok	see notes	Channel-1 positive receiver input – Positive side of channel-1 TMDS low-voltage signal differential input pair Channel-1 receives green-pixel data in active display and CTL1 control signals in blank.
86	Rx1–	ok	see notes	Channel-1 negative receiver input – Negative side of channel-1 TMDS low-voltage signal differential input pair
80	Rx2+	ok	see notes	Channel-2 positive receiver input – Positive side of channel-2 TMDS low-voltage signal differential input pair Channel-2 receives red-pixel data in active display and CTL2, CTL3 control signals in blank.
81	Rx2-	ok	see notes	I Channel-2 negative receiver input – Negative side of channel-2 TMDS low-voltage signal differential input pair
8	SCDT	ok		Sync detect - Output to signal when the link is active or inactive. The link is considered to be active when DE is actively switching. The TFP401/401A monitors the state of DE to determine link activity. SCDT can be tied externally to PDO to power down the output drivers when the link is inactive. High: Active link Low: Inactive link
3	ST	ok		Output drive strength select – Selects output drive strength for high- or low-current drive. (See dc specifications for IOH and IOL vs ST state).

				High: High drive strength Low: Low drive strength
7	~STAG	better to pup and pdown options for flexibility		Staggered pixel select – An active-low signal used in the 2-pixel/clock pixel mode (PIXS = high). Time-staggers the even and odd pixel outputs to reduce ground bounce. Normal operation outputs the odd and even pixels simultaneously. High: Normal simultaneous even/odd pixel output Low: Time-staggered even/odd pixel output
47	VSYNC	ok		Vertical sync output

Comments

Do you have any ESD circuitry/ CMC for EMI reductions at the output lanes?