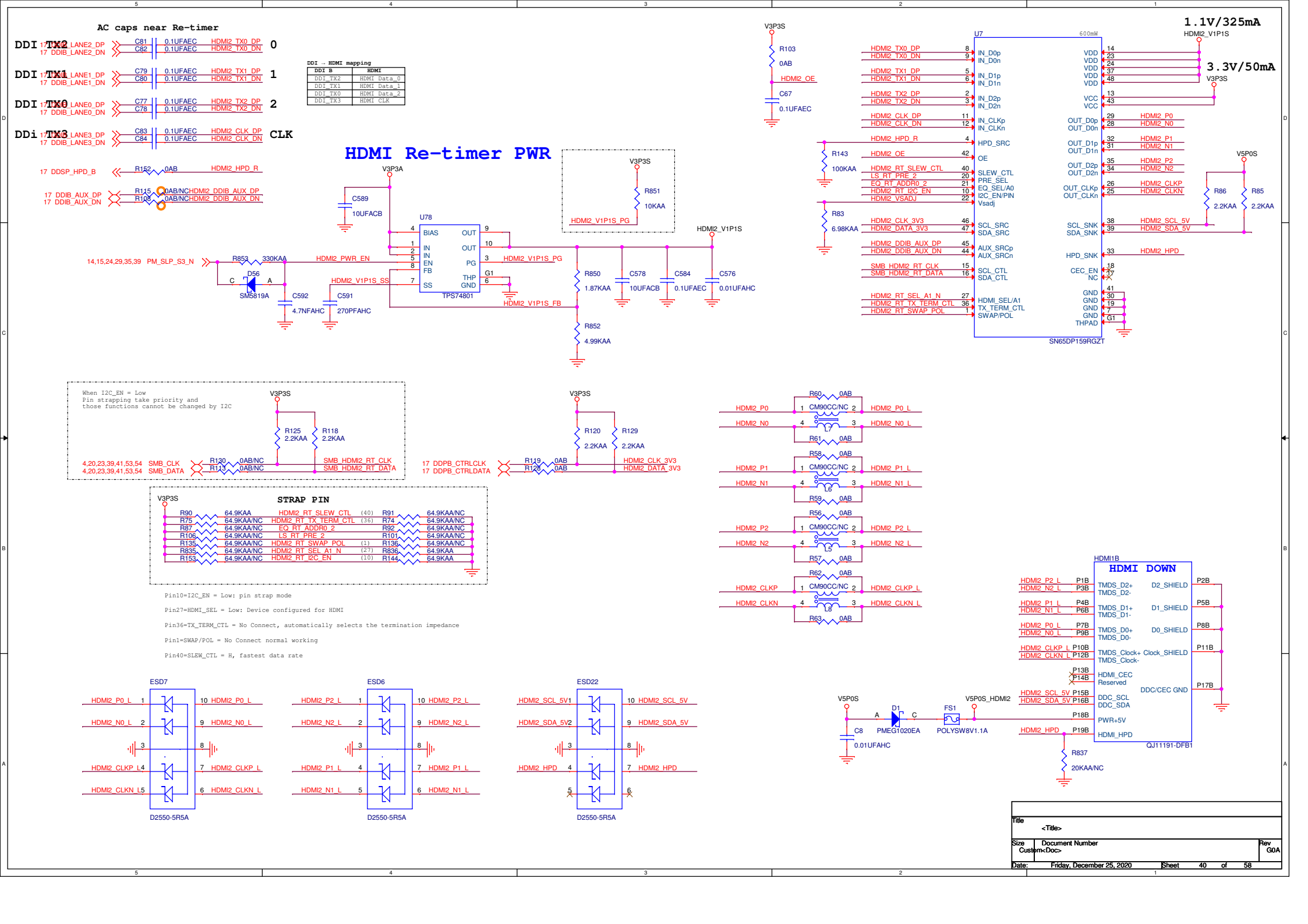
AC caps near Re-timer
DDI TX2
DDI TX1
DDI TX0
DDi TX3
C81 0.1UFAEC HDMI2_TX0_DP
C82 0.1UFAEC HDMI2_TX0_DN
C79 0.1UFAEC HDMI2_TX1_DP
C80 0.1UFAEC HDMI2_TX1_DN
C77 0.1UFAEC HDMI2_TX2_DP
C78 0.1UFAEC HDMI2_TX2_DN
C83 0.1UFAEC HDMI2_CLK_DP
C84 0.1UFAEC HDMI2_CLK_DN
0
1
2
CLK
DDI → HDMI mapping
DDI B | HDMI
DDI_TX2 | HDMI Data_0
DDI_TX1 | HDMI Data_1
DDI_TX0 | HDMI Data_2
DDI_TX3 | HDMI CLK
17 DDSP_HPD_B
R152 0AB HDMI2_HPD_R
17 DDIB_AUX_DP
17 DDIB_AUX_DN
R115 0AB/NC HDMI2_DDIB_AUX_DP
R108 0AB/NC HDMI2_DDIB_AUX_DN
HDMI Re-timer PWR
V3P3A
C589 10UFACB
U78
BIAS
IN
IN
EN
FB
SS
OUT
OUT
PG
THP
GND
TPS74801
14,15,24,29,35,39 PM_SLP_S3_N
R853 330KAA HDMI2_PWR_EN
D56 SM5819A
C592 4.7NFAHC
C591 270PFAHC
HDMI2_V1P1S_SS
HDMI2_V1P1S_FB
V3P3S
R851 10KAA
HDMI2_V1P1S_PG
HDMI2_V1P1S
R850 1.87KAA
C578 10UFACB
C584 0.1UFAEC
C576 0.01UFAHC
R852 4.99KAA
When I2C_EN = Low
Pin strapping take priority and
those functions cannot be changed by I2C
R125 2.2KAA
R118 2.2KAA
4,20,23,39,41,53,54 SMB_CLK
4,20,23,39,41,53,54 SMB_DATA
R130 0AB/NC
R113 0AB/NC
SMB_HDMI2_RT_CLK
SMB_HDMI2_RT_DATA
17 DDPB_CTRLCLK
17 DDPB_CTRLDATA
R119 0AB
R128 0AB
R120 2.2KAA
R129 2.2KAA
HDMI2_CLK_3V3
HDMI2_DATA_3V3
STRAP PIN
R90 64.9KAA HDMI2_RT_SLEW_CTL (40) R91 64.9KAA/NC
R75 64.9KAA/NC HDMI2_RT_TX_TERM_CTL (36) R74 64.9KAA/NC
R87 64.9KAA/NC EQ_RT_ADDR0_2 R92 64.9KAA/NC
R106 64.9KAA/NC LS_RT_PRE_2 R101 64.9KAA/NC
R135 64.9KAA/NC HDMI2_RT_SWAP_POL (1) R136 64.9KAA/NC
R835 64.9KAA/NC HDMI2_RT_SEL_A1_N (27) R836 64.9KAA
R153 64.9KAA/NC HDMI2_RT_I2C_EN (10) R144 64.9KAA
Pin10=I2C_EN = Low: pin strap mode
Pin27=HDMI_SEL = Low: Device configured for HDMI
Pin36=TX_TERM_CTL = No Connect, automatically selects the termination impedance
Pin1=SWAP/POL = No Connect normal working
Pin40=SLEW_CTL = H, fastest data rate
ESD7
ESD6
ESD22
HDMI2_P0_L
HDMI2_N0_L
HDMI2_CLKP_L
HDMI2_CLKN_L
HDMI2_P2_L
HDMI2_N2_L
HDMI2_P1_L
HDMI2_N1_L
HDMI2_SCL_5V1
HDMI2_SDA_5V2
HDMI2_HPD
D2550-5R5A
V3P3S
R103 0AB HDMI2_OE
C67 0.1UFAEC
1.1V/325mA
3.3V/50mA
HDMI2_V1P1S
U7
600mW
HDMI2_TX0_DP
HDMI2_TX0_DN
HDMI2_TX1_DP
HDMI2_TX1_DN
HDMI2_TX2_DP
HDMI2_TX2_DN
HDMI2_CLK_DP
HDMI2_CLK_DN
HDMI2_HPD_R
HDMI2_OE
HDMI2_RT_SLEW_CTL
LS_RT_PRE_2
EQ_RT_ADDR0_2
HDMI2_RT_I2C_EN
HDMI2_VSADJ
HDMI2_CLK_3V3
HDMI2_DATA_3V3
HDMI2_DDIB_AUX_DP
HDMI2_DDIB_AUX_DN
SMB_HDMI2_RT_CLK
SMB_HDMI2_RT_DATA
HDMI2_RT_SEL_A1_N
HDMI2_RT_TX_TERM_CTL
HDMI2_RT_SWAP_POL
IN_D0p
IN_D0n
IN_D1p
IN_D1n
IN_D2p
IN_D2n
IN_CLKp
IN_CLKn
HPD_SRC
OE
SLEW_CTL
PRE_SEL
EQ_SEL/A0
I2C_EN/PIN
Vsadj
SCL_SRC
SDA_SRC
AUX_SRCp
AUX_SRCn
SCL_CTL
SDA_CTL
HDMI_SEL/A1
TX_TERM_CTL
SWAP/POL
VDD
VCC
OUT_D0p
OUT_D0n
OUT_D1p
OUT_D1n
OUT_D2p
OUT_D2n
OUT_CLKp
OUT_CLKn
SCL_SNK
SDA_SNK
HPD_SNK
CEC_EN
NC
GND
THPAD
HDMI2_P0
HDMI2_N0
HDMI2_P1
HDMI2_N1
HDMI2_P2
HDMI2_N2
HDMI2_CLKP
HDMI2_CLKN
HDMI2_SCL_5V
HDMI2_SDA_5V
HDMI2_HPD
R143 100KAA
R83 6.98KAA
V5P0S
R86 2.2KAA
R85 2.2KAA
SN65DP159RGZT
R60 0AB
R61 0AB
R58 0AB
R59 0AB
R56 0AB
R57 0AB
R62 0AB
R63 0AB
CM90CC/NC
L7
L6
L5
L8
HDMI2_P0_L
HDMI2_N0_L
HDMI2_P1_L
HDMI2_N1_L
HDMI2_P2_L
HDMI2_N2_L
HDMI2_CLKP_L
HDMI2_CLKN_L
HDMI1B
HDMI DOWN
TMDS_D2+
TMDS_D2-
TMDS_D1+
TMDS_D1-
TMDS_D0+
TMDS_D0-
TMDS_Clock+
TMDS_Clock-
HDMI_CEC
Reserved
DDC_SCL
DDC_SDA
PWR+5V
HDMI_HPD
D2_SHIELD
D1_SHIELD
D0_SHIELD
Clock_SHIELD
DDC/CEC GND
P2B
P5B
P8B
P11B
P17B
QJ11191-DFB1
V5P0S_HDMI2
C8 0.01UFAHC
D1 PMEG1020EA
FS1 POLYSW8V1.1A
R837 20KAA/NC
Title
<Title>
Size Custom
Document Number <Doc>
Rev G0A
Date: Friday, December 25, 2020
Sheet 40 of 58