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TIDA-00429- "e-Fuse Power Switch with DevSleep SATA Interface"

1. System Introduction:

This reference design demonstrates DevSleep capability of TPS25940x eFuse from Texas Instruments.

The need to consume less power and provide extended battery life is a critical part for today's portable devices. DevSleep is a new state introduced in the SATA® specification, which requires SATA-based storage solutions to reach a level of low power operation. This is necessary to meet the aggressive power/battery life requirements of SATA-based mobile devices. DevSleep enables hosts and devices to completely hibernate the SATA interface. In this mode, power consumption of the device is limited to 5 mW or less for SSDs. Typically, device shall exit DevSleep mode in ≤ 20 ms.

TPS25940 provides a dedicated DevSleep interface terminal (DEVSLP) to force the device in low power mode. The DEVSLP pin is compatible with standard hardware signals asserted from the host controller. When pulled high, it puts the device in low power DevSleep mode. In this mode, the quiescent current consumption of the TPS25940 is limited to 95 μ A typical.

The interesting part of this design is that, during DevSleep mode, the output voltage remains active and overload current limit is set to (DEVSLP(LIM)), which is 0.67A (Typ). The functionality of reverse comparator and current monitoring is disabled in this mode. All other protections are still active and ensuring the safety of the system even in DevSleep mode.

2. System Operation and Test Set-Up

The TPS25940EVM is fully capable to demonstrate the DevSleep feature. EVM has two channels on the board for Autoretry and latched version of TPS25940 and both channels are capable for DevSleep Operation. This experiment is conducted on channel one, which is auto-retry version.

Refer to the schematic shown in figure 1, and test set up shown in figure 2. The test set-up needs external control signal (from function generator or microcontroller) to be applied at the DevSleep pin thru J6 connector with jumper in 1-2 location. Whenever DevSleep signal goes high the device is forced into sleep mode. The necessary waveforms of DevSleep operation are shown and discussed in test results section below.

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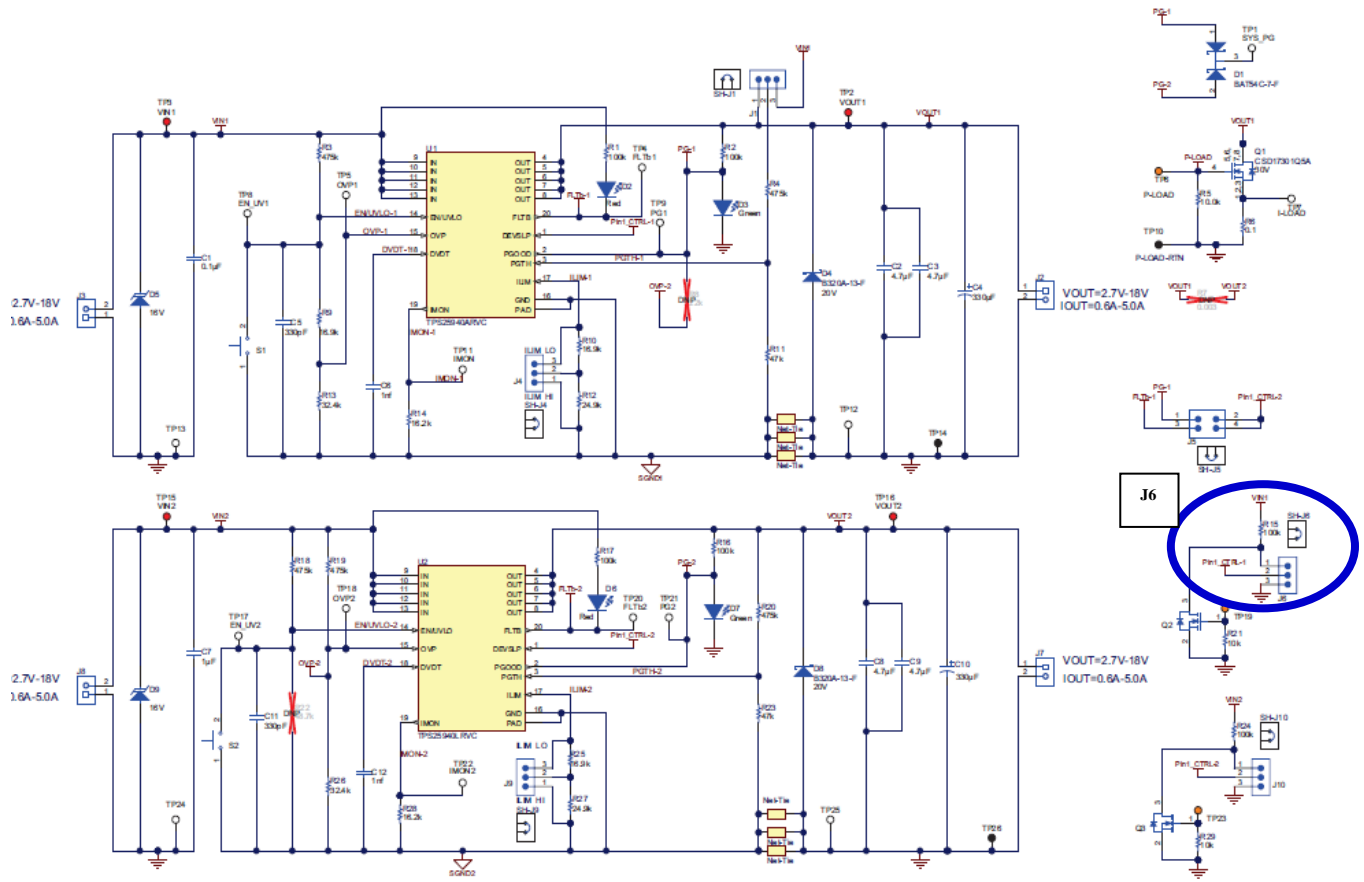


Figure 1: TPS25940EVM Schematic

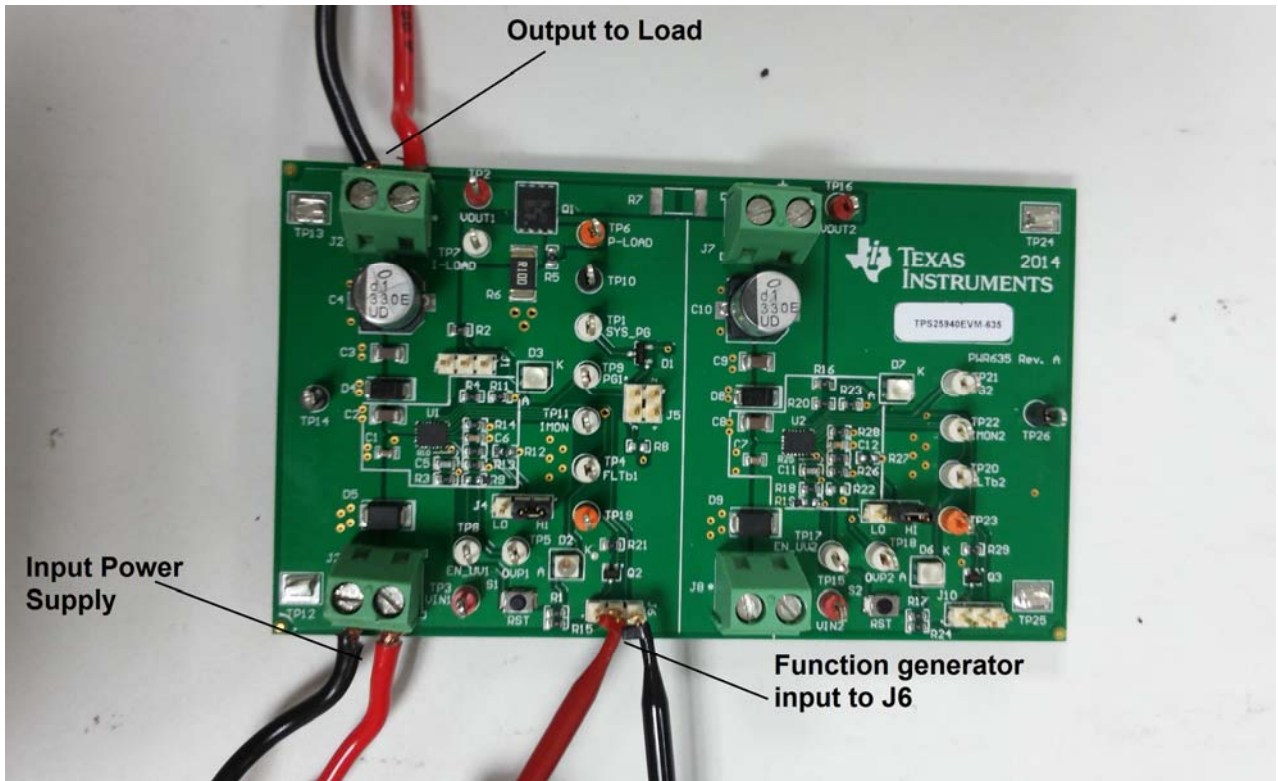


Figure 2: TPS25940EVM Test Set-up for DevSleep feature Demostartion

3. Test Results

Test setup for DevSleep Demostartion

- Vin from the Bench Power supply = 12V
- Output Voltage from TPS25940EVM = 12V
- TPS25940 EVM Current limit set by RILIM= 16.9KOhm (5.3A), J4 Jumper (1,2)
- Output Load Variation – 500mA to 850mA

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Scope label Information

- VIN- Input supply voltage to TPS25940 EVM.
- ILOAD – Load current
- VOUT – Load voltage
- DEV_SLP – External Enable/disable signal on DevSleep pin (DEVSLP).
- IMON- Load current monitoring

Test Result 1:

When the load current from the device is lower than the DevSleepILIM (670mA typical), the high or low signal on DEVSLP pin has no impact on the load current and the device operation is as shown on figure 3.

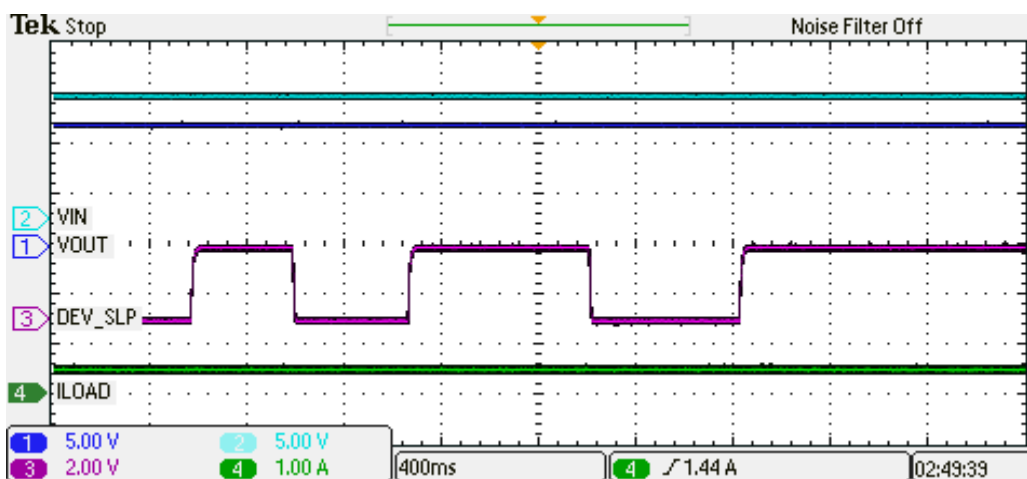


Figure 3: Vin=12V, Iload=500mA (<680mA), enabling DevSleep mode has no impact on load current

Test Result 2:

When the load current from the device is increase to the higher value than the DevSleepLIM (670mA typical), Enabling of devSleep bring down the load current to DeVSleep Limit as shown on figure 5.

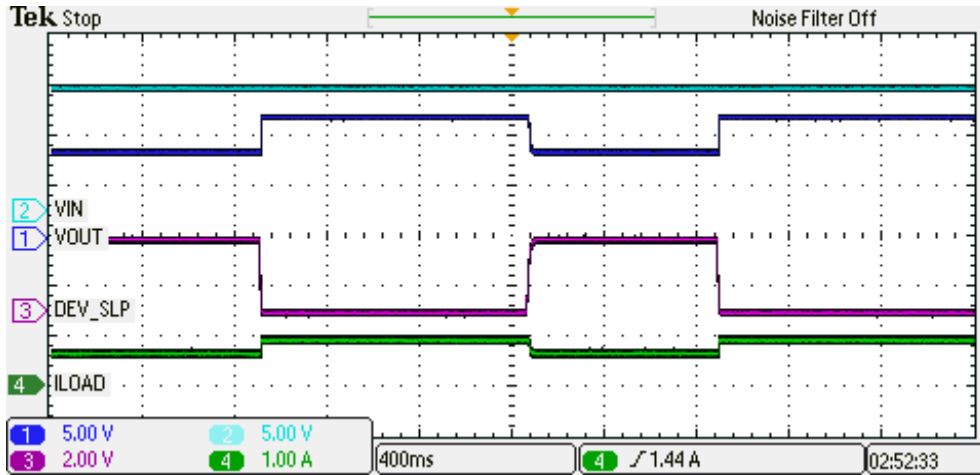


Figure 4: Vin=12V, Iload=850mA(>680mA), enabling DevSleep mode reduces the load current(Iload) to DevSleep LIM

Test Result 3:

Figure 6 shows, IMON feature gets disbled when DevSleep mode is enabled.

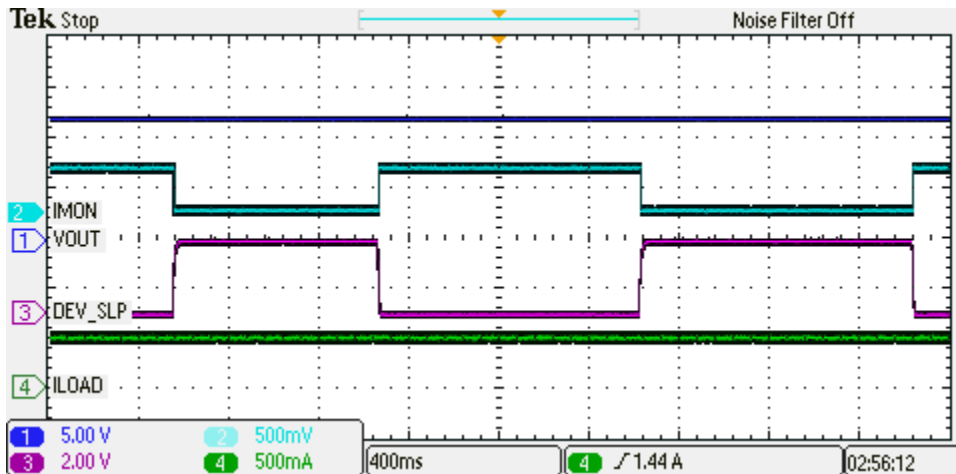


Figure 5: IMON feature is disabled, when Devsleep Mode is enable

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Test Result 4:

This case demonstrate the time device takes to enabling the IMON when DevSleep Mode is disabled.

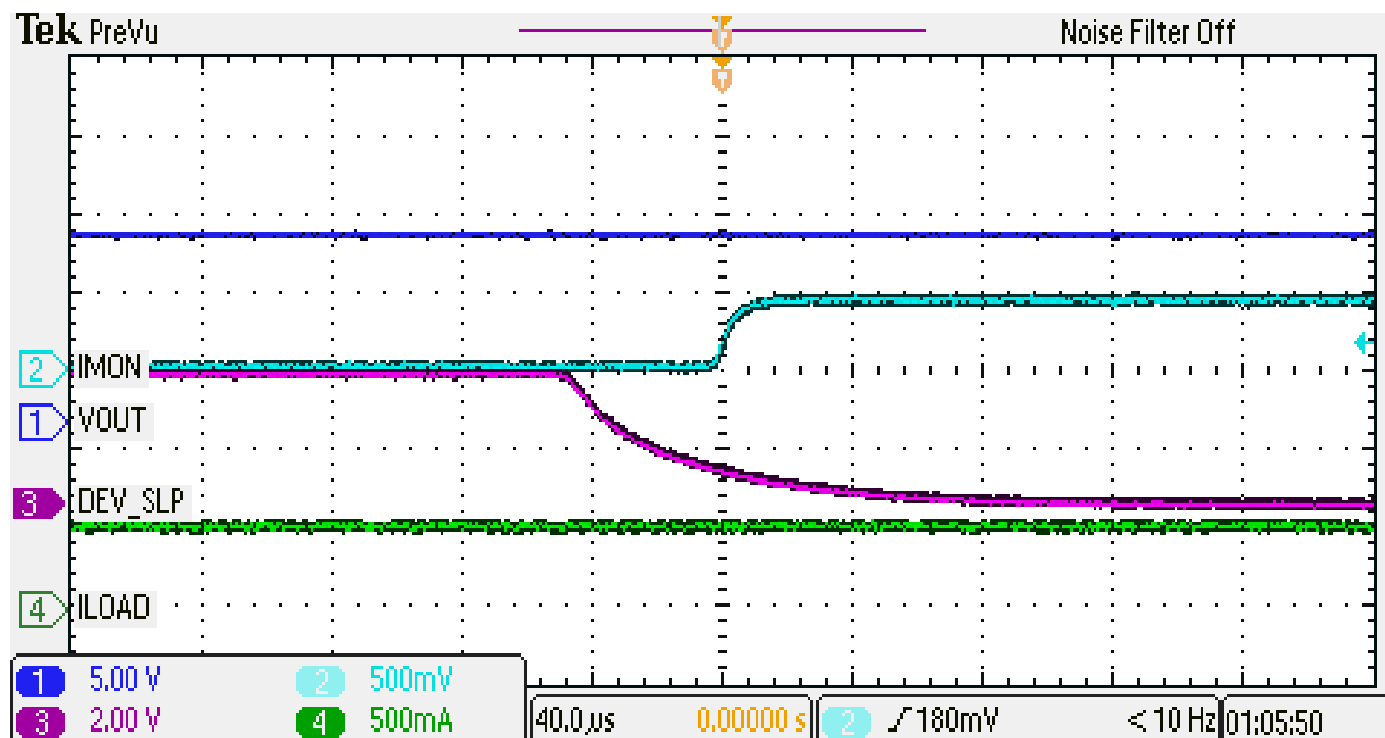


Figure 6 : Showing IMON enabling time after disabling DevSleep

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