DS90Ux940N Deserializer with Bug Fixes for CSI Issues

Ethernet and FPD-Link

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Background

- TI has become aware that the DS90Ux940-Q1 device can have failures on the CSI interface.
- Root causes of the issues have been identified.
- TI has implemented metal fix to resolve the above mentioned CSI and other issues.
- Per request from several customers, TI will release the updated device under a new part number: DS90Ux940**N**-Q1.
- DS90Ux940N-Q1 is pin-pin compatible with DS90Ux940-Q1, with the same underlying functionality.
- TI recommends transitioning to the updated 940N-Q1 device for new programs, as well as current production programs, as appropriate.

Summary of issues & corrective actions on DS90Ux940N

#	Bug Description	Details	Depth of changes	Validation Status
1	Error re-loading of trimmed registers	Trimmed registers get re-loaded with soft RESET (a reset, which is not supposed clear trim registers) is set - this is unexpected behavior	Soft reset is disabled from resetting the state machine for loading trim / indirect registers. Changes include wiring changes for reset signals to flops and a minor change to state machine requiring use of spare logic gates.	Verification and Validation results confirm that issues are fixed with the design changes
2	Corruption of CSI indirect registers	CSI Indirect registers can get corrupted during Digital RESET (soft). Internal configuration state causes garbage value (from write data) to be latched into indirect registers (CSI_IA) during RESET - this is unexpected behavior		
3	CSI Data lane getting out of phase	Releasing the clock divider from reset occurs as the PLL is starting up. The PLL clock output may be unstable and have improper timing and poor signal levels. The result on a single divider circuit would be negligible as the divider will always resolve to proper counting sequence once the clock is stable. Since the clock feeds two independent circuits, there is the possibility that the initial clock signal could affect the two dividers differently, such that they see different numbers of clock edges as the clock is starting up. Due to this, there is the potential that the two divider circuits may become out of proper phase alignment by the time the clock stabilizes.	Clock divider reset is released after PLL is locked, ensuring proper alignment. The change involves wiring changes only.	
4	CSI Initial state error (LP00 instead of LP11)	During the power-up, the initial state of LP is expected to be '11' (Stop) instead of '00‘. While not a violation of the D-PHY specification, it is preferable to enter the Stop state as soon as possible.	Changed the power-up state of flops to '11' instead of '00‘. Uses a few spare logic gates.	
5	Device Incorrectly enter AV_MUTE state	For HDCP operation, the device looks for control codes for AV Mute and Encryption enable/disable. When not in HDCP EESS mode, the device should not look for the commands. If the 940 sees a data value of 0x66_66_66 at the start of vertical sync, it will enter AV Mute state and not recover.	AV Mute is qualified with the HDCP mode information. Very minor changes with couple of connections using spare logic gates.	

AEC-Q completed with no failures : Only ESD and Latch-up was required to be redone

DS90Ux940N Implementation plan

- DS90U**H**940N-Q1 has been released to market on **October 30th, 2018**.

- DS90U**B**940N-Q1 is planned to release to market by March 08, 2019.

- Now that UH940N-Q1 has been released, the UH940-Q1 device will move to NRND (Not Recommended for New Designs) status.
  - Once a device is moved to NRND status, TI does not recommend using that device for new programs
  - This is **not** the same as EOL; customer may continue to purchase device in NRND status
    - Device is sold 'As-Is'
    - Known issues may be documented in errata or equivalent, with no plan for resolution
    - Recommended path forward may be to transition to alternate part (940N-Q1 in this case)

- After UB940N-Q1 is released, the UB940-Q1 device will also move to NRND (Not Recommended for New Designs) status.

FAQ

- **What are the silicon changes between DS90Ux940N and DS90Ux940?**
  - Metal-level routing and ECO changes to address the CSI and other issues as noted in slide#3
  - Number of layers affected: 6 Metal Layers
  - Percentage of net changed/affected: 0.8% of digital nets
  - Percentage of routing changed/affected: 2% to 3% of digital routing
- **What are the datasheet changes between DS90Ux940N and DS90Ux940?**
  - Updated to current TI requirements
  - Content added to clarify features and usage
  - Some spec parameter updates
- **Should software workarounds implemented for the Ux940-Q1 CSI Issue#2 & Issue#3 be removed?**
  - Software workarounds (see Appendix) implemented on Ux940-Q1 can be used on the Ux940N-Q1 with no side effects
  - Issue#2: Setting indirect address register pointer to unused location and waiting 500us after reset has no consequence on Ux940N
  - Issue#3: Toggling lock at startup only resets the CSI lock and since issue is fixed, step B will not be executed
- **Should software workaround for serializer-side AV Mute issue (Issue#5) be removed?**
  - Software workaround (see Appendix) implemented on serializer can be used for systems using Ux940N-Q1 with no side effects
- **Are there other software workarounds required for the Ux940N-Q1?**
  - After issuing a DIGITAL RESET0 (0x01[1] = 1), wait ≥500us before accessing any DS90Ux940N registers via I2C
  - Please see the Adaptive Equalizer section in datasheet for usage recommendations

Appendix: DS90Ux940 Software Workarounds

- **Issue#2**
  - **Step A:** Before issuing a DIGITAL RESET1 (0x01[0]=1) or DIGITAL RESET0 (0x01[1] = 1), set the CSI Indirect Address (CSIIA) register (address 0x6C) to point to an unused register location (by setting CSIIA register 0x6C=0xFF)
  - **Step B:** After issuing a DIGITAL RESET1 (0x01[0]=1) or DIGITAL RESET0 (0x01[1] = 1), wait ≥500us before accessing any DS90UH940 registers via I2C
- **Issue#3**
  - **Step A:** To reduce likelihood of SOT/data errors, implement the following software workaround once the CSI Pass condition from the DS90Ux940 is detected at startup
    - Force Lock Indication Low by setting register 0x40 = 0x4B
    - Release the forced Lock status by setting register 0x40 = 0x43
      - Above steps results in restart of CSI PLL logic
    - Wait for re-assertion of the CSI Pass indication
  - **Step B:** To recover from SOT/data errors after initialization, the system should monitor the CSI interface for SOT/data errors prior to capturing/displaying video data. If SOT/data errors exist, repeat the workaround mentioned in Step A until proper CSI SOT is detected.
- **Issue#5 (this is serializer-side configuration)**
  - Set DE_GATE_RGB register bit (0x04[4] = “1”) to prevent video from being sent during the blanking interval
  - If DE is active low, also set DE_POLARITY register bit 0x12 bit[5] = 1