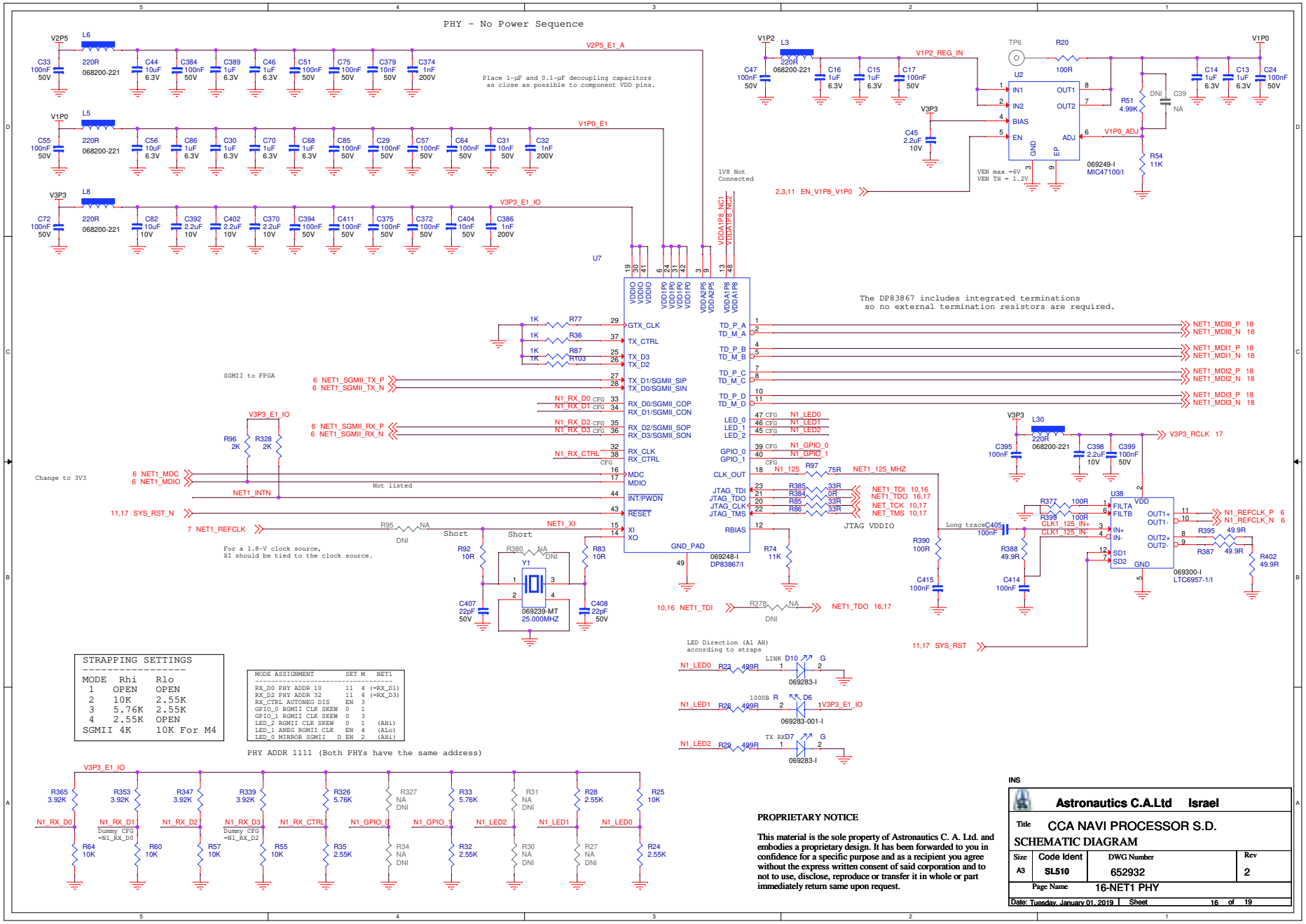
PHY - No Power Sequence
Place 1-µF and 0.1-µF decoupling capacitors as close as possible to component VDD pins.
The DP83867 includes integrated terminations so no external termination resistors are required.
SGMII to FPGA
Change to 3V3
Not listed
Short
For a 1.8-V clock source, XI should be tied to the clock source.
JTAG VDDIO
LED Direction (Al AH) according to straps
069248-I DP83867/I
069249-I MIC47100/I
069300-I LTC6957-1/I
069239-MT 25.000MHZ
069283-I
069283-001-I
STRAPPING SETTINGS
MODE Rhi Rlo
1 OPEN OPEN
2 10K 2.55K
3 5.76K 2.55K
4 2.55K OPEN
SGMII 4K 10K For M4
MODE ASSIGNMENT SET M NET1
RX_D0 PHY ADDR 10 11 4 (=RX_D1)
RX_D2 PHY ADDR 32 11 4 (=RX_D3)
RX_CTRL AUTONEG DIS EN 3
GPIO_0 RGMII CLK SKEW 0 1
GPIO_1 RGMII CLK SKEW 0 3
LED_2 RGMII CLK SKEW 0 1 (AHi)
LED_1 ANEG RGMII CLK EN 4 (ALo)
LED_0 MIRROR SGMII D EN 2 (AHi)
PHY ADDR 1111 (Both PHYs have the same address)
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INS
Astronautics C.A.Ltd Israel
Title CCA NAVI PROCESSOR S.D.
SCHEMATIC DIAGRAM
Size A3
Code Ident SL510
DWG Number 652932
Rev 2
Page Name 16-NET1 PHY
Date: Tuesday, January 01, 2019 Sheet 16 of 19