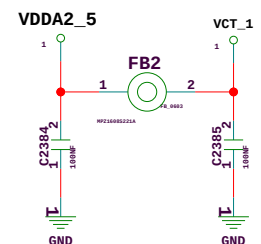
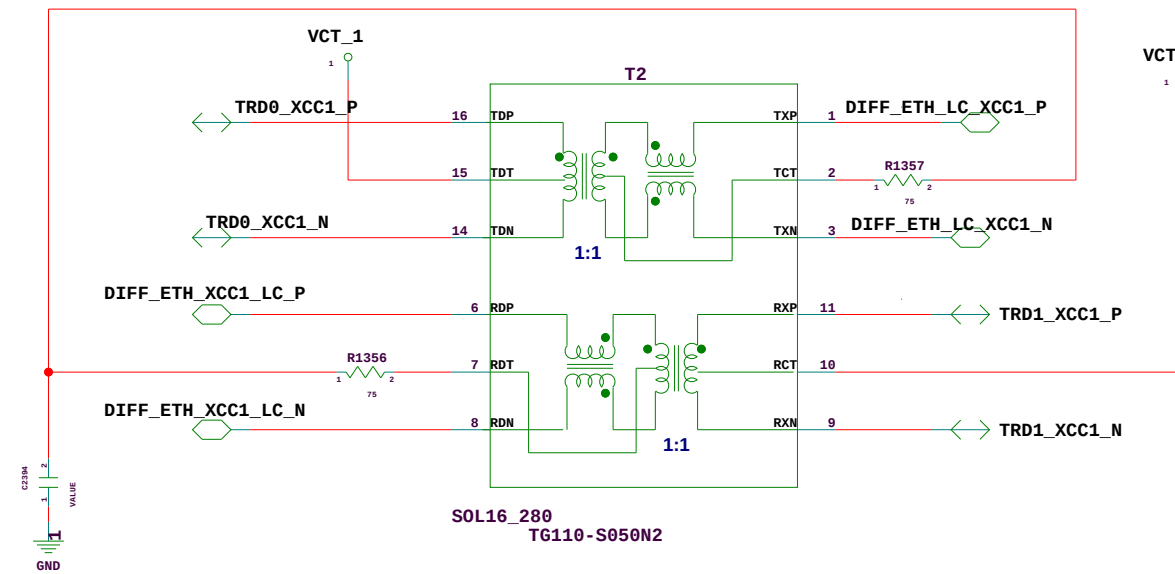
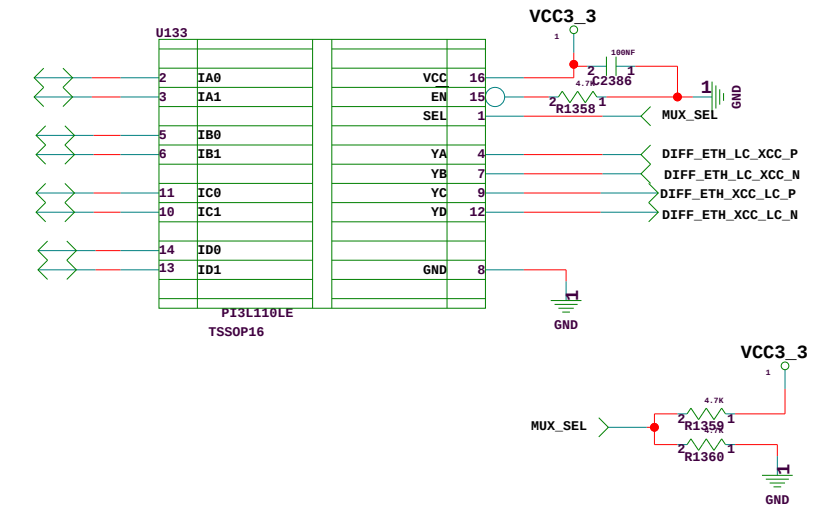
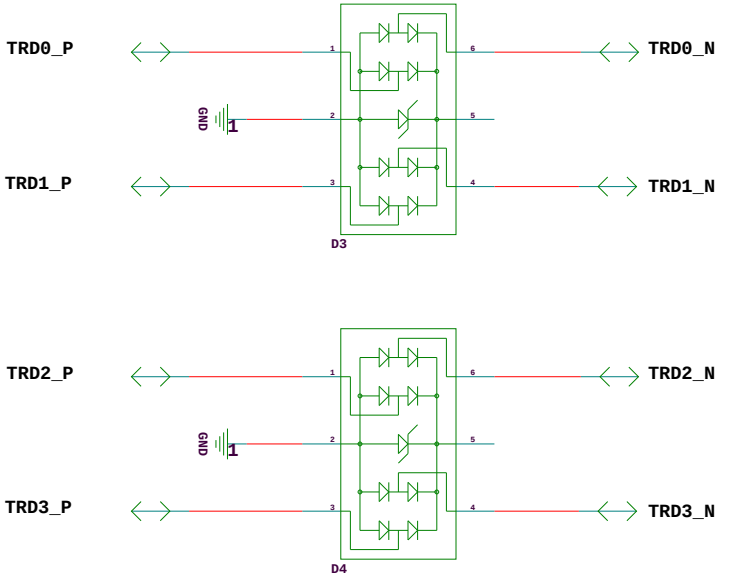
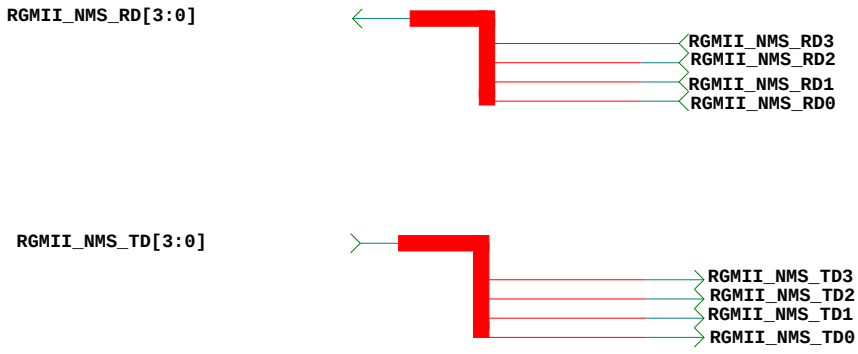
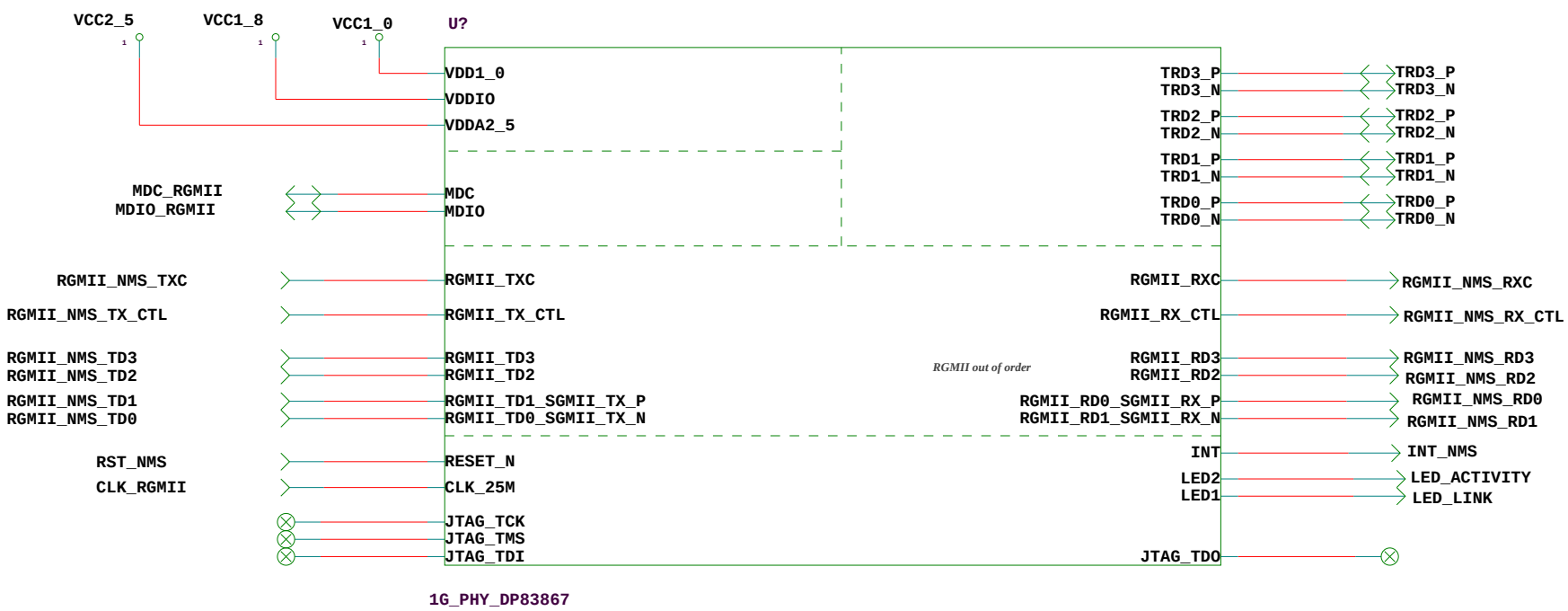


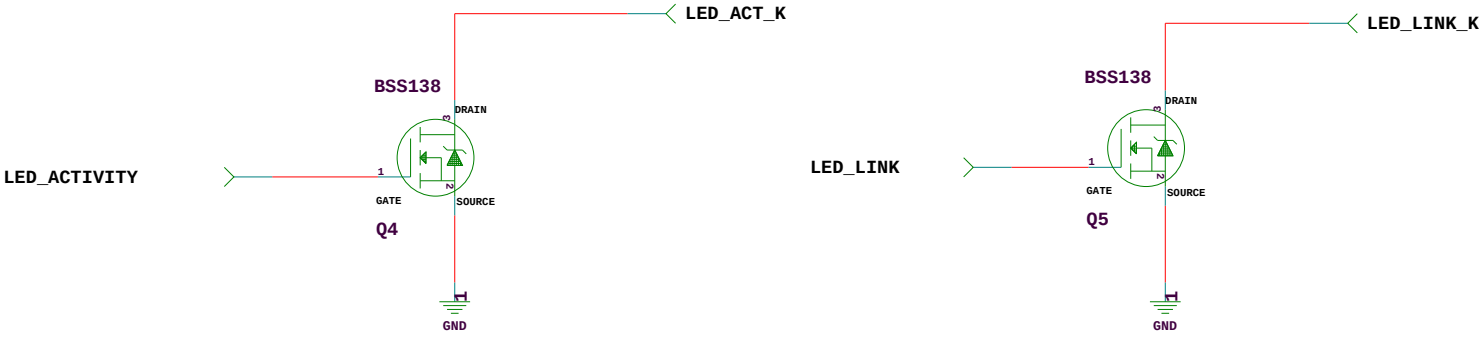
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1G RGMII PHY

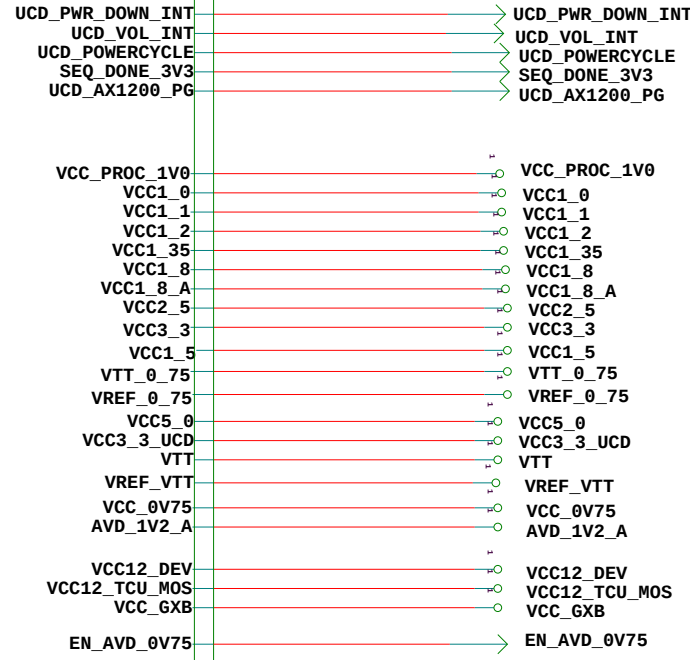
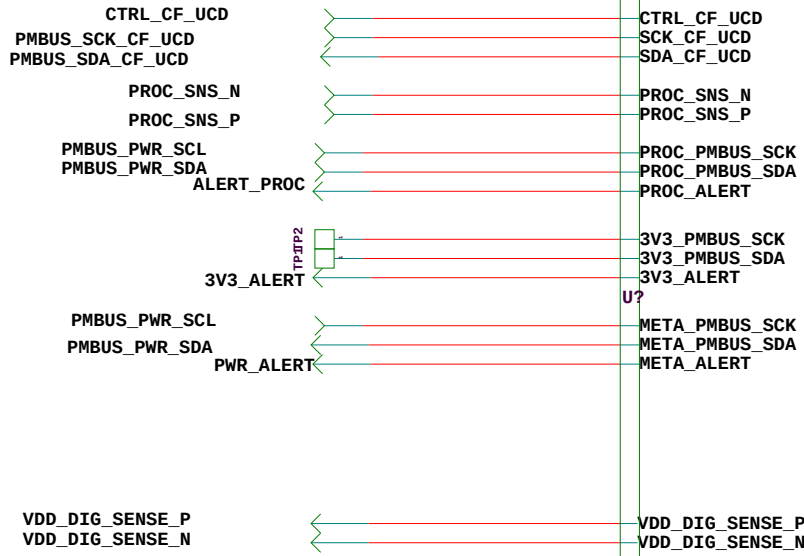


Layout Note: Place the TVS array near the RJ45



Description:		Tejas Networks	
DESCRIPTION		Sheet 2 of 25	
Project:	LINE36	Drawn By:	KEVIN
Date:	6-24-2024_12:02	Rev:	REV
		Reviewed By:	DHIRAJ
PART NUMBER:		PART_NUMBER	

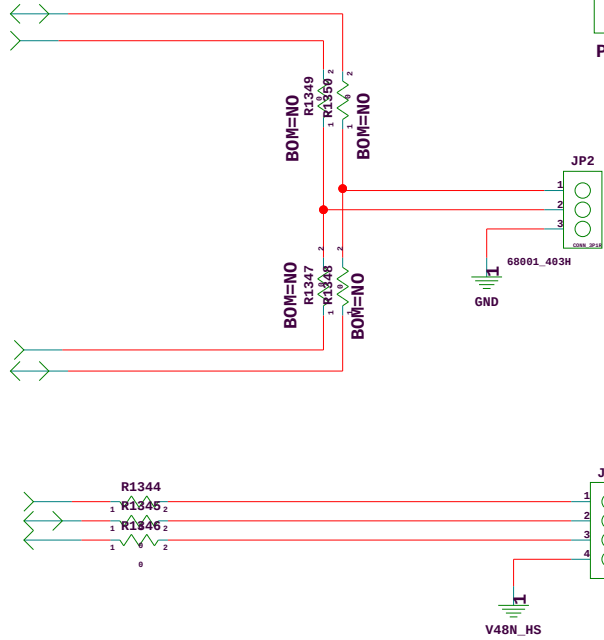
POWER TOP



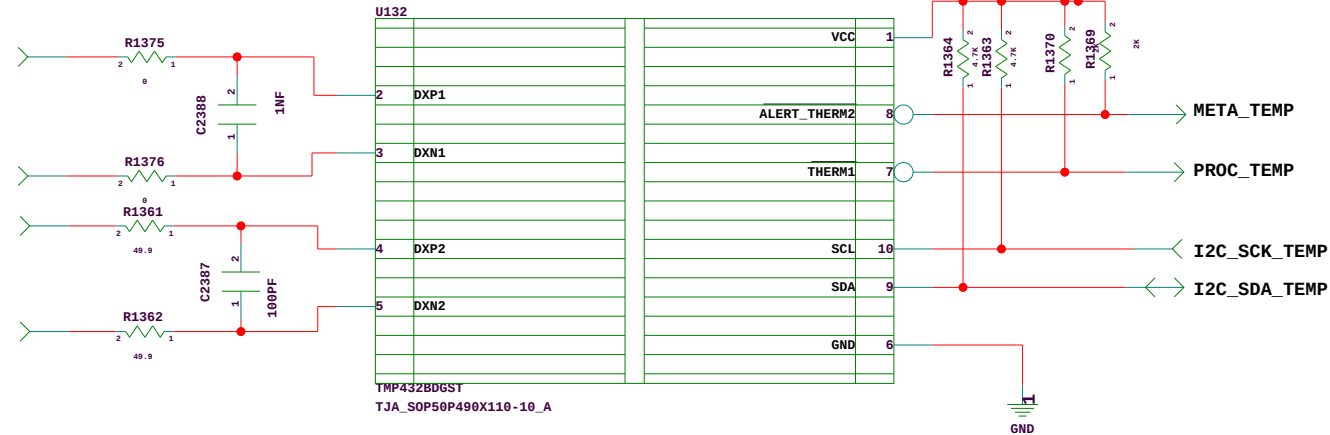
I2C_DATA_TPLL
I2C_CLK_TPLL

RC31012_SCL_3V3_CGEN
RC31012_SDA_3V3_CGEN

ALERT_HSO_ISO
SDA_HSO_ISO
SCK_HSO_ISO



PROC_THERM_P
PROC_THERM_N
META_THERM_P
META_THERM_N



Description:

DESCRIPTION

Tejas Networks

Sheet 3 of 25

Project: LINE36

Drawn By: KEVIN

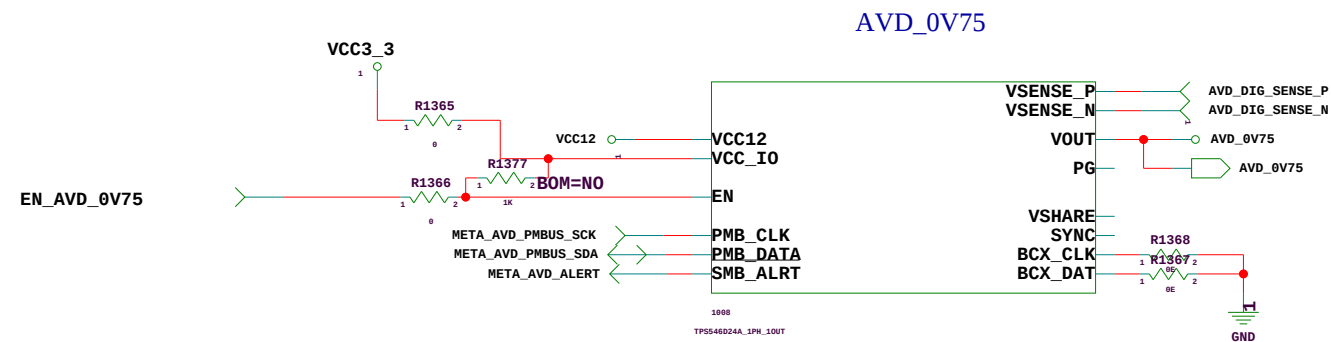
Date: 6-24-2024_12:00

Rev: REV

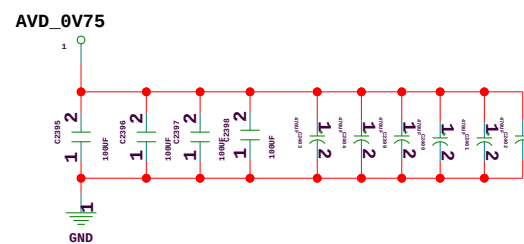
Reviewed By: DHIRAJ

PART NUMBER:

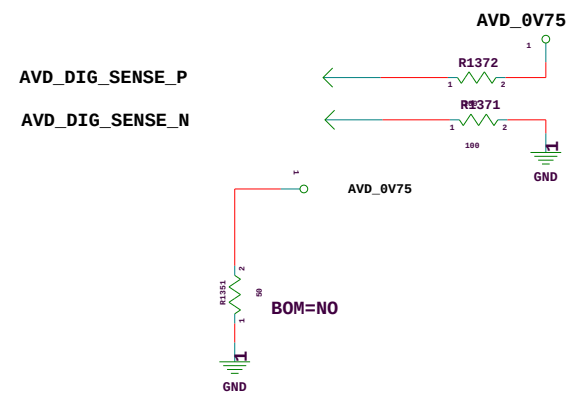
PART_NUMBER



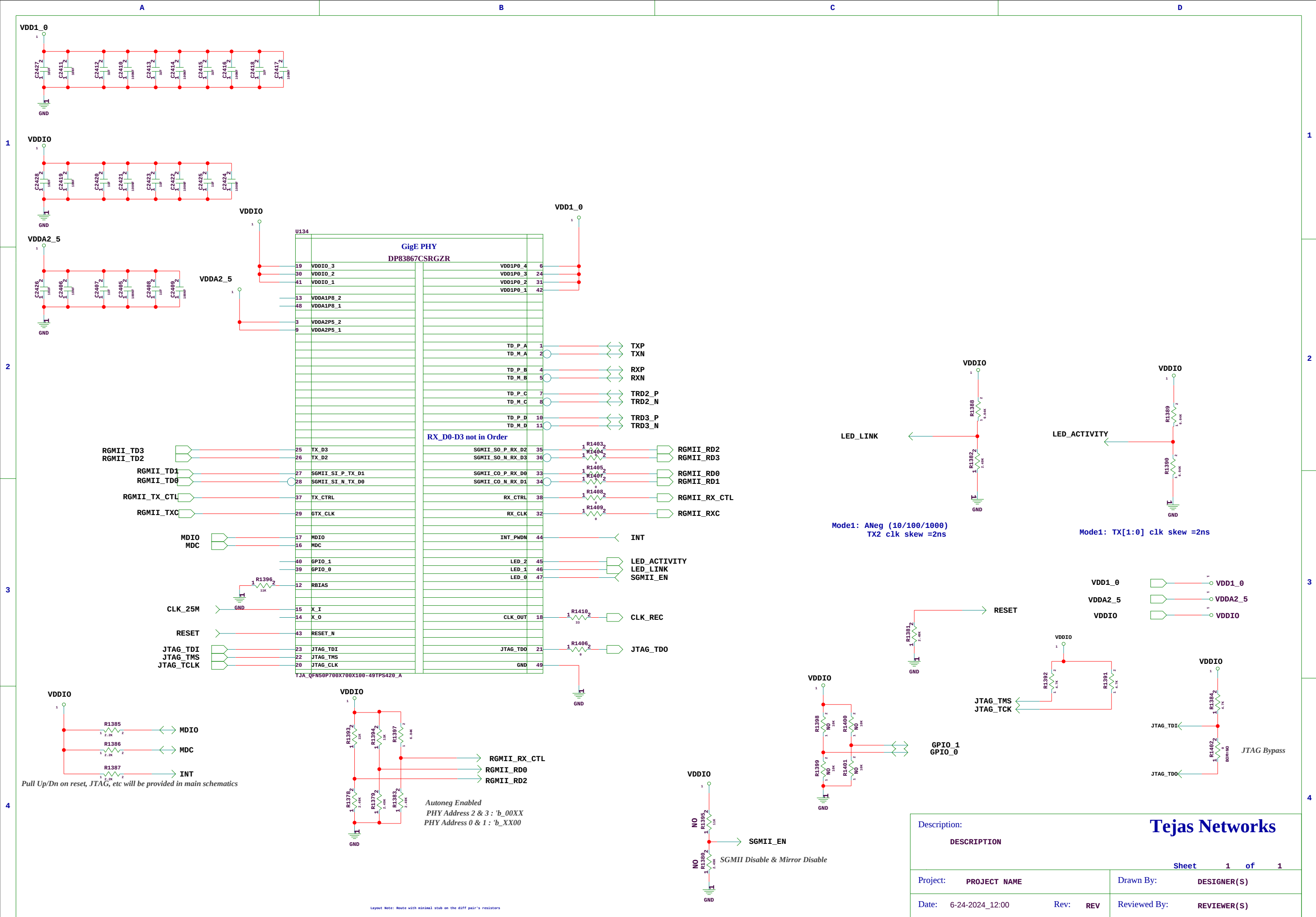
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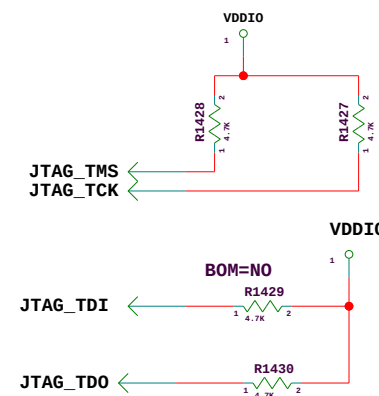
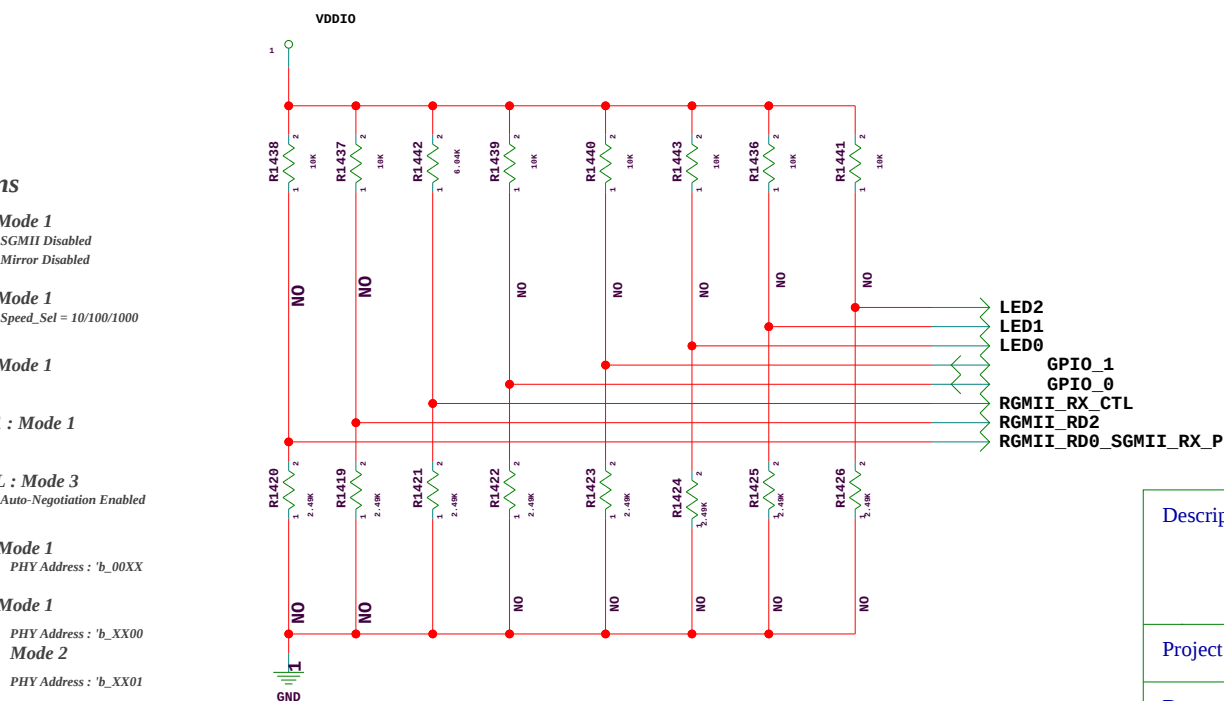
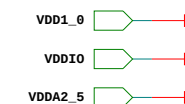
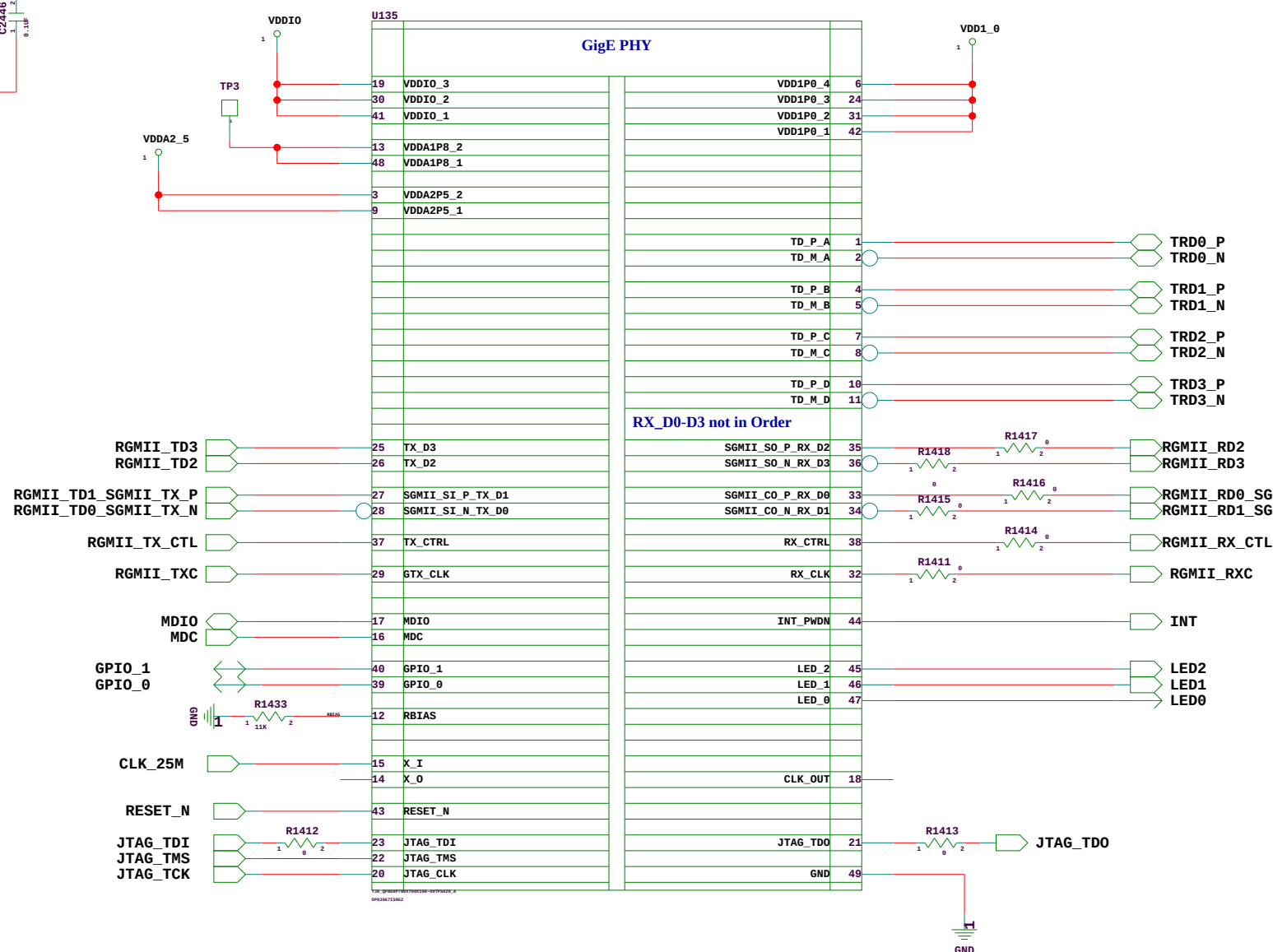
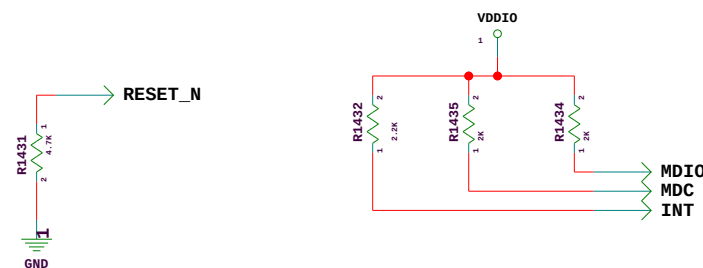
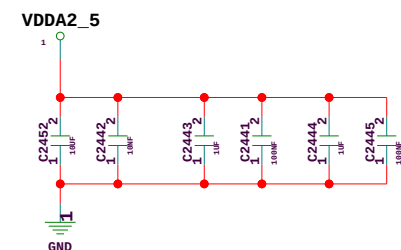
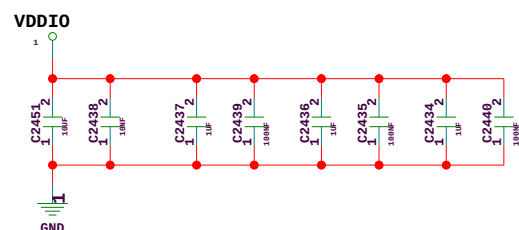
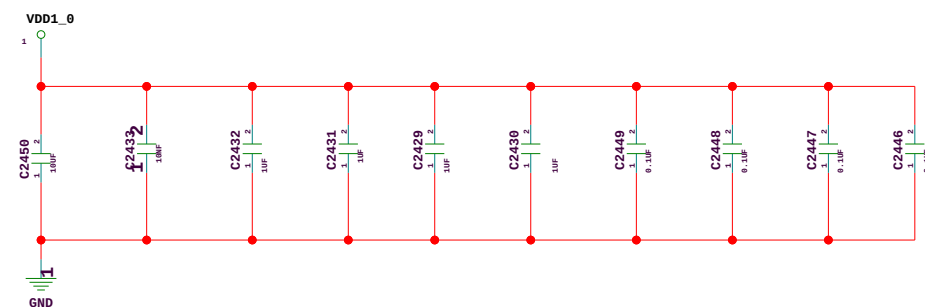


Place all the caps near U1



Description:		Tejas Networks	
DESCRIPTION		Sheet 4 of 25	
Project:	PROJECT NAME	Drawn By:	DESIGNER(S)
Date:	6-24-2024_12:00	Rev:	REV
		Reviewed By:	REVIEWER(S)
	PART NUMBER:	PART_NUMBER	





Strap Pins

LED_0 : Mode 1
SGMII Disabled
Mirror Disabled

LED_1 : Mode 1
Speed_Sel = 10/100/1000

LED_2 : Mode 1

GPIO_0/1 : Mode 1

RX_CTRL : Mode 3
Auto-Negotiation Enabled

RX_D2 : Mode 1
PHY Address : 'b_00XX

RX_D0 : Mode 1
PHY Address : 'b_XX00
Mode 2
PHY Address : 'b_XX01

Description:

DESCRIPTION

Tejas Networks

Sheet 1 of 1

Project: PROJECT NAME

Drawn By: **DESIGNER(S)**

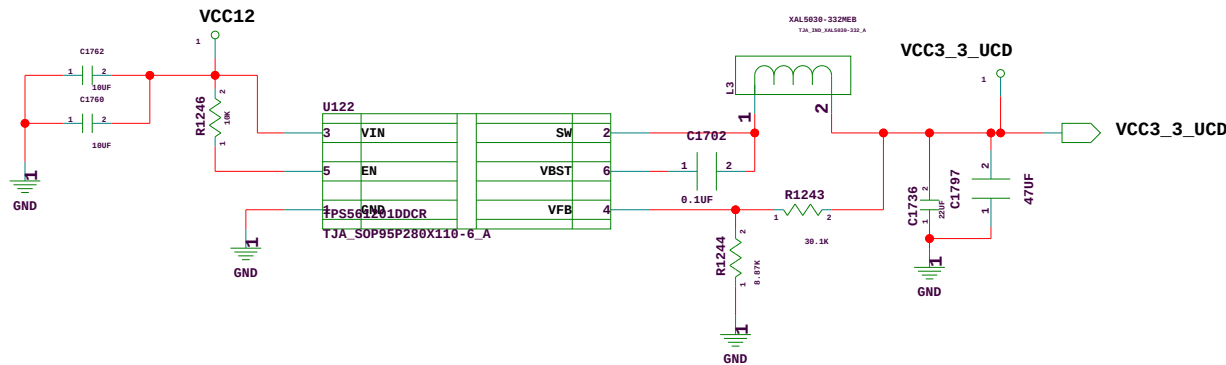
Date: 6-24-2024_12:00

Rev: REV

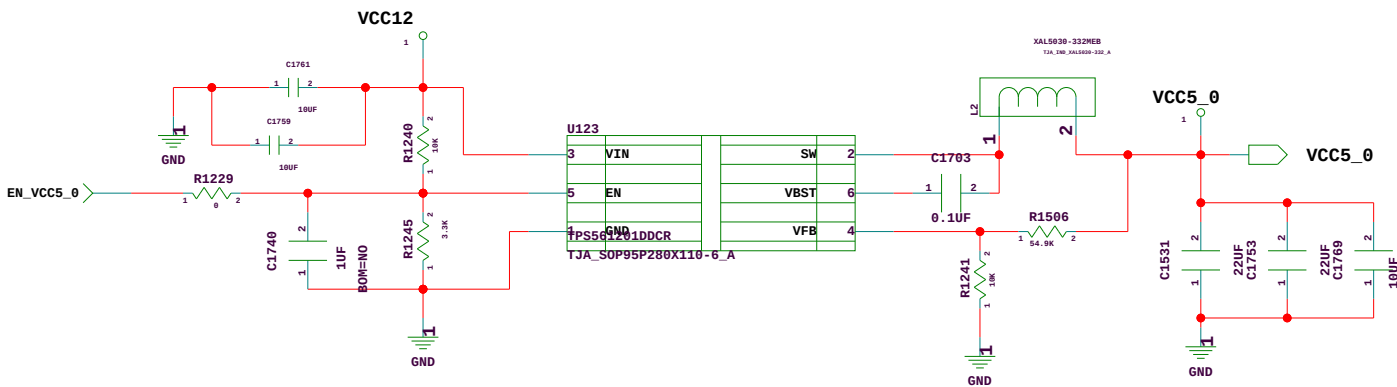
Reviewed By: REVIEWER(S)

PART NUMBER:

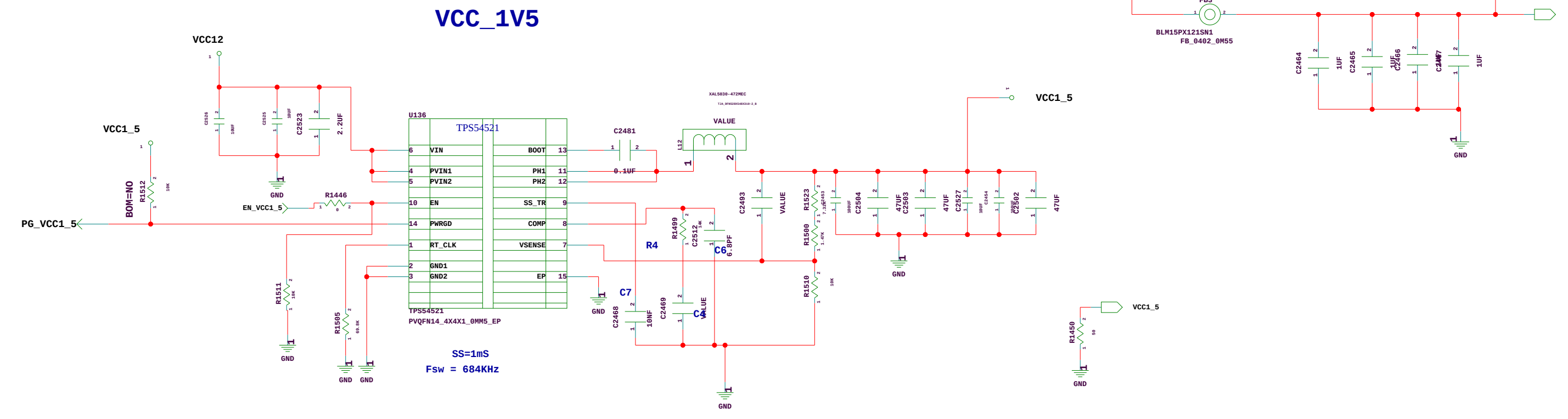
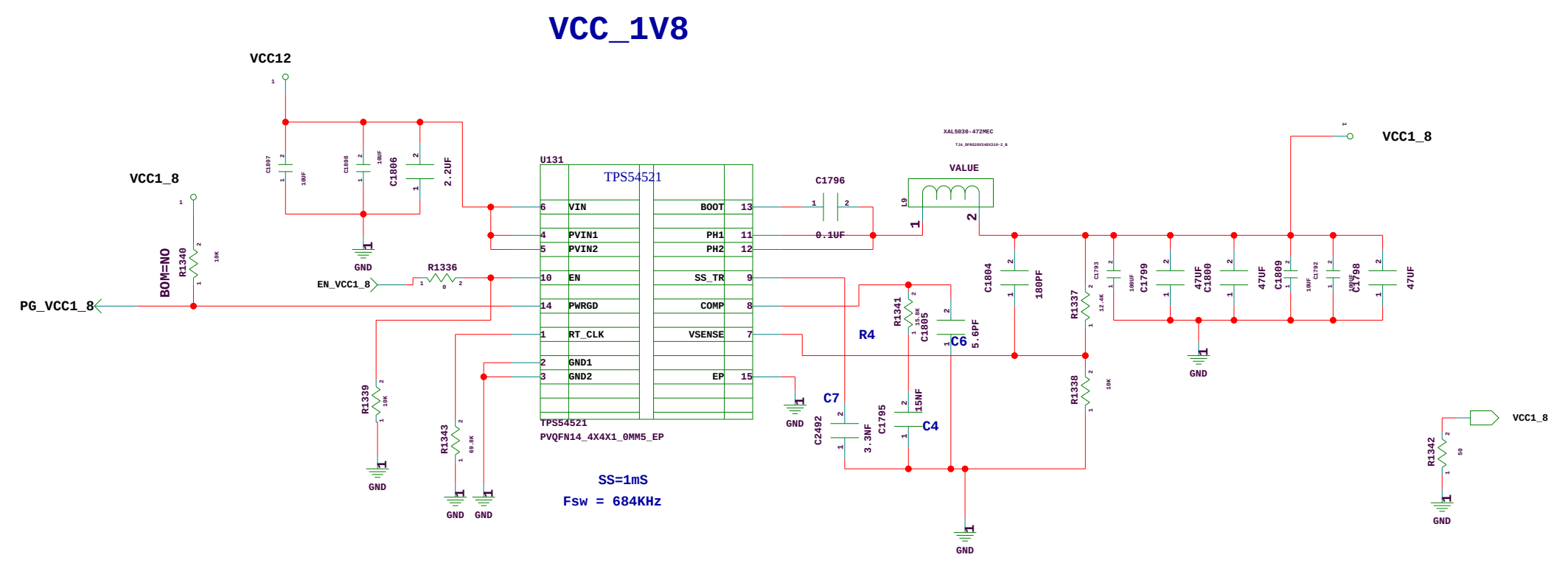
VCC_UCD



VCC_USB



Description:		Tejas Networks	
DESCRIPTION		Sheet 1 of 10	
Project:	LINE36	Drawn By:	KEVIN/MANI
Date:	6-24-2024_12:00	Rev:	5
		Reviewed By:	ANURAG



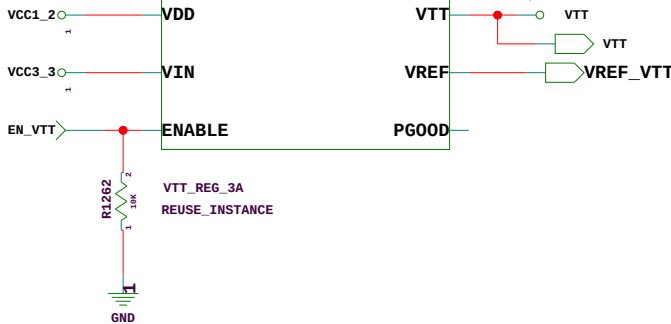
Description:		Tejas Networks	
DESCRIPTION			
		Sheet	2 of 10
Project:	LINE36	Drawn By:	KEVIN/MANI
Date:	6-24-2024_12:00	Rev:	5
		Reviewed By:	ANURAG

VTT_OV6_LS1043A

VCC3_3

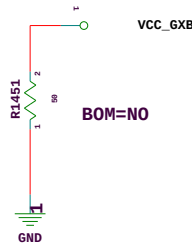
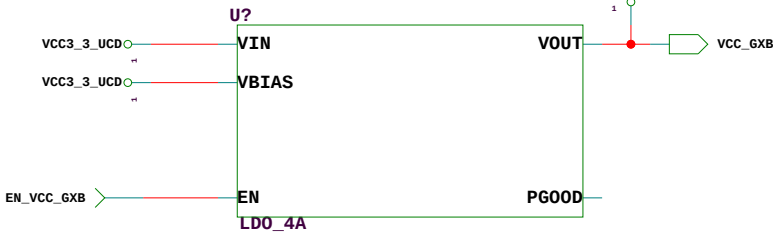
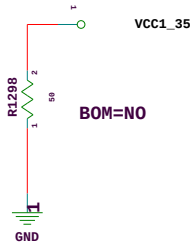
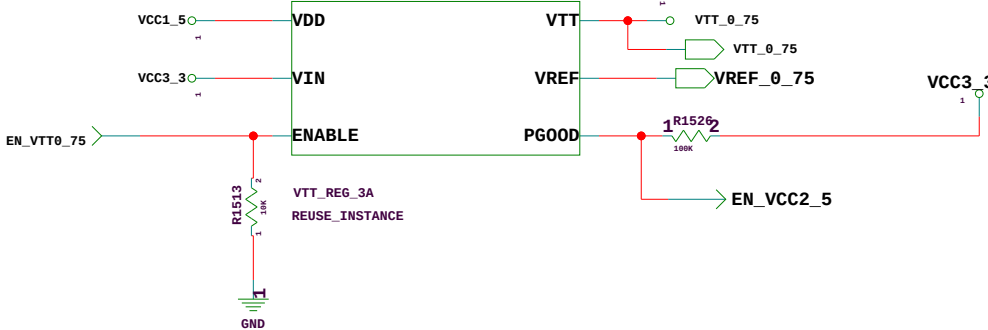


PLACE THIS CAP NEAR VIN PIN



VTT_OV75_CFPGA

VCC3_3



Description:

DESCRIPTION

Tejas Networks

Sheet 5 of 10

Project: LINE36

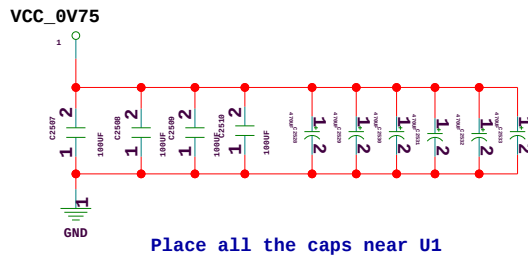
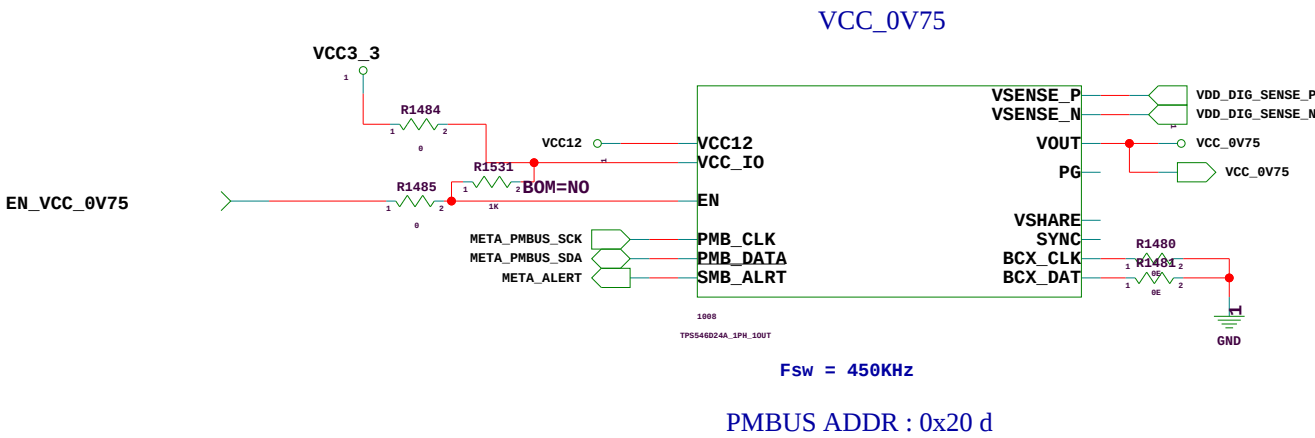
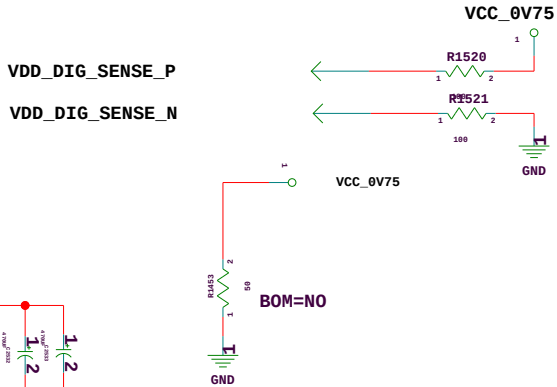
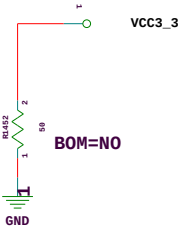
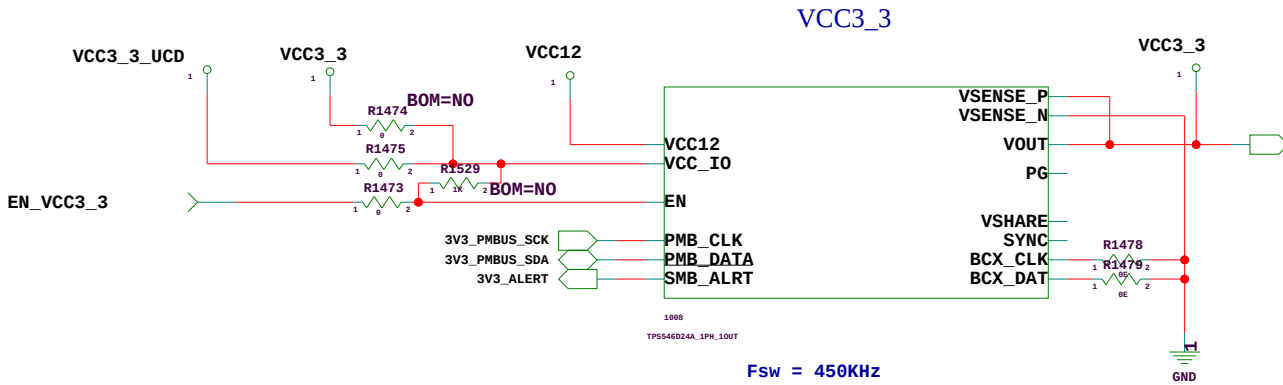
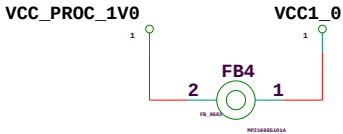
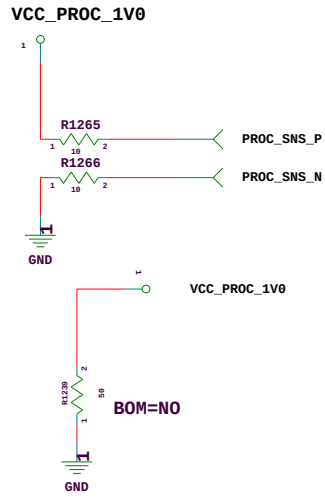
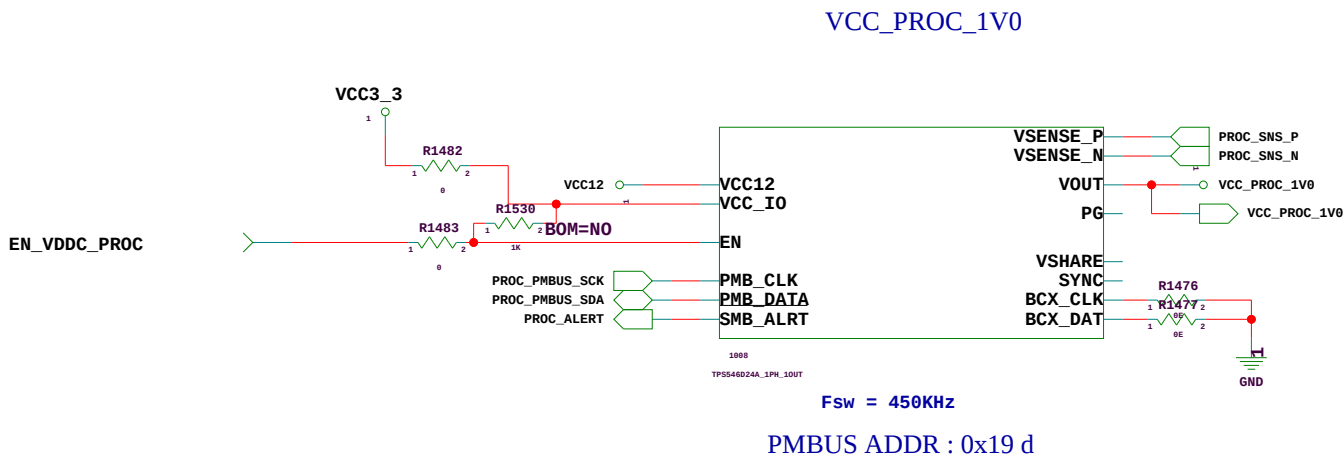
Drawn By: KEVIN/MANI

Date: 6-24-2024_12:00

Rev: 5

Reviewed By: ANURAG

PART NUMBER: 141-PCC000155-E



A

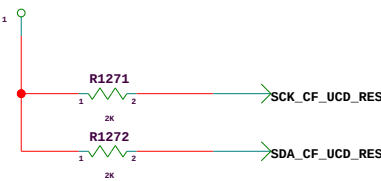
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C

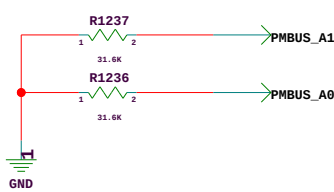
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UCD90160

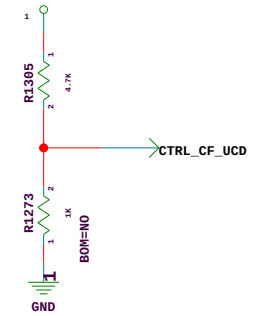
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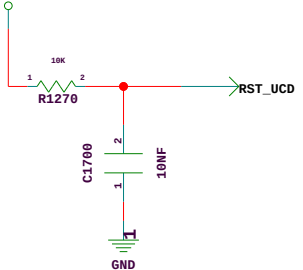
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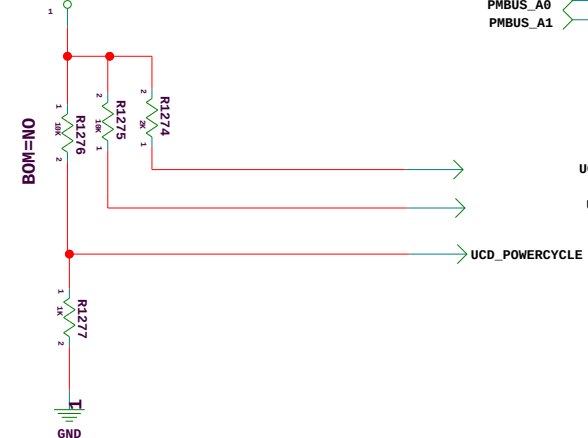
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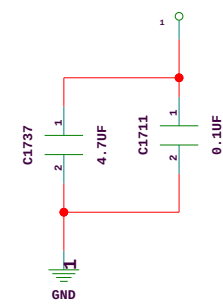
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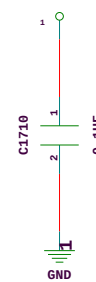
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VCC3_3_UCD

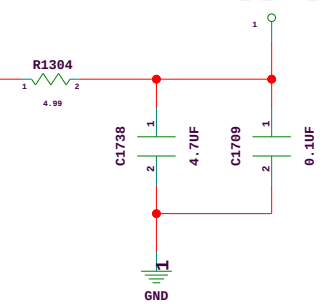


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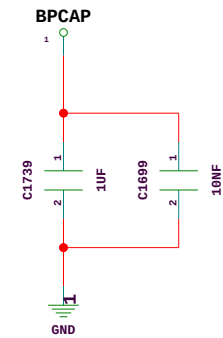


PLACE CLOSE TO PIN 7

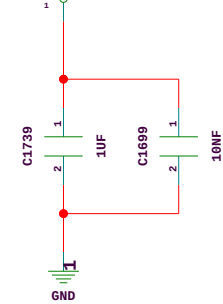
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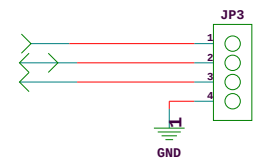
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BPCAP

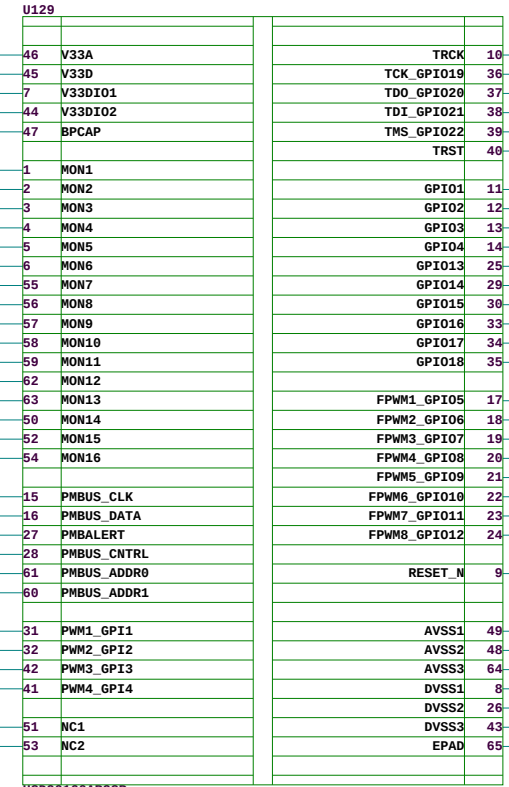
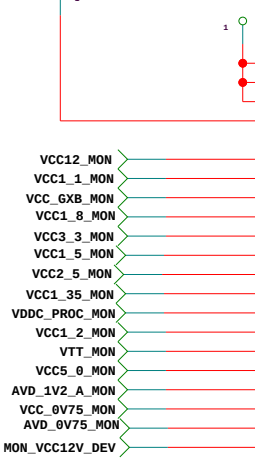


UCD_VOL_INT_RES
SDA_CF_UCD_RES
SCK_CF_UCD_RES



TJA_SAEJEC_KTSW-SDA-BS-1-A
HTSM-104-05-F-S

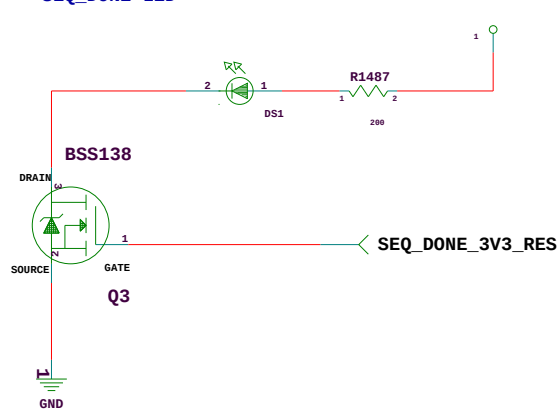
BPCAP VCC3_3_UCD VCC3_3_UCD_A



PMBUS ADDR : 0x52

SEQ_DONE LED

VCC3_3_UCD

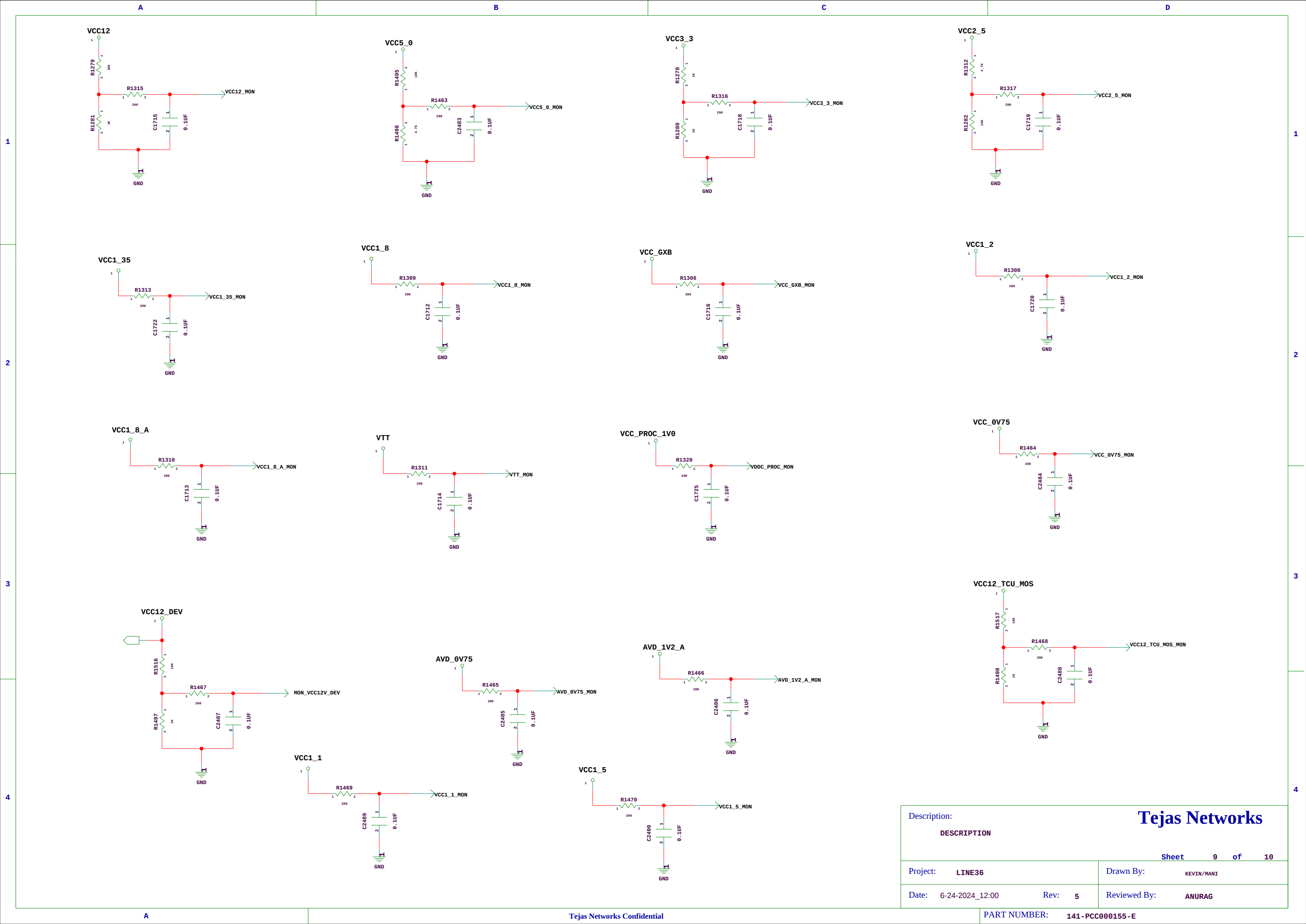


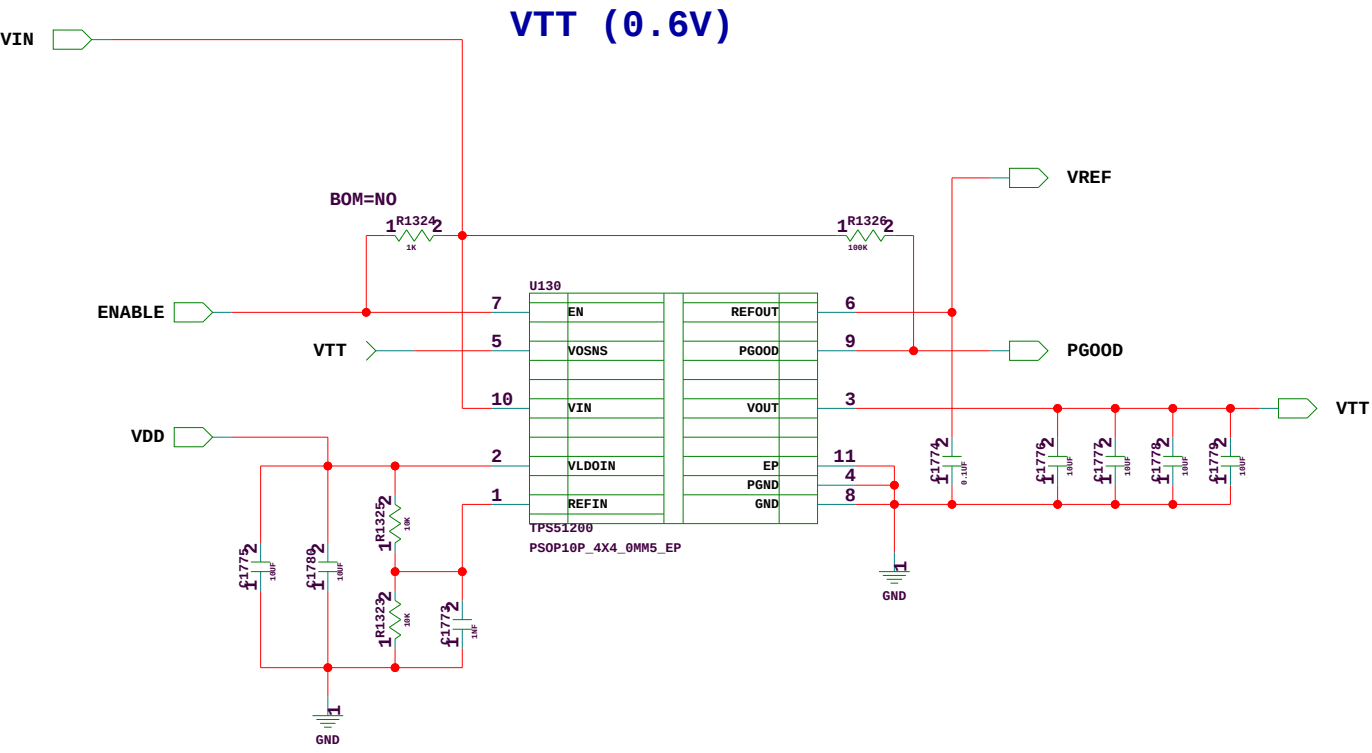
Tejas Networks

Description:		DESCRIPTION	
Project:		LINE36	
Date:		6-24-2024_12:00	
Rev:		5	
Drawn By:		KEVIN/MANI	
Reviewed By:		ANURAG	

PART NUMBER: 141-PCC000155-E

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Description:		Tejas Networks	
DESCRIPTION		Sheet 1 of 2	
Project:	LINE36	Drawn By:	KEVIN/MANI
Date:	6-24-2024_12:00	Rev:	5
		Reviewed By:	ANURAG

A

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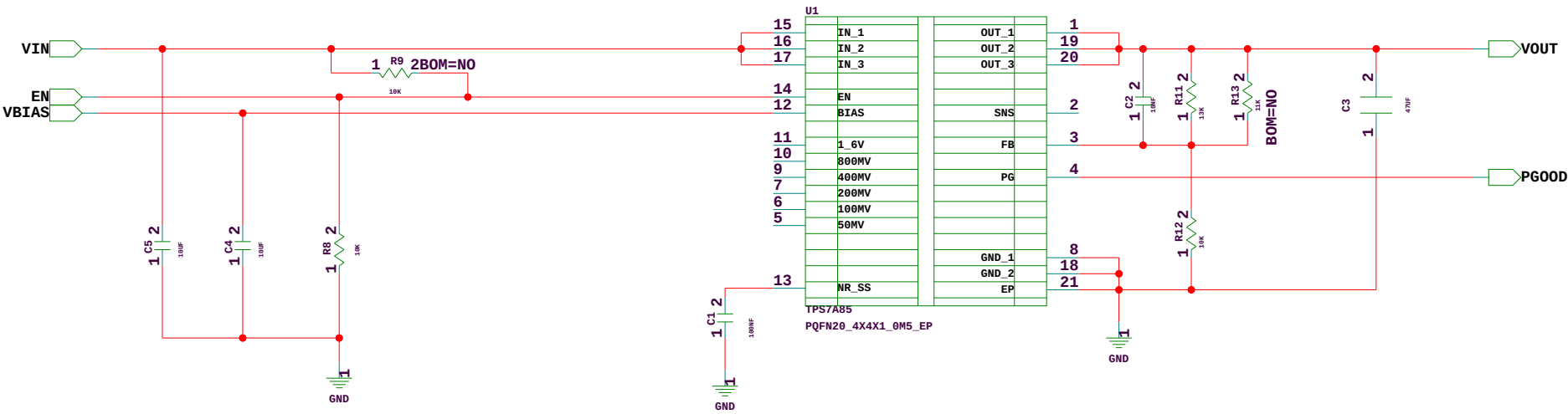
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Description:		Tejas Networks	
DESCRIPTION			
		Sheet 2 of 2	
Project:	IO-U3	Drawn By:	VISHWAS
Date:	9-7-2023_16:37	Rev:	1
		Reviewed By:	ANEESH & ARUL

A

Tejas Networks Confidential

PART NUMBER: PART_NUMBER



Description:

DESCRIPTION

Tejas Networks

Sheet 1 of 1

Project: PROJECT NAME

Drawn By: KEVIN/MANI

Date: 6-24-2024_12:00

Rev: REV

Reviewed By: DHIRAJ

PART NUMBER: PART_NUMBER

A

B

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2

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Description:		Tejas Networks	
DESCRIPTION			
		Sheet 2 of 2	
Project:	IO-U3	Drawn By:	VISHWAS
Date:	9-7-2023_16:37	Rev:	1
		Reviewed By:	ANEESH & ARUL

A

Tejas Networks Confidential

PART NUMBER: PART_NUMBER

