TI SN65LVCP1414 IBIS-AMI Models

User's Guide

Version 00.01.00
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Disclaimer

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The TI IBIS-AMI models contain information on products that is based on high-level specifications. These may not accurately represent the product design in all cases. Please verify the accuracy of the models with TI before using the results.

1 Introduction

This document describes the organization, structure, and proper usage of the TI SN65LVCP1414 IBIS-AMI models (compiled and approved for external customer release), hereafter referred to as the "model" for short. The model is intended for use by the SN65LVCP1414 design team and by SN65LVCP1414 customers for system-level modeling and verification. This document assumes that you are familiar with the relevant IBIS-AMI modeling specifications.

1.1 Formatting Conventions

The help readability, various formatting conventions are used throughout this document:

- Hyperlinks to material within and outside this document are marked in blue.
- Courier font is used for file names, code, variables, structures, parameters, and terminal commands.

1.2 Charter of the SerDes IBIS-AMI models

The models are designed in accordance with the IBIS-AMI standard and attempt to model the significant characteristics of most components in the SN65LVCP1414. The models are not intended to be an exact representation of SN65LVCP1414 components implemented. Rather, the models seek to provide as high a degree of accuracy as is feasible outside of Spice-based models and simulations.

1.3 Is / Is Not Table

The following table describes the features and purposes of the models, as well as the limitations of the models.

Table 1: Model Is / Is Not Table

Is	Is Not
Compiled for 32-bit AMI EDA tool that run in Windows platform	Compiled for any other platform (i.e. 32- or 64-bit Linux)
Compliant to IBIS-AMI 5.0	Compliant to a more recent BIRD revisions, if they exist
Model of SN65LVCP1414 functionality, non-idealities, and performance	Exact representation of implemented components

2 About this Release

2.1 IBIS-AMI Model Files

Table 2 shows the key IBIS-AMI model files delivered with the model release as part of the compressed archive.

Table 2: IBIS-AMI files included with the model release

File Name	Type	Description
TI_SN65LVCP1414_AMI_users_guide.pdf	PDF	TI SN65LVCP1414 AMI model user's guide.
sn65lvcp1414.ibs	IBIS	Top-level IBIS wrapper for the Tx and Rx AMI model.
sn65lvcp1414.ami	AMI	Parameters file for the Rx model as required by the IBIS-AMI standard. This is a text file which is common for all OS/execution platforms.
sn65lvcp114.dll	DLL	Windows 32-bit compiled shared library for the Rx model. This shared library includes the AMI_Init, AMI_GetWave, and AMI_Close functions defined in the IBIS-AMI standard.
sn65lvcp1414_rxterm.s2p sn65lvcp1414_rxterm.s4p	s-parameter	Termination at the receiver's input. This s2p/s4p should be connected directly to the input of the device after the receiver package. It is recommended to use s2p for receiver termination if EDA tool can handle s2p, otherwise, please use the s4p for the receiver termination.
sn65lvcp1414_rx_pkg.s4p	s-parameter	Receiver package
sn65lvcp1414_tx_pkg.s4p	s-parameter	Transmitter packages

2.2 RX AMI model specific parameters

The following settings correspond to the following values for this model.

Table 3. Parameters for SN65LVCP1414

vod	0 = low vod setting 1 = high vod setting
dcgain	0 = low dc gain setting (-6dB) 1 = high dc gain setting (0dB)
acgain	If dcgain = 0 acgain = 0 actual acgain is 0 acgain = 1 actual acgain is 11 if dcgain = 1 acgain = 0 actual acgain is 1 acgain = 1 actual acgain is 11
EQ	0 to 7. Please refer to datasheet page 15 for level of gain
cable	0 = trace mode 1 = cable mode

3 Model Verification

This model had been through detail verification and correlation processes. There are three project kits included in this release package for QCD, Hyperlynx, and ADS. User can use these project kits as the foundation and start building their system by adding more complex structure to it.

3.1 SiSoft Quantum Channel Designer (QCD) User's Guide

The following are steps specific to SiSoft Quantum Channel Designer (QCD).

1. Open the installation archive using the winzip utility in Windows.
2. Create a project

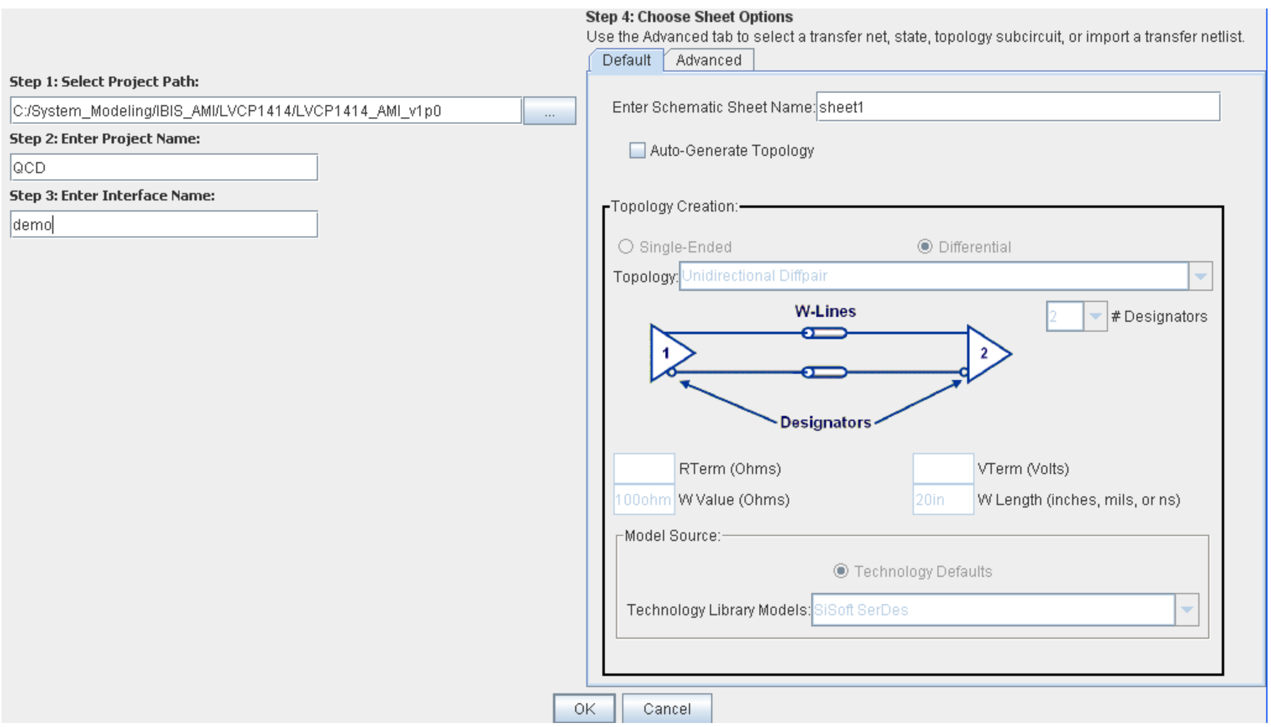


Figure 1. Create a project

3. In QCD, import the IBIS files (`sn65lvcp1414.ibs`).

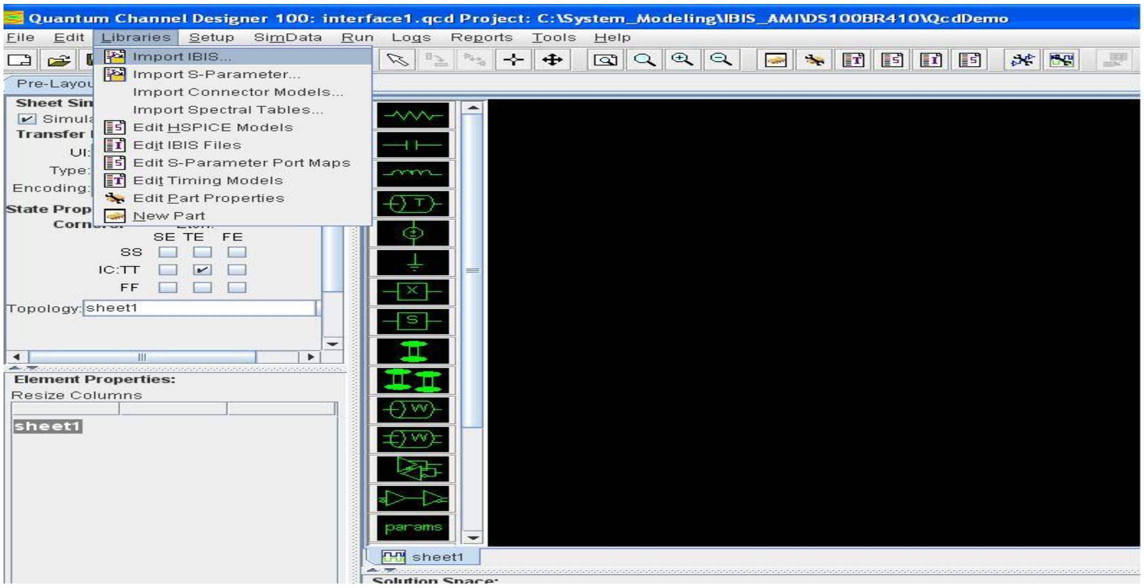


Figure 2. Import IBIS file

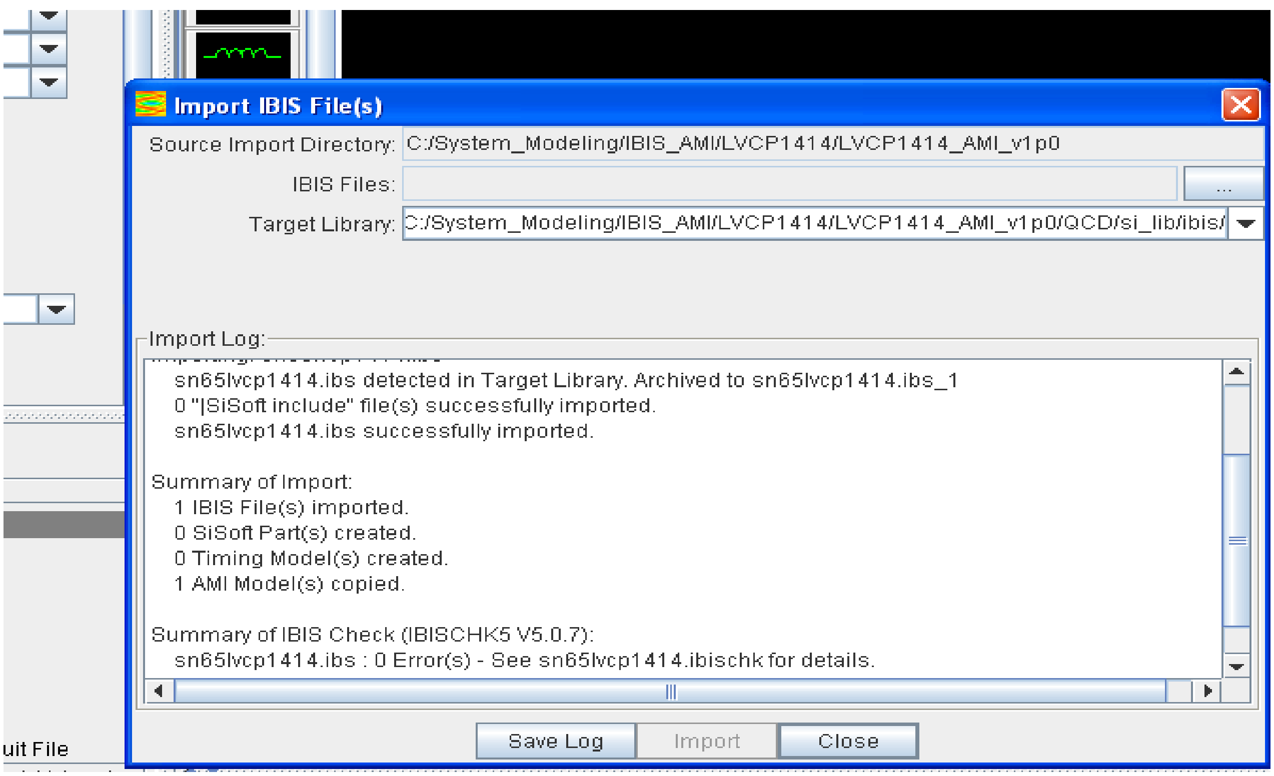


Figure 3. IBIS file successfully imported

4. Import the s-parameter files for channel.

    a. At this point, the `.dll`, `.ibs`, and `.ami` files have been copied to your project folder, in the `si_lib/ibis/` sub-directory.

5. Add TX and RX buffer symbols on the sheet

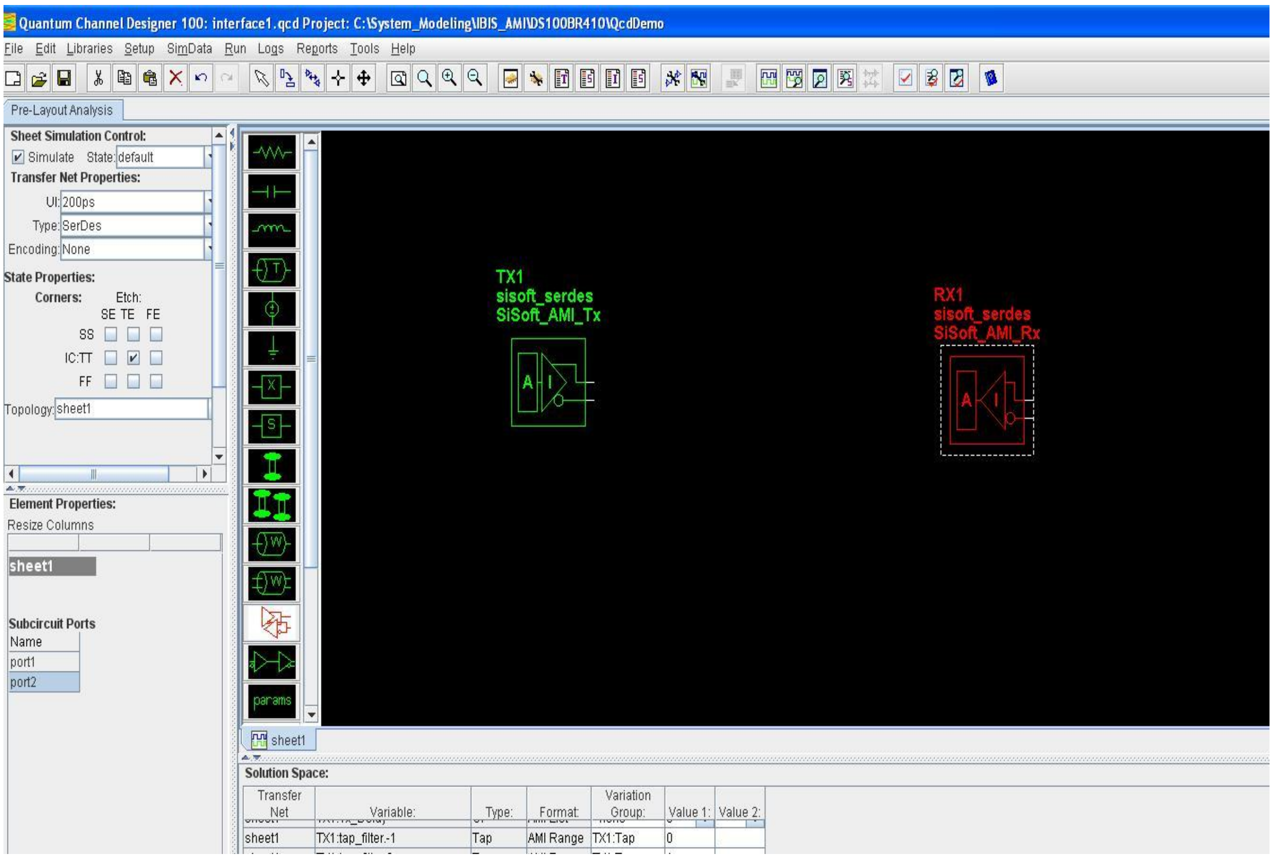


Figure 4. Insert TX and RX buffers

6. Instantiate the sn65lvcp1414 RX by right clicking on the RX symbol, and then clicking on Select IBIS File & Model. Also instattiate a transmitter to drive the sn65lvcp1414.

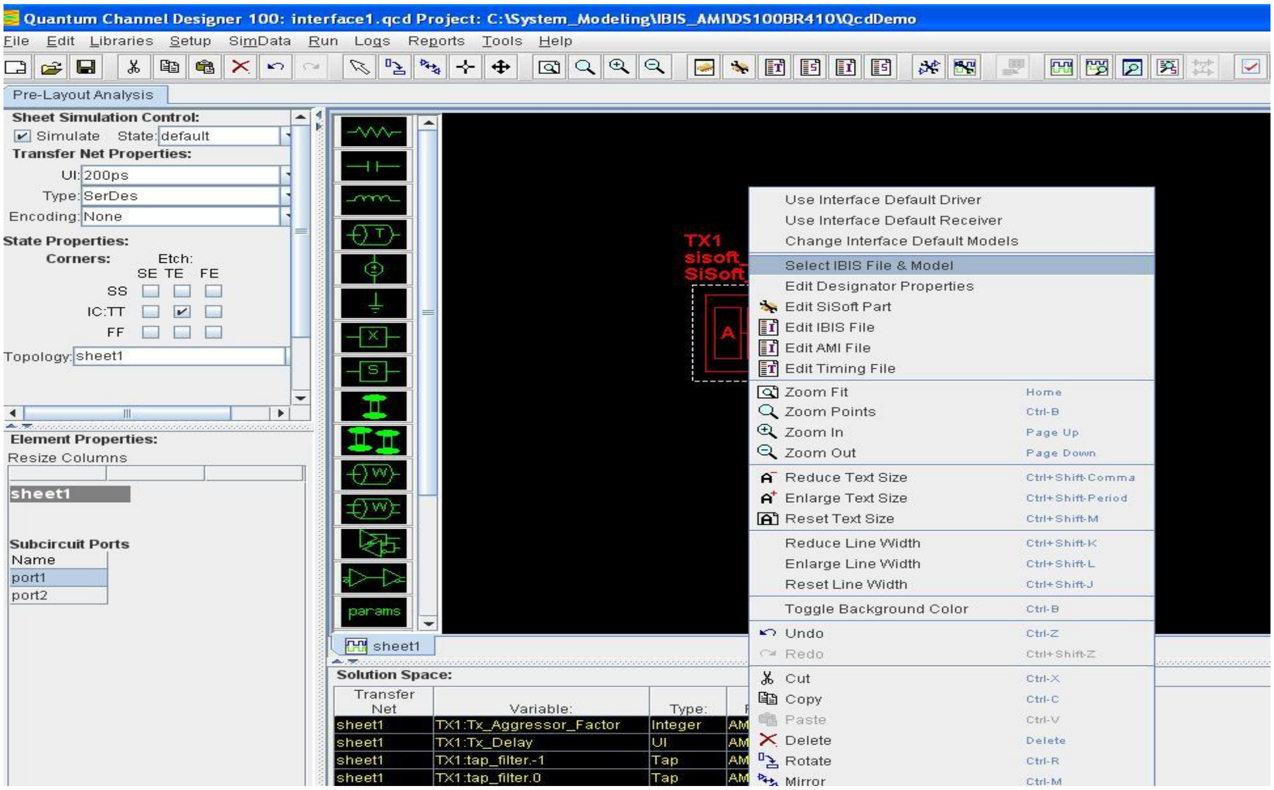


Figure 5. Instantiate Sisoft ideal TX and sn65lvcp1414 RX model

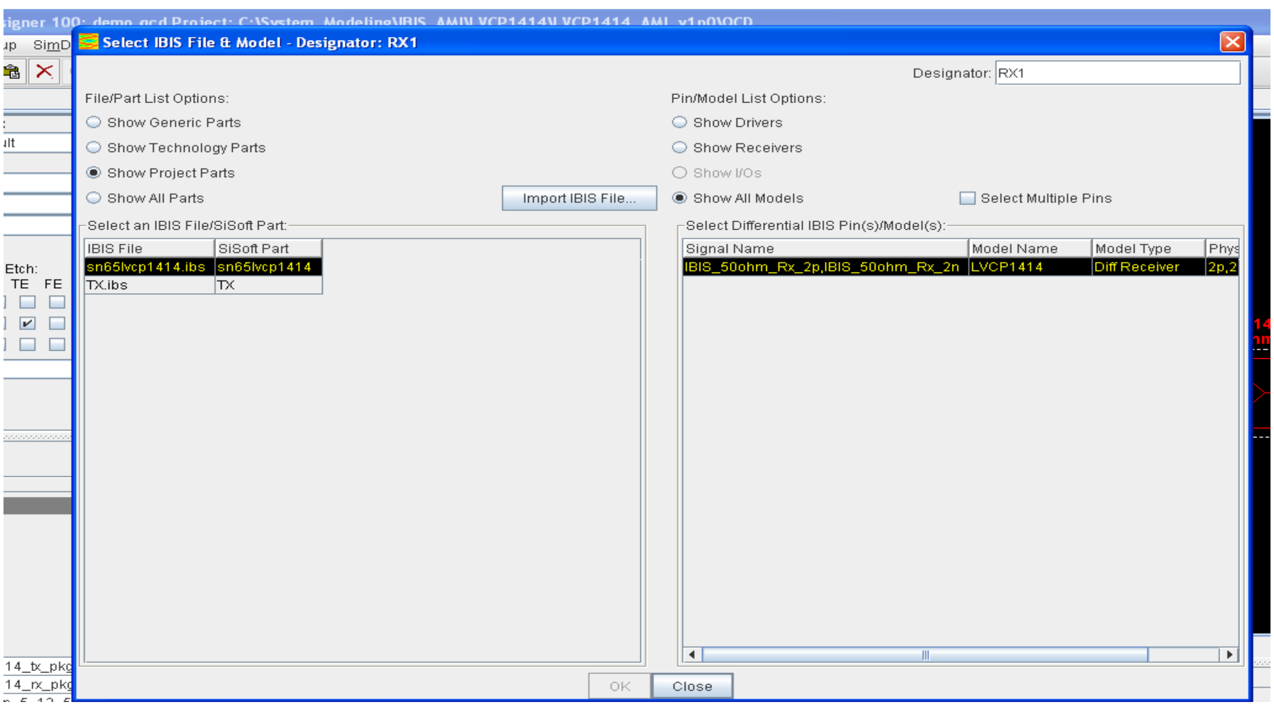


Figure 6. Choose sn65lvcp1414 for RX

7. The complete schematic for this demo. As shown in the schematic a return loss s-parameter is connected to the input of the receiver. This

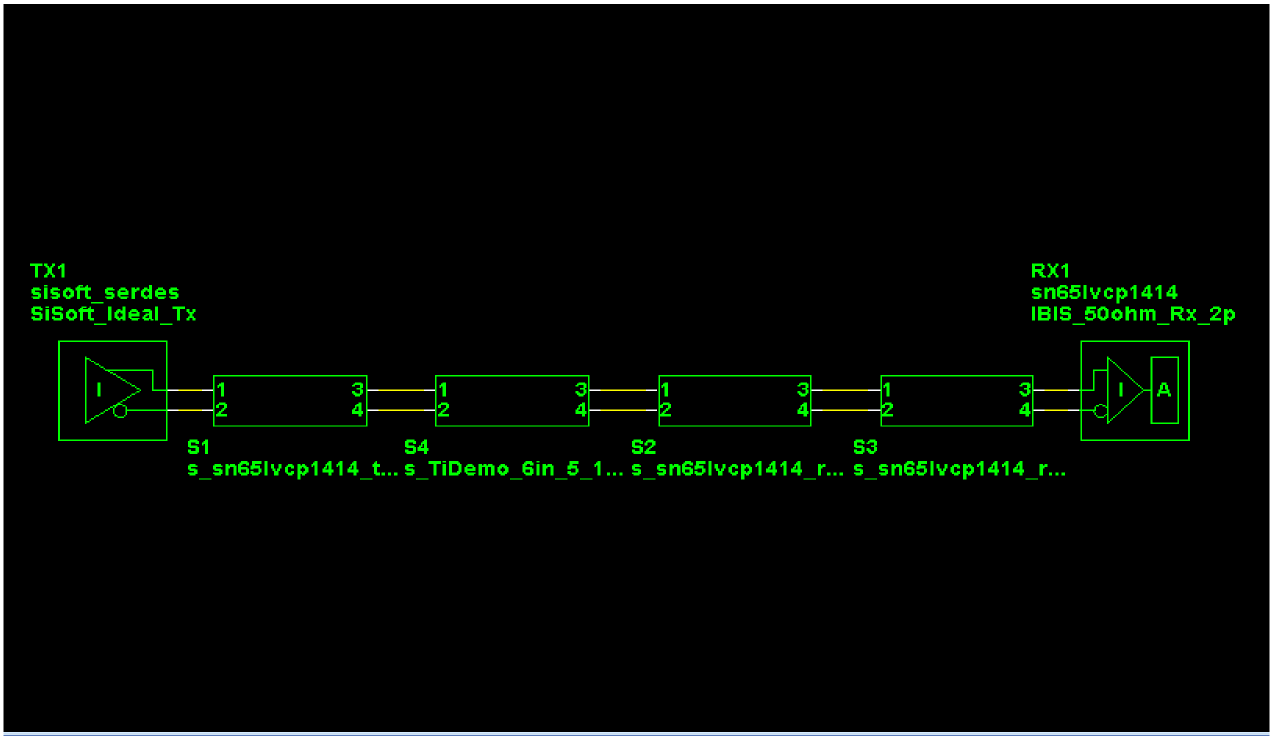


Figure 7. Complete schematic to verify sn65lvcp1414

8. Setup up simulation parameters

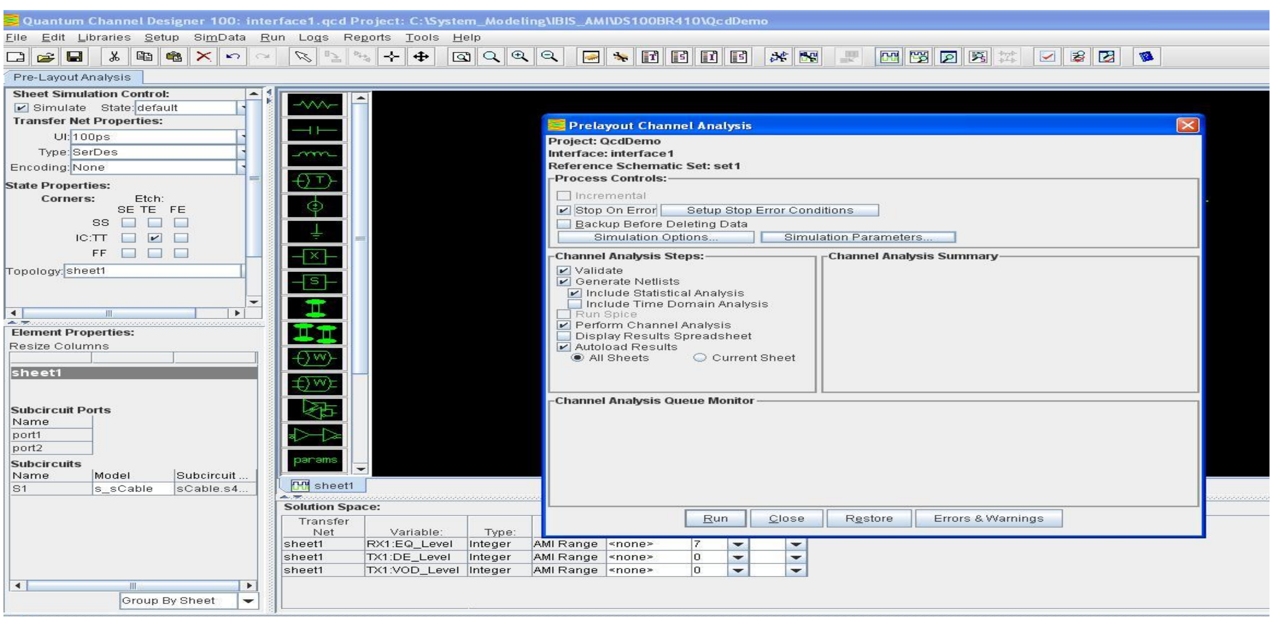
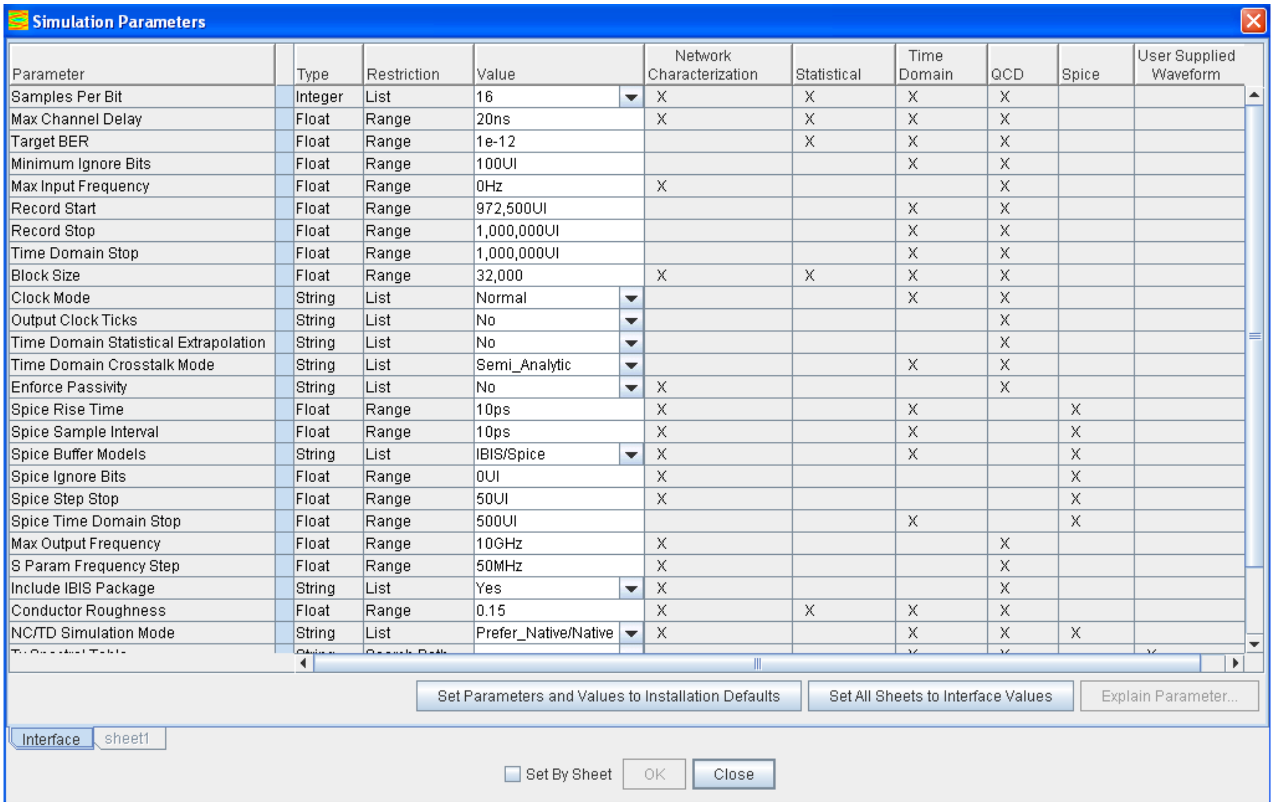


Figure 8. Click on the Simulation Parameter button to properly setup the parameters



Parameter	Type	Restriction	Value	Network Characterization	Statistical	Time Domain	QCD	Spice	User Supplied Waveform
Samples Per Bit	Integer	List	16	X	X	X	X		
Max Channel Delay	Float	Range	20ns	X	X	X	X		
Target BER	Float	Range	1e-12		X	X	X		
Minimum Ignore Bits	Float	Range	100UI			X	X		
Max Input Frequency	Float	Range	0Hz	X			X		
Record Start	Float	Range	972,500UI			X	X		
Record Stop	Float	Range	1,000,000UI			X	X		
Time Domain Stop	Float	Range	1,000,000UI			X	X		
Block Size	Float	Range	32,000	X	X	X	X		
Clock Mode	String	List	Normal			X	X		
Output Clock Ticks	String	List	No				X		
Time Domain Statistical Extrapolation	String	List	No				X		
Time Domain Crosstalk Mode	String	List	Semi_Analytic			X	X		
Enforce Passivity	String	List	No	X			X		
Spice Rise Time	Float	Range	10ps	X		X		X	
Spice Sample Interval	Float	Range	10ps	X		X		X	
Spice Buffer Models	String	List	IBIS/Spice	X		X		X	
Spice Ignore Bits	Float	Range	0UI	X				X	
Spice Step Stop	Float	Range	50UI	X				X	
Spice Time Domain Stop	Float	Range	500UI			X		X	
Max Output Frequency	Float	Range	10GHz	X			X		
S Param Frequency Step	Float	Range	50MHz	X			X		
Include IBIS Package	String	List	Yes	X			X		
Conductor Roughness	Float	Range	0.15	X	X	X	X		
NC/TD Simulation Mode	String	List	Prefer_Native/Native	X		X	X	X	

Figure 9. Setup the simulation parameters

9. Run the simulation.

4 Model Caveats

The model has the following limitations and known issues:

- This is an Equalizer model and hence it does not generate clock tick. Users that simulate this model as serial link is responsible to verify the capability of an EDA tool to regenerate the RX eye without clock tick.
- This model is compiled for 32bit AMI EDA tools. One can possibly run this model on a 64bit Windows machine by installing 32bit AMI EDA tools on the 64bit Windows machine