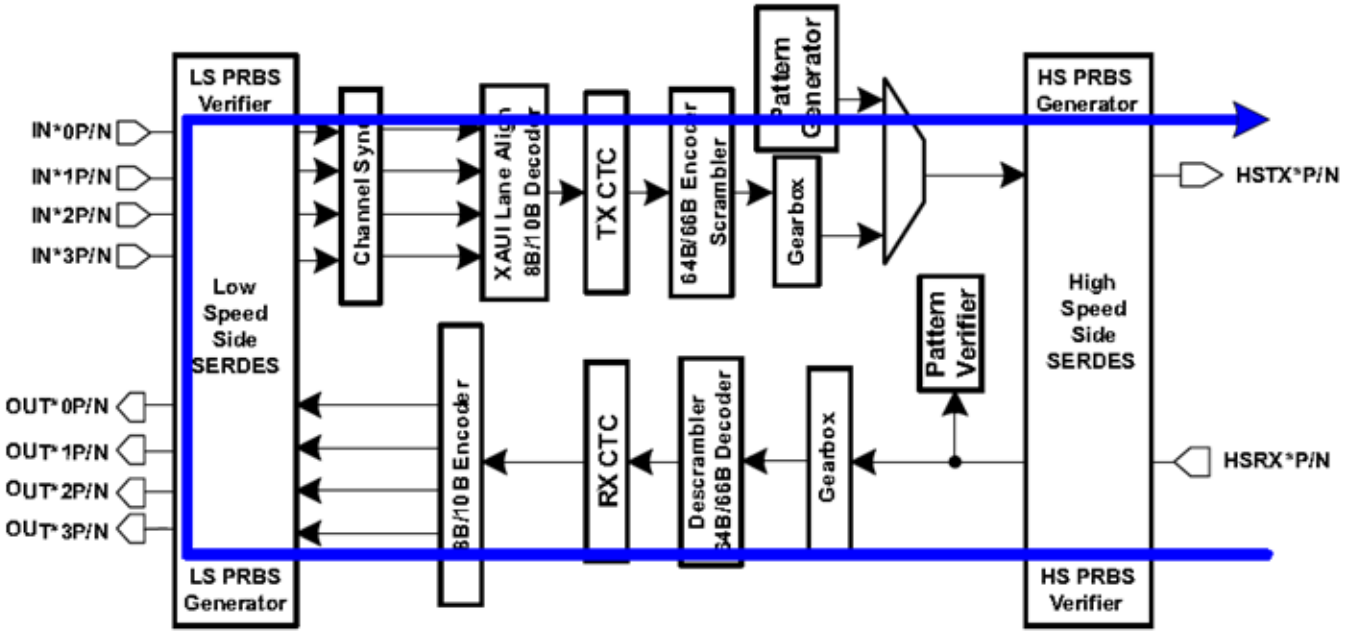
Deep Remote Loopback for the 10GBASE-KR Mode

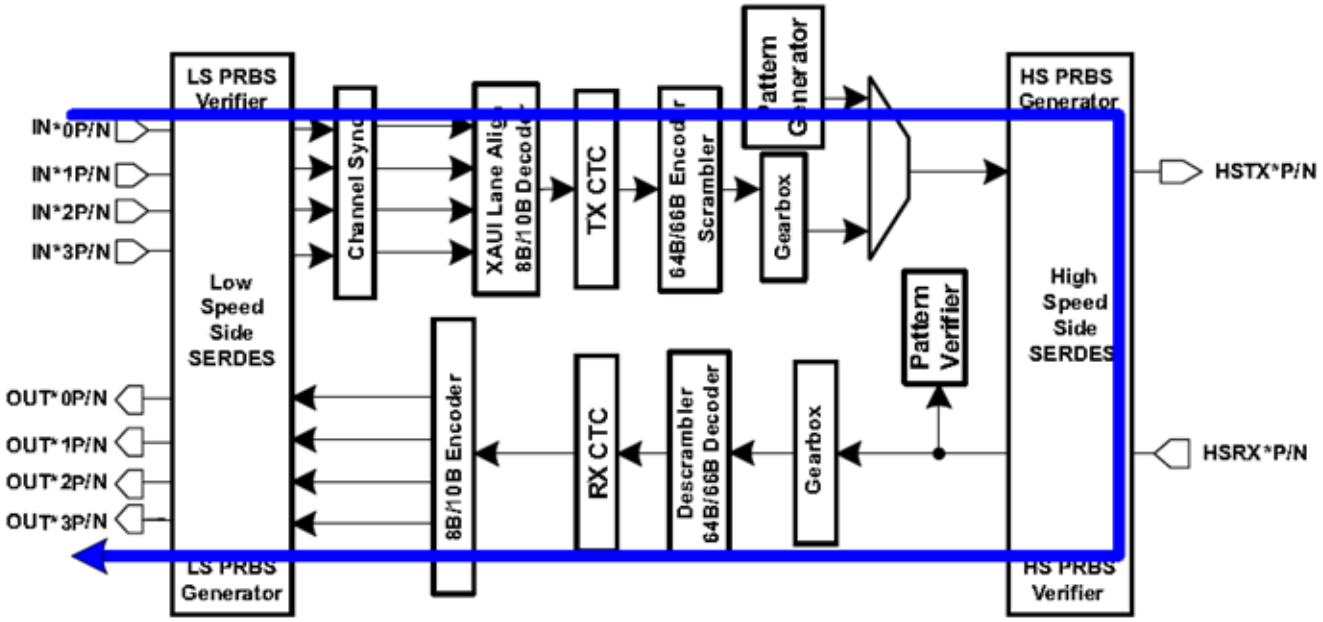


To enable the Deep Remote Loopback:

0x1E.000B [Bit 3] =‘1’

Data is accepted on the high speed side receive SERDES pins (HSRX*P/N), tranverses the entire data path is returned through the entire transmit data path and sent out through the high speed side transmit (HSTX*P/N). The low speed side outputs on OUT*P/N pins are still available for monitoring and should be correctly terminated. The low speed side inputs on IN*P/N should be electrically idle (floating).

Deep Local Loopback for the 10GBASE-KR Mode



To enable the Deep Local Loopback:

0x1E.000B [Bit 1] =‘1’

Data is accepted on the low speed SERDES pins (IN*P/N), traverses the entire transmit data path, is returned through the entire receive data path and sent out through the low speed side receive SERDES pins (OUT*P/N). The high speed side outputs on HSTX*P/N pins are available for monitoring. The high speed side inputs on HSRX*P/N should be electrically idle (floating).