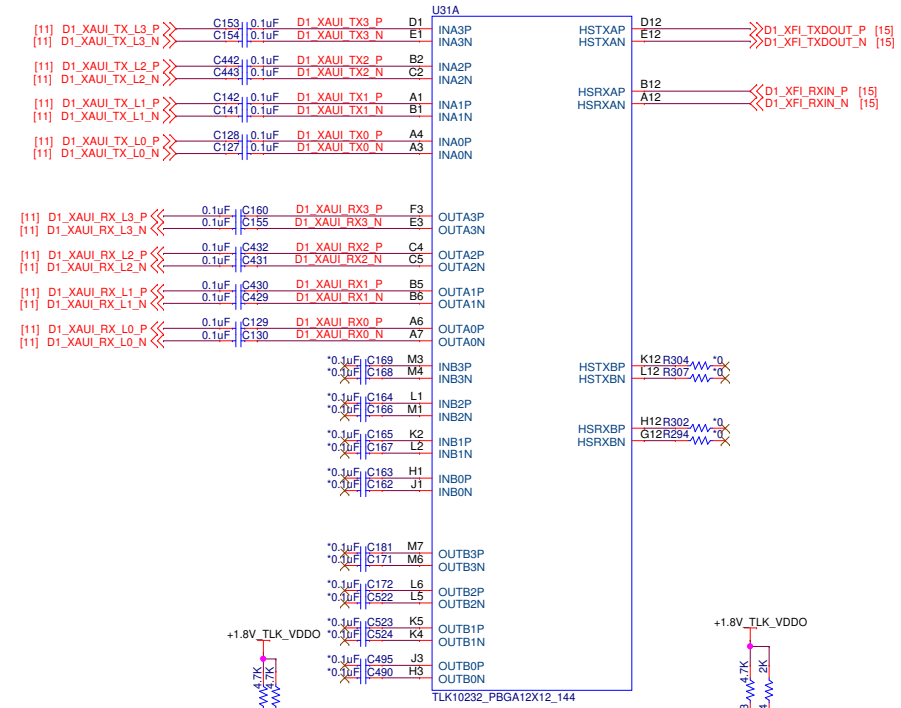
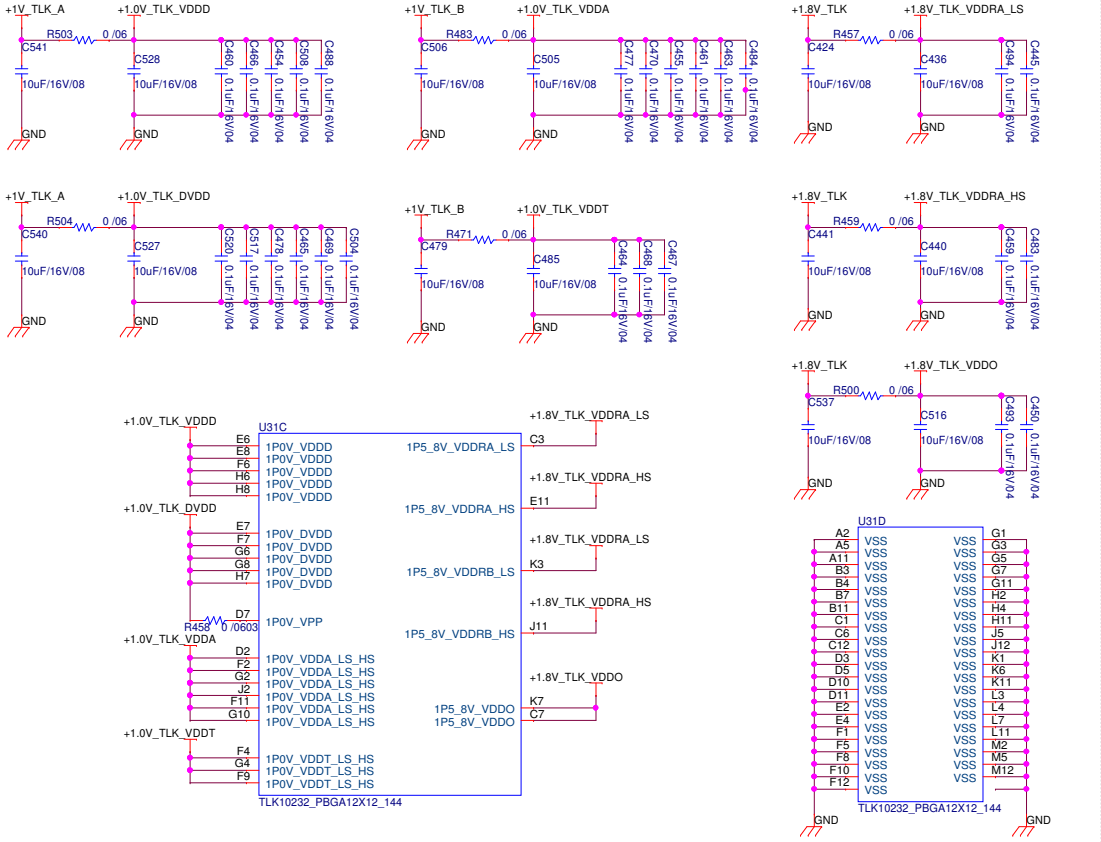
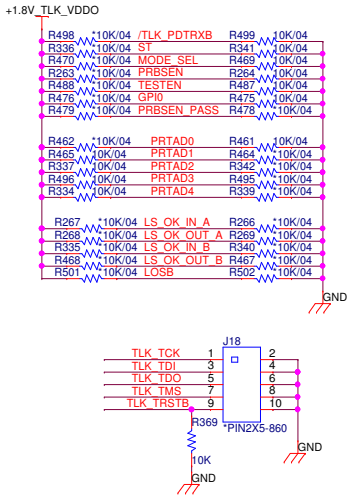
XAUI
FPGA<<<>>>TLK10232







PULL UP/DOWN

LOSA (output) : 0: Signal detected.1: Loss of signal.
LS_OK_IN_A (input)= 0: Channel A link partner receive lanes not aligned.
1: Channel A link partner receive lanes aligned
LS_OK_OUT_A (output)= 0: Channel A link partner transmit lanes not aligned.
1: Channel A link partner transmit lanes aligned.
PDTRXA_N (input) 0 : power down 1: operation
PRBSEN (input) = 0: Disable PRBS, 1: Enable PRBS
PRBS_PASS (output) = 0: PRBS error is detected,
1: PRBS pattern reception is error free
TESTEN = 0 : operation, 1: Debug mode
GPI0 = 0 : operation, 1: Debug mode
AMUXA &AMUXB =NC

{MODE_SEL pin, Register 1E.0001 bit 10}	ST = 0 (Clause 45)	ST = 1 (Clause 22)
1x	10G	10G
01	10G	10G
00	10G-KR/1G-KX (Determined by Auto Neg)	1G-KX (No Auto Neg)