# Schematic Review Form

TMDS181

| Pin # | Name | Info | Violations | Description |
|---|---|---|---|---|
| 13, 43 | VCC | missing high freq filtering capacitor | | 3.3 V power supply |
| 14,23,24,37,48 | VDD | slightly more filtering may result in a more stable VDD | | 1.2 V power supply |
| 7,19,41,30,Pad | GND | ok | | Ground |
| 2,3 | IN_D2p/n | ok | | Channel 2 differential input |
| 5,6 | IN_D1p/n | ok | | Channel 1 differential input |
| 8,9 | IN_D0p/n | ok | | Channel 0 differential input |
| 11,12 | IN_CLKp/n | ok | | Clock differential input |
| 34,35 | OUT_D2n/p | ok | | TMDS data 2 differential output |

| 31,32 | OUT_D1n/p | ok | | TMDS data 1 differential output |
|---|---|---|---|---|
| 28,29 | OUT_D0n/p | ok | | TMDS data 0 differential output |
| 25,26 | OUT_CLKn/p | ok | | TMDS data clock differential output |
| 4 | HPD_SRC | This will be coming from receptacle. (page 43 in datasheet) | seems that the HPD are swapped for sink and source | Hot plug detect output to source side |
| 33 | HPD_SNK | This will be going to rx (page 43 in datasheet) | seems that the HPD are swapped for sink and source | Hot plug detect input from sink side |
| 45,44 | SPDIF_IN ARC_OUT | gnd, float | | SPDIF signal input Audio return channel output |
| 47,46 | SDA_SRC SCL_SRC | gnd | | Source side TMDS port bidirectional DDC data line Source side TMDS port bidirectional DDC clock line |
| 39,38 | SDA_SNK SCL_SNK | coming from receptacle | | Sink side TMDS port bidirectional DDC data line Sink side TMDS port bidirectional DDC clock line |
| 42 | OE | ok | | Operation enable/reset pin OE = L: Power-down mode OE = H: Normal operation Internal weak pull up: Resets device when transitions from H to L |

| | | | | |
|---|---|---|---|---|
| 17 | SIG_EN | ok | | Signal detector circuit enable<br>SIG_EN = L: Signal detect circuit disabled:<br>SIG_EN = H: Signal detect circuit enabled:<br>When no valid clock device enters<br>standby mode.<br>Internal weak pull down |
| 20 | PRE_SEL | ok | | De-emphasis control when I2C_EN/PIN = Low.<br>PRE_SEL = L: −2 dB<br>PRE_SEL = No Connect: 0 dB<br>PRE_SEL = H: Reserved<br>When I2C_EN/PIN = High de-emphasis is controlled through I2C |
| 21 | EQ_SEL/A0 | ok | | Input receive equalization pin strap when I2C_EN/PIN = Low<br>EQ_SEL = L: Fixed EQ at 7.5 dB at 3 GHz<br>EQ_SEL = No Connect: Adaptive EQ<br>EQ_SEL = H: Fixed at 14 dB at 3 GHz<br>When I2C_EN/PIN = High address bit 1<br>Note: 3 level for pin strap programming but 2 level when I2C address |
| 10 | I2C_EN/PIN | ok | | I2C_EN/PIN = High; puts device into I2C Control Mode<br>I2C_EN/PIN = Low; puts device into pin strap mode<br>Note: I2C CSR is addressable at all times, but features that can be controlled by pin strapping can only be changed by I2C when this pin is pulled high |
| 15 | SCL_CTL | ok | | I2C clock signal<br>Note: When I2C_EN = Low Pin strapping takes priority and those functions cannot be changed by I2C |
| 16 | SDA_CTL | ok | | I2C data signal<br>Note: When I2C_EN = Low Pin strapping takes priority and those functions cannot be changed by I2C |

| 22 | VSadj | ok | | TMDS-compliant voltage swing control nominal resistor to GND |
|---|---|---|---|---|
| 27 | A1 | ok | | High address bit 2 for I2C programming<br>Weak internal pull down<br>Note: When in Pin Strapping Mode leave pin as No connect |
| 36 | TX_TERM_CTL | ok | | Transmit termination control<br>TX_TERM_CTL = H, no transmit termination<br>TX_TERM_CTL = L, transmit termination impedance in approximately 75 to 150 Ω<br>TX_TERM_CTL = No Connect, automatically selects the termination impedance<br>Data rate (DR) > 3.4 Gbps – 75 to 150 Ω differential near end termination<br>2 Gbps > DR < 3.4 Gbps – 150 to 300 Ω differential near end termination<br>DR < 2 Gbps – no termination<br>Note: If left floating will be in automatic select mode. |
| 1 | SWAP/POL | ok | | Input lane SWAP and polarity control pin<br>SWAP/POL = H: receive lanes polarity swap (retimer mode only)<br>SWAP/POL = L: receive lanes swap (redriver and retimer mode)<br>SWAP/POL = No Connect: normal operation |
| 18/40 | NC | ok | | No connect |

**Comments**

see E2E