Techpoint

TP9950 – 1-channel HD-TVI / CVBS / HD Analog Video Decoder with MIPI-CSI2 and Bi-directional Data Back Channel

Preliminary Data Sheet

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1 Introduction

1.1 Description

TP9950 is the universal HD/SD video decoder supporting High Definition Transport Video Interface (HD-TVI) video, NTSC/PAL CVBS video as well as some common HD analog video format decoding. It contains single multi-standard decoders internally for decoding of existing HD analog format of selected input out of the multiple inputs selector. It also can work with any legacy CVBS camera for backward compatibility. The primary application is the HD automotive or any other applications require transport of HD video using low cost cable/ connector.

TP9950 has internal clamping, automatic gain control amplifier for optimal signal conditioning. It has Anti-aliasing filter to reduce crosstalk. Its programmable equalization amplifier and automatic control loop maintain the best performance for low quality and long cable.

TP9950 does majority of the signal processing digitally for its consistency and performance. All control loops are programmable for maximum flexibility. All pixel data are line-locked sampled according to SMPTE-296M and SMPTE-274M standard for the HD-TVI input. It has programmable picture control functions for best video quality. Working with compatible encoder or integrated ISP with HD-TVI encoder and host controller, it supports 2-way data communication over the same cable. For the legacy SD signal, it can also provide programmable upstream data support. The Short to Battery (STB) and Short to Ground (STG) functions are embedded for easy system integration.

TP9950 also integrates MIPI CSI-2 transmitter in compliance with MIPI standard for video data transport.

1.2 Features

- Supports 1-CH HD-TVI and other HD analog video decoding
- Supports 1-CH NTSC/PAL CVBS video decoding
- Supports standard HD and FHD resolution as well as other flexible resolutions defined within the bandwidth limit.

Input

- High speed 10-bit Analog-to-Digital converters (ADC) for 2X over-sampling
- Programmable DC restoration or clamp control
- Programmable gain amplifier (PGA) and Automatic Gain Control (AGC) for best S/N performance
- Programmable Anti-aliasing low pass filter
- Single-ended of differential input support
- Embedded Equalizer (EQ) amplifier for best extended reach performance
- Adaptive EQ algorithm for different cable characteristics.

Signal Processing

- Brightness, Contrast, Saturation, Hue and Sharpness control through host interface
- Supports SMPTE-296M and SMPTE-274M standard sampling for High Definition signals

- Advanced Sync processor for best low signal performance
- Internal digital Horizontal PLL for Line-Locked sampling
- Internal digital Color PLL for accurate color demodulation
- Color gain control and programmable color killer for best small signal performance
- Internal digital filters for HD Y/C separation
- Integrated high quality adaptive 4H comb filter YC separation for NTSC/PAL CVBS decoding to minimize false color and cross luminance artifacts.
- Free run mode with optional blue screen

Output

- MIPI CSI-2 1.1 compliant transmitter up to 2 data lanes
- 8 bit BT656/601

General

- Up-stream data insertion through host interface
- Programmable down-stream data decoding
- Fast 2-wire serial host interface
- Power down mode
- Internal PLL for clock generation
- Embedded Short-To-Battery (STB) and Short-To-Ground (STG) detection
- 1.2/3.3V operation
- 40 pin QFN package
- Single 27MHz crystal operation

2 Order Information

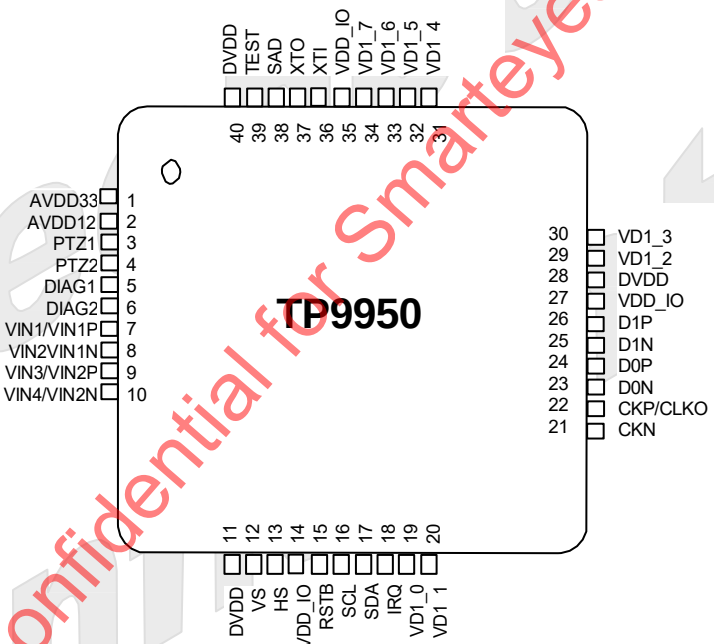
Package Description

Part #	Name	Description	Pin Count	Body Size
TP9950-FA	EPQFN 40L	Quad Flat No Lead Package	40	5 x 5 mm^2

Note:

3 Pin Diagram

40L QFN (Top View)



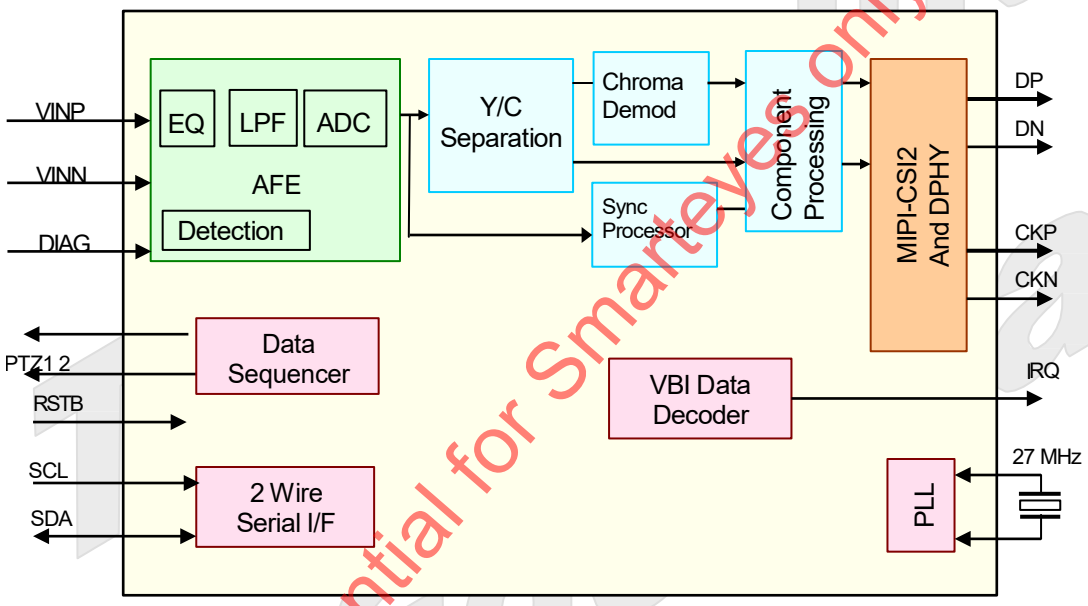
3.1 Pin Description

Pin#	I/O	Pin Name	Description
Analog Section			
7, 8,	I	VIN1-2 / VIN1P/N	Analog Video input. The signal should be AC coupled in by 0.1uF
9, 10	I	VIN3-4 / VIN2P/N	Analog Video input. The signal should be AC coupled in by 0.1uF
3, 4	O	PTZ1-2	Multi-function pins. Left unconnected or use as directed.
5, 6	I	DIAG1-2	Video input fault detection input
1	P	AVDD33	Analog 3.3V power supply
2	P	AVDD12	Analog 1.2V power supply
MIPI Section			
21	O	CKN	MIPI Clock output (negative)
22	O	CKP/CKO	MIPI Clock output (positive) or regular CMOS clock output
23	O	D0N	MIPI Lane 0 data output (negative)
24	O	D0P	MIPI Lane 0 data output (positive)
25	O	D1N	MIPI Lane 1 data output (negative)
26	O	D1P	MIPI Lane 1 data output (positive)
Digital Section			
36	I	XTI	Crystal Input or clock input
37	O	XTO	Crystal output
38	I	SAD	The MPU Serial interface Chip Address Select bit
39	I	TEST	Test pin
15	I	RSTB	Reset input. Low active
16	I	SCL	The MPU Serial interface Clock Line
17	B	SDA	The MPU Serial interface Data Line
18	O	IRQ	Interrupt signal output
12	O	VS	Vertical Sync or multipurpose output
13	O	HS	Horizontal Sync or multipurpose output
19, 20, 29, 30, 31, 32, 33, 34	I/O	VD1_0-7	Video output pin.
14, 27, 35	P	VDD_IO	Digital 3.3V/1.8V power supply
11, 28, 40	P	DVDD	Digital 1.2V power supply
Exposed Pad	P	GND	Connect to system ground

I = Input, O=Output, B=Bidirectional, P=Power

4 Functional Description

4.1 Block Diagram



4.2 Analog Front End (AFE)

The analog front-end conditions and digitizes the AC coupled HD-TVI signal or conventional CVBS signal for further processing. It consists of EQ (equalizer), LPF (anti-alias filter), PGA (Programmable Gain Amplifier), clamp circuits and 10-bit over-sampling high speed ADC (Analog-to-Digital Converter). The clamping circuit restores the DC component of the input signal to establish the proper black level. The PGA together with its control loop compensates for the signal amplitude irregularity due to channe condition and mismatches. It can support a signal variation of +-6dB. The EQ and its associatec feedback loop compensates for the high frequency signal loss due to long cable transmission. The LPF removes signal images due to sampling process and prepares it for digitization. The filter order anc corner frequency can be controlled through register. Both EQ and PGA can both operate in automatic and manual modes through register control. The high speed ADC has 10-bit resolution.

4.3 Sync Processor

The sync processor of TP9950 extracts the horizontal synchronization and the vertical synchronization signals in the video signal. The processor contains digital phase-locked-loops and decision logic tc achieve reliable sync detection in various signal conditions. Minor irregularity in the sync period due tc noise can be filtered out. It can also generate free run signal during video loss and allows the sampling of the video signal in line-locked fashion.

4.4 Y/C separation

The Y/C separation module separates the luminance and chrominance components of the HD-TVI signal for further processing. This is achieved by low-pass and band-pass filter combination due to the spectrum allocation of the luma and chroma signals. For the CVBS signal, a 4H/5-line adaptive comb filter is employed to achieve the high quality 2D Y/C separation. It minimizes the artifacts typically associated with CVBS signal separation.

4.5 Chroma demodulation

The chroma demodulation of the HD-TVI or CVBS signal is done by quadrature down mixing and low-pass filtering. The local carrier signal for use in the quadrature demodulation is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference signal on every scan line. This arrangement allows the demodulation to be done easily with single crystal frequency.

4.6 Automatic Chroma Gain Control

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. The range of ACC controls are –6db to +26db.

4.7 Color Killer

For low color amplitude signals, black and white video, or noisy signals, the color will be “killed” for easy viewing. The color killer uses the burst amplitude measurement as well as sub-carrier PLL status to switch off the color in the output.

4.8 Component Processing

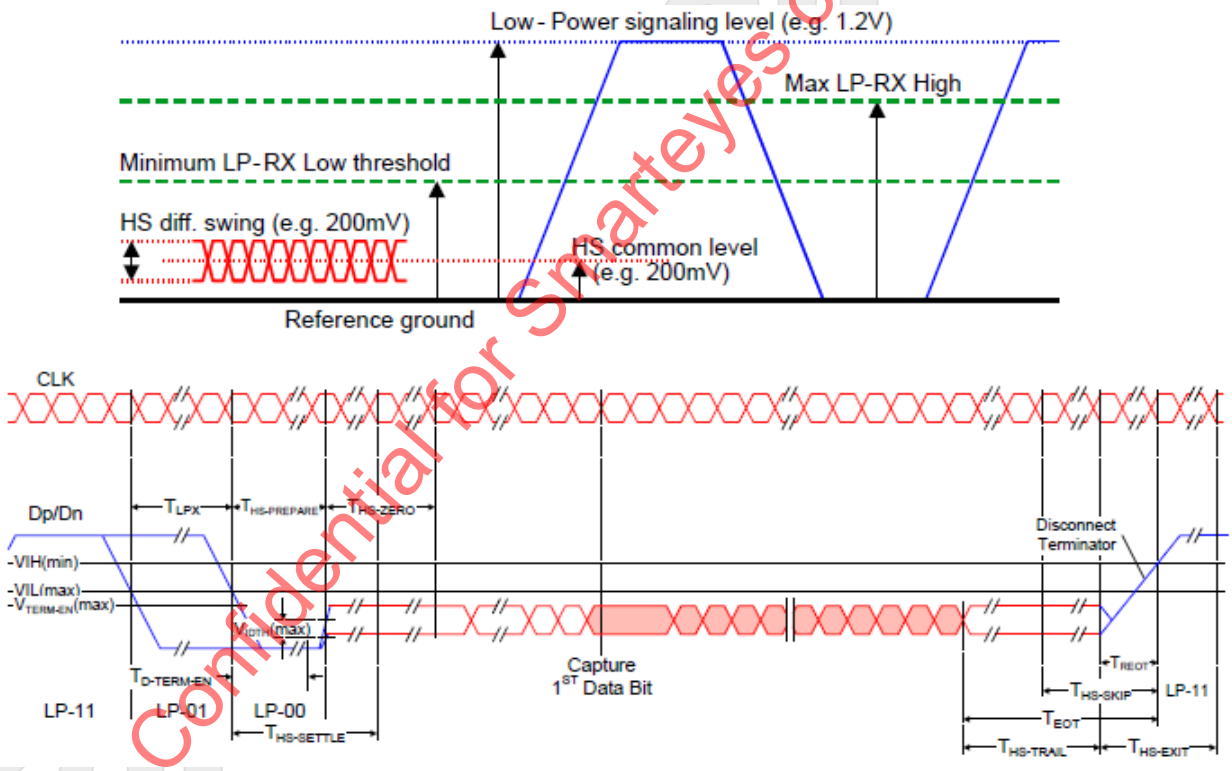
The TP9950 supports the typical brightness, contrast, color saturation and hue adjustment for changing the output video characteristic.

4.9 Sharpness

The TP9950 also provides a sharpness control function through control registers. The center peaking frequency depending on the operating modes.

4.10 MIPI Output

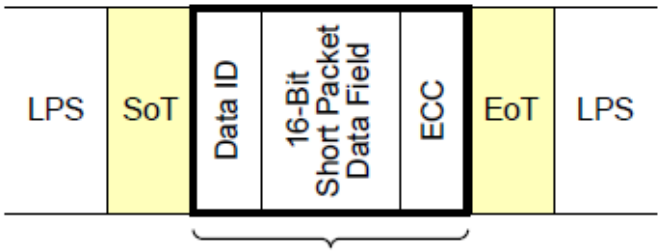
The MIPI transmitter is compatible with MIPI CSI-2 v1.1 interface and D-PHY v1.1 standard. It consists of a low level protocol module that handles all necessary header insertion and mode control and the MIPI physical layer module that handles data conversion and MIPI compatible signal level generation. The D-PHY uses a combination of High Speed Differential Signaling (HS) and Low Power Signaling (LP) to communicate with the MIPI receiver on the other side of the link. The LP signals use their relative voltage levels to communicate state information.



• Figure 1 D-PHY LP & HS Line Levels & Data Burst Transmission

A D-PHY burst transmission consists of the LP state changes signalling a Start of Transmission (SoT), followed by the payload data, then a transition to the Stop state (also called the Low Power State) signalling the End of Transmission (EoT).

CSI-2 transmissions consist of either short packets or long packets. Short packets are used to transmit Frame Start (FS) and Frame End (FE) signals at the beginning (before the first active horizontal line) and end (after the last active line) of a full video frame. Long packets are used to transmit a single horizontal line of video at a time. The packet structure for short and long packets are shown in the figures below.



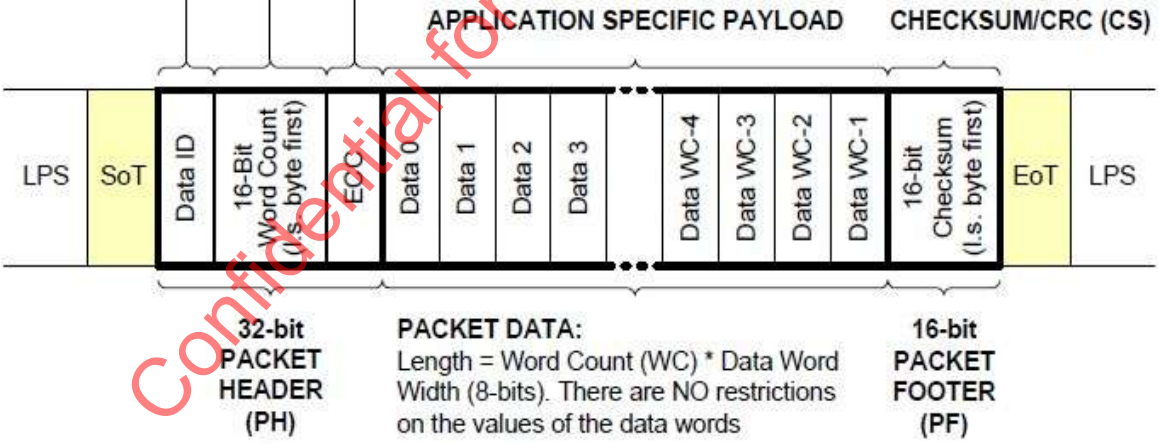
32-bit SHORT PACKET (SH)
Data Type (DT) = 0x00 – 0x0F

Figure 2 Short Packet Structure

DATA IDENTIFIER (DI):
Contains the Virtual Channel Identifier and the Data Type Information
Data Type denotes the format/content of the Application Specific Payload Data.
Used by the application specific layer.

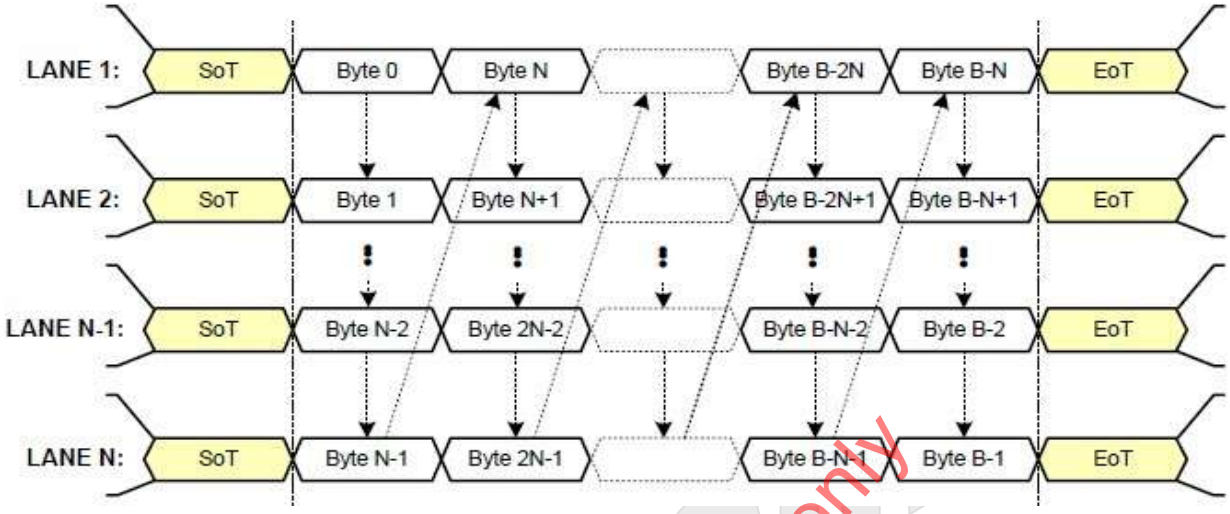
16-bit WORD COUNT (WC):
The receiver reads the next WC data words independent of their values. The receiver is NOT looking for any embedded sync sequences within the payload data. The receiver uses the WC value to determine the end End of the Packet

8-bit Error Correction Code (ECC) for the Packet Header:
8-bit ECC code for the Packet Header. Allows 1-bit errors with the packet header to be corrected and 2-bit errors to be detected



• Figure 3 Long Packet Structure

The MIPI protocol module takes the video data stream and form the packet data. After the protocol handling, it is then de-multiplexed into 1 or 2 or 4 data lanes following the MIPI CSI-2 specification before forwarding to the analog D-PHY module for data seralization and level conversion. The first byte of data is always sent on data lane 1. If 2 or more lanes are used, the second byte will be sent on data lane 2 and so on. If the number of bytes sent is not divisible by the number of lanes, any lanes without a byte to send at the final byte time will enter the EoT sequence.



• Figure 4 N-Lane D-PHY Byte Ordering

The MIPI transmitter supports various combination of input channel and output lanes provided the maximum output data rate is less than 1.2Gb/s. The minumum data rate should be at least 148Mb/s. An on-chip PLL generates all necessary clocks from a 27MHz crystal or clock input.

4.11 Power Management

The TP9950 can be put into power-down mode through software control.

4.12 Host Interface

The TP9950 registers are accessed via 2-WIRE serial interface that is compatible to standard I2C protocol. It operates as a slave device. Serial clock and data lines, SCL and SDA, transfer data from the bus master at a rate up to 400 Kbits/s. The TP9950 has one serial interface address select pin SAD to program up to two unique serial addresses. This allows TP9950 to share the same serial bus with other system components without address conflict.

Its device ID can be programmed though pin configuration based on following table.

Serial Bus Interface 7-bit Slave Address							Read/Write bit
1	0	0	0	1	0	SAD	1=Read 0=Write

5 Parametric Information

5.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
AVDD33 to Ground	-	**-0.5**	-	4.0	V
AVDD12 to Ground		**-0.5**	-	1.6	V
DVDD to Ground	-	**-0.5**	-	1.6	V
VDD_IO to Ground	-	**-0.5**	-	4.0	V
Digital Signal Input Pin to Ground	-	-0.5	-	VDD_IO+ 0.5	V
Analog Input Voltage	-	Ground – 0.5	-	1.92	V
Storage Temperature	T_S	–65	-	+150	°C
Junction Temperature	T_J	-	-	+125	°C

NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the ranges list in above table can induce destructive latch-up.

5.2 Recommended Operation Condition

5.2.1 Power Supply

Parameter	Symbol	Min	Typ	Max	Units
Power Supply — IO 3.3V/1.8V	VDD_IO	3.15/1.7	3.3/1.8	3.45/2.0	V
Power Supply — Analog 3.3V	AVDD33	3.15	3.3	3.45	V
Power Supply — Analog 1.2V	AVDD12	1.1	1.2	1.3	V
Power Supply — Digital	DVDD	1.1	1.2	1.3	V
Maximum $\|V_{DD\_IO} - AVDD\|$		-	-	0.3	V
Ambient Operating Temperature	T_A	-40		+85	°C

5.2.2 Reference Clock Input

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage (XTI)	V_{IH}	2.0	-	VDD_IO + 0.5	V
Input Low Voltage (XTI)	V_{IL}	-	-	0.8	V
Input Clock Frequency	Fclk		27		MHz
Crystal Spec					
Nominal frequency (fundamental)		-	27	-	MHz
Deviation base on normal operation condition		-50	-	+50	ppm

Load capacitance	CL	-	20	-	pF
Series resistor	RS	-	80	-	Ohm
Oscillator Input					
Nominal frequency		-	27	74.25	MHz
Deviation		-50	-	+50	ppm
Duty cycle		-	-	55	%

5.3 AC/DC Characteristic

5.3.1 Power Consumption

Parameter	Symbol	Min	Typ	Max	Units
Analog Supply current (3.3V)	Iaa3	-	24		mA
Analog supply current (1.2V)	Iaa12		60		mA
Digital I/O Supply current	Idde	-	9		mA
Digital Core Supply Current	Idd	-	140*/84**	-	mA

*1080p30 **720p and below

5.3.2 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0	-	-	V
Input Low Voltage (TTL)	V_{IL}	-	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	VDD_IO + 0.5	V
Input Low Voltage (XTI)	V_{IL}	-	-	0.8	V
Input High Current (V_{IN} =V_{DD})	I_{IH}	-	-	10	µA
Input Low Current (V_{IN} =VSS)	I_{IL}	-	-	–10	µA
Input Capacitance (f=1 MHz, V_{IN} =2.4 V)	C_{IN}	-	5	-	pF
Digital Outputs					
Output High Voltage (I_{OH} = –8 mA)	V_{OH}	2.4	-	VDD_IO	V
Output Low Voltage (I_{OL} = 8 mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	µA
Output Capacitance	C_O	-	5	-	pF

5.3.3 Analog Electrical Characteristics

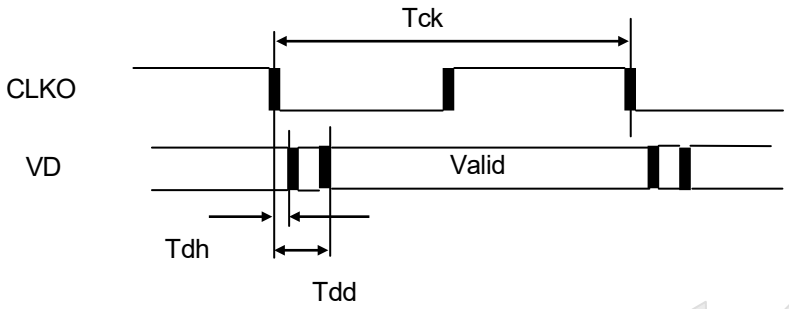
Parameter	Symbol	Min	Typ	Max	Units
Analog Input					
Analog Pin Input voltage	Vi	0.5	1	1.5	Vpp
Analog Pin Input Capacitance	C A	-	7	-	pF
ADCs					
ADC resolution	ADCR	-	10	-	bits
ADC integral Non-linearity	AINL	-	±1	-	LSB
ADC differential non-linearity	ADNL	-	±1	-	LSB
ADC clock rate	f_{ADC}	-	-	160	MHz
Video bandwidth (-3db)	BW	-	70	-	MHz

5.3.4 Decoder Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Horizontal PLL					
Line frequency	f_{LN}	15.625			KHz
static deviation	Δf_H	-	-	6.2	%
Vertical PLL					
Frame/Field frequency	f_{LN}	15		60	KHz
static deviation	Δf_H	-	-	5.5	%
Subcarrier PLL					
Lock in range (SPR=0) – HD 1080p, 720p60/50	Δf_{S-HD}	-		±4500	Hz
Lock in range (SPR=0) – HD 720p30/25	Δf_{S-HD}	-		±2200	Hz
Lock in range (SPR=2) - SD	Δf_{S-SD}	-		±800	Hz

5.3.5 Clocks, Data Timing

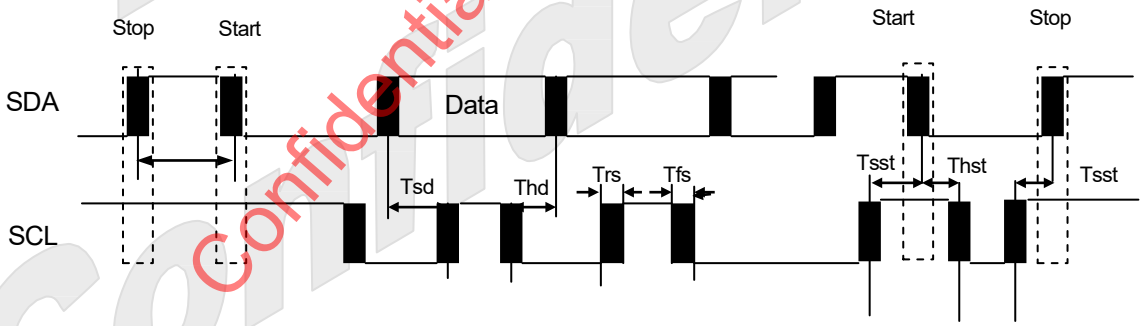
Parameter	Symbol	Min	Typ	Max	Units
Output CLKO					
Frequency	1/Tck	-		148.5	MHz
Duty Cycle		-	-	55	%
Rise/Fall time (12mA)		1	1.5		ns
CLKO (Falling Edge) to Data Delay @ 74.25MHz	Tdd	-	0.5	-	ns
CLKO (Falling Edge) to Data Delay @ 148.5MHz	Tdd	-	0	-	ns
Data hold time	Tdh	-	0	-	ns



5.3.6 Serial Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
Setup time for start/stop condition	Tsst	200			ns
Hold time for start / stop condition	Thst	200			ns
Data setup time (write)	Tsd	50			ns
Data hold time (write)	Thd(w)	150	-		ns
SCL, SDA rise time	Trs			1000 / 300*	ns
SCL, SDA fall time	Tfs			300	ns
SCL (Falling edge) to SDA delay time (read)	Thd(r)	150			ns
SCL clock frequency	fscl	-	100	400	KHz

* Fast (400KHz) mode



5.3.7 HS Transmitter DC Characteristics

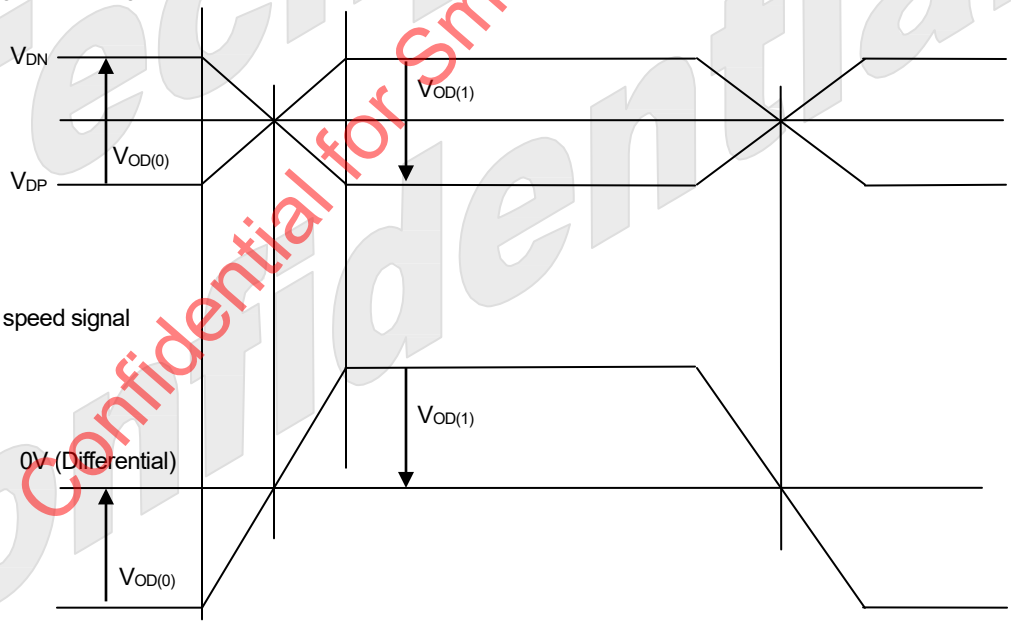
Parameter	Symbol	Min	Typ	Max	Units
HS transmit static common mode voltage 1*	VCMTX	150	200	250	mV
VCMTX mismatch when output is Differential-1 or Differnetial-0 2*	|ΔVcmtx(1,0)|			5	mV
HS transmit differential voltage 1*	|Vod|	140	200	270	mV
Vod mismatch when output is Differential-1 or Differential-0 1*	|ΔVod|			10	mV
HS output high voltage 1*	Vohhs			360	mV
Single-ended output impedance	Zos	40	50	62.5	Ω
Single-ended output impedance mismatch	ΔZos			10	%

Note:

1*. Value when driving into load impedance anywhere in the ZID range.

2*. A transmitter should minimize ΔVod and ΔVcmtx(1,0) in order to minimize radiation, and Optimize signal integrity.

Ideal Single-Ended High Speed Signals



Ideal Differential High speed signal

5.3.8 HS Transmitter AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Common-level variations above 450MHz	ΔVcmtx (HF)			15	mVrms
Common-level variations between 50-450MHz	ΔVcmtx (LF)			25	mVrms
Unit Interval Instantaneous	Ulinst		6.7340 3.3670 1.6835 0.8417		ns
UI Variation (UI≥1ns)	ΔUI	-10		10	%
Clock Lane DDR Clock Frequency (= 1/(2*Ulinst min)	fhmax		74.25 148.5 297 594		MHz
Data to Clock Skew (UI≥1ns)	Tskew	-0.15		0.15	Ulinst
20%-80% rise time and fall time	tr and tf			0.3	UI 1*, 2*
				0.35	UI 1*, 3*
		150			Ps 4*

Note: The frequency 'fh' is the highest fundamental frequency for data transmission

1*. UI is equal to 1/(2*fh).

2*. Applicable when supporting maximum HS bit rates ≤ 1Gbps(UI ≥ 1 ns).

3*. Applicable when supporting maximum HS bit rates > 1Gbps(UI<= 1 ns) but less than 1.5Gbps(UI=>0.667ns)

4*. Applicable when supporting maximum HS bit rates <= 1.5Gbps. However, to avoid excessive radiation, bit rates < 1Gbps (UI ≥ 1ns), should not use values below 150ps.

5.3.9 HS Transmitter AC Characteristics — Global Operation (continued)

Parameter	Symbol	Min	Typ	Max	Units
Time for the Data Lane receiver to enable the HS line termination	Td-term-en	Time for Dn to reach V-term-en		35 + 4 x Ulinst	ns
Transmitted time interval from the start of Ths-trail to the start of the LP-11 state to following a HS burst	Teot			105 + 12xUlinst	ns
Time that the transmitter drives LP=11 following a HS burst	Ths-exit	100			ns
Data Lane HS Entry	Ths-prepare	40 + 4xUlinst		85 + 6xUlinst	
Ths-prepare + time that the transmitter drives the HS-0 stat prior to transmitting the Sync sequence	Ths-prepare + Ths-zero	145 + 10xUlinst			ns
Time interval during which the HS receiver shall ignore any data Lane HS transitions, starting from the beginning of Ths-settle	Ths-settle	85 + 6xUlinst		145 + 10xUlinst	ns
Time interval during which the HS-RX should ignore any transitions on the data Lane, following a HS burst. He end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	Ths-skip	40		55 + 4xUlinst	ns
Data Lane HS Exit	Ths-trail	60 + 4xUlinst			ns
Transmitted length of LP state	Tlpx	50			ns
Recovery Time from Ultra Low Power State (ULPS)	Twakeup	1			ms

5.3.10 LP Transmitter DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Thevenin output high level 1*	Voh	1.1	1.2	1.3	V
Thevenin output low level	Vol	-50		50	mV
Output impedance of LP transmitter	Zolp	110			Ω

Note:

1*. Applicable when the supported data rate <= 1.5 Gbps.

5.3.11 LP Transmitter AC Characteristics

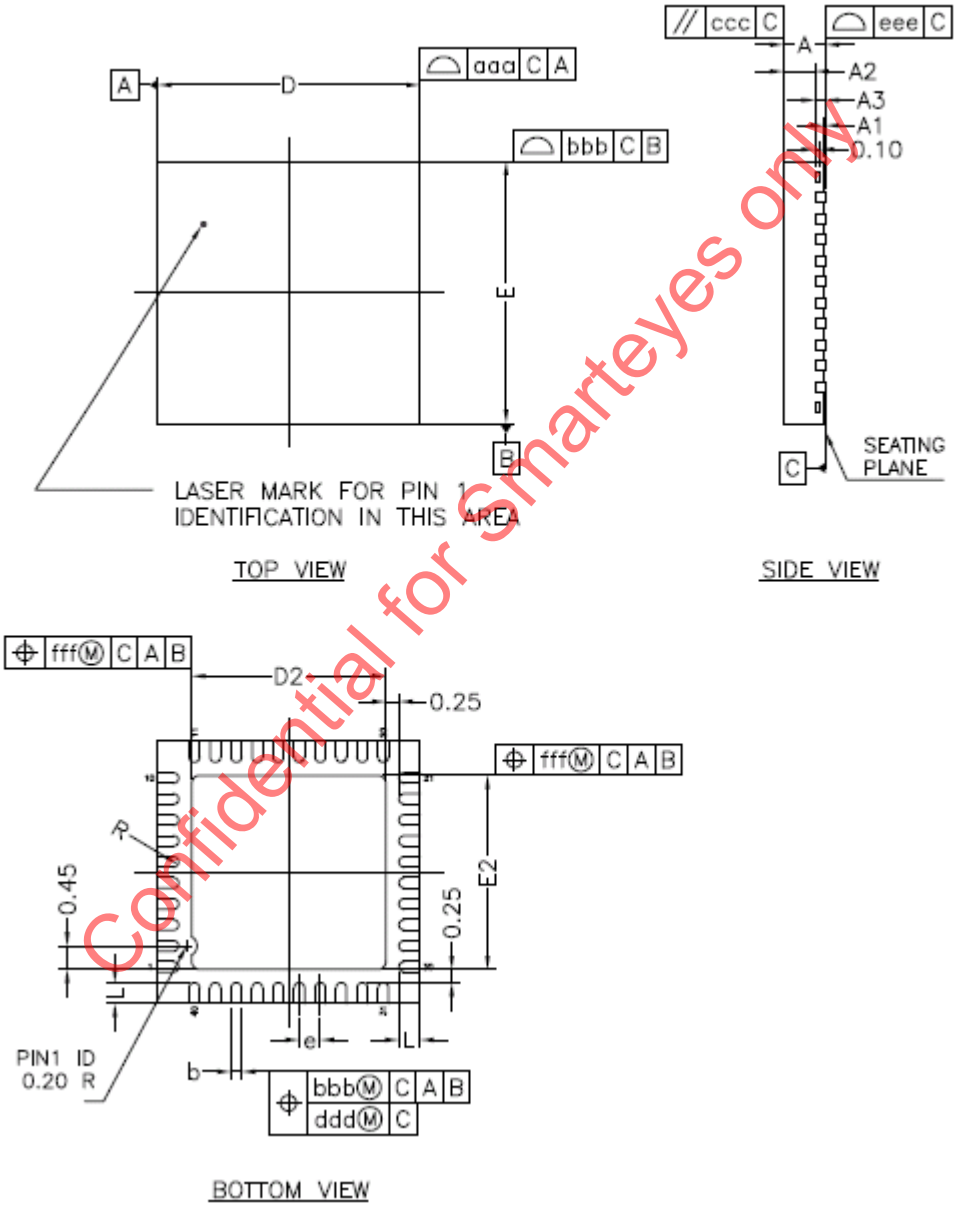
Parameter		Symbol	Min	Typ	Max	Units
15%-85% rise time and fall time 1*		Trlp/Tflp			25	ns
30% - 85% rise time and fall time Cload≤70pF		Treot			35	ns
Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	Tlp-pulse-tx	40			ns
	All other pulses		20			ns
Period of the LP exclusive-OR clock		Tlp-per-tx	90			ns
Slew rate @Cload = 0pF 1*		ΔV/Δtsr			500	mV/ns
Slew rate @Cload = 5pF 1*					300	
Slew rate @Cload = 20pF 1*					250	
Slew rate @Cload = 70pF 1*					150	
Slew rate @Cload = 0 to 70pF (Falling Edge Only)			30			
			25			
Slew rate @Cload = 0 to 70pF (Rising Edge Only)			30			
			25			
Load Capacitance 1*		Cload	0		70	pF

Note:

1*. Cload includes the low-frequenc equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distrited line capacitance can be up to 50pF for a transmission line with 2ns delay.

6 Mechanical Data

6.1 40 Pin QFN



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.80	---	---	0.031
A1	---	---	0.05	---	---	0.002
A2	---	0.53	0.58	---	0.021	0.023
A3	0.20 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	5.00 bsc			0.197 bsc		
D2	3.55	3.70	3.85	0.140	0.146	0.152
E	5.00 bsc			0.197 bsc		
E2	3.55	3.70	3.85	0.140	0.146	0.152
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 bsc			0.016 bsc		
R	0.075	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

7 Control Registers

7.1 TP9950 Register SUMMARY

* Following Index can be read/write accessible when MPAGE=0.

Index	7	6	5	4	3	2	1	0	Reset
00									11h
01	VDLOSS	VLOCK	HLOCK	SLOCK	VDET	EQDET	NINTL	CDET	-
02	MD1120	GMEN	OPLMT	F444	MD656	SD	P720	ITLC	C2h
03	EGAIN				SYWD	CVSTD			-
04	STATUS								-
05									00h
06	SRESET	-	-	CKPLVD	-	AGC_EN	AGCGAIN [8]	EQRST	32h
07	BPASS2	EQ_EN	EQGAIN						40h
08	AGCGAIN [7-0]								00h
09	MAXEN	DETEN	EQREF						24h
0A	MAXTH				EQHY				48h
0B	BPASS1	TL_EN	TFREQ	TLGAIN					40h
0C			EQSY	FSEL	TLHY				43h
0D	FLT	PBW	FS4	COMB	YCMB	SDSTD			50h
0E	-			CMCP					00h
0F	UOFFSET				VOFFSET				00h
10	-	BRIGHTNESS							00h
11	-	CONTRAST							40h
12	-	UVGAIN							40h
13	HUE								00h
14	HGM	NMD	SHARPNESS						00h
15	HDELAY [11-8]				AO	YDLY			13h
16	HDELAY [7-0]								15h
17	HACTIVE [7-0]								00h
18	VDELAY [7-0]								19h
19	VACTIVE [7-0]								D0h
1A	VACTIVE [11-8]				HACTIVE [11-8]				25h
1B	RDSEL				VSEL	VSEDG	VFLD2	HSE	00h
1C	YCM			NPXL [12-8]					06h
1D	NPXL [7-0]								72h
1E	HPXL								80h
1F	VLNN								80h

Index	7	6	5	4	3	2	1	0	Reset
20	PCLAMP								30h
21	WPGN				CLPGN				86h
22	SYHT								38h
23	CLMP								3Ch
24	-	FR	FMT		NMGN				04h
25	PKWT								FFh
26	CLEN	CKLY	GTST	SFLT	CBW		PSP	CLMD	05h
27	MP	UE	UG						2Dh
28	VLCKOUT		VLCKIN		VMODE	DETV	AFLD	VINT	00h
29	LOSSCNT				HSWIN				48h
2A	CKLM	CFQ			FCS	LCS	HPM		30h
2B	CKILLHY		CGAINMAX						4Ah
2C	FQEN	CHLOK	SPR		ACCT		SPM		0Ah
2D	PGATE								30h
2E	CGAINTH								70h
2F	TEST								00h
30	BFSTD [27-20]								48h
31	BFSTD [19-12]								BAh
32	BFSTD [11-4]								2Eh
33	BFSTD [3-0]				HS	HPRNG	FGAP		90h
34				CIDEN	CHID				00h
35	A135	DS2	FSL	VPM	-				05h
36	-								DCh
37	-								00h
38	CL_ISET	AFE_ISET			DIF_EN	DIFCM		IB_ISET	40h
39	LPF_VM	LPF_S2	EQ_SEL		LPF_SEL		VCOM_SEL		0Eh
3A	EQ1BP	EQ1FQ			EQ2BP	EQ2FQ			32h
3B	ADC_CTL								26h
3C									00h
3D	ADC_PD	T_PD_B	PD_CLP		PD_BUF	PD_LPF	PD_EQ	PDA	60h
3E	AFE_CTL				T_AFE			TO_EN	00h
3F	-								00h

Index	7	6	5	4	3	2	1	0	Reset
40					MPAGE				00h
41	DIAG_SEL		PTZ TEST	OENAFE	AIN_SEL				00h
4C	VSMUX		VSPOL	HSPOL	HSMUX		VSOE	HSOE	40h
4E		VD1DS	CK2DS	CK1DS		VD1OE	CK2OE	CK1OE	00h
4F			HSVSDS					IRQOE	00h
50	VD1X4	VD14SEL			VD1CT MD	VD13SEL			00h
54								VD1SWP	00h
B5				V1HIRQ				V1IRQ	00h
B6				V1RXIRQ				V1TXIRQ	00h
B7			STG1 IRQ	STG0 IRQ			STB1 IRQ	STB0 IRQ	00h
B9								HL1IRQ EN	00h
BA								VD100H	00h
BC						V1IRQMD			00h
BE	IRQCLR MD		IRQ EDGE	IRQPOL	SYS LOAD	MBIST			00h
E6				STG IRQEN				STB IRQEN	00h
E7	PWD_STB_A				STG_REF_A				13h
E8						STB_REF_A			03h
EF					STG_OUT_A		STB_OUT_A		00h
F0			PTZ_DRV_EN		STG_EN_A		STB_EN_A		00h
F3				CLKDLY					00h
F4	VCKRST	OCK148	PLL297					SYSCLK PD	20h
F5				VADCKP OL				SYSCLK 1MD	10h
F6		VD12SEL				VD11SEL			00h
FA					CLK POL	CLKMD			88h
FB				TSTIRQ	EXTCK	TEST_MODE			00h
FC	TESTO SWP	TEST OUT	TESTOUTSEL						00h
FD	SACNTN	BO4M	BOHM	BO7	REVISION				00h
FE	DEVICE_ID [15-8]								28h
FF	DEVICE_ID [7-0]								50h

* Following Index show Data register. These can be read/write accessible when MPAGE=0.

Index	7	6	5	4	3	2	1	0	Reset
55	TXDATA1 [47-40]								00h
56	TXDATA1 [39-32]								00h
57	TXDATA1 [31-24]								00h
58	TXDATA1 [23-16]								00h
59	TXDATA1 [15-8]								00h
5A	TXDATA1 [7-0]								00h
5B	TXDATA2 [47-40]								00h
5C	TXDATA2 [39-32]								00h
5D	TXDATA2 [31-24]								00h
5E	TXDATA2 [23-16]								00h
5F	TXDATA2 [15-8]								00h
60	TXDATA2 [7-0]								00h
61									00h
62	TXDATA3 [39-32]								00h
63	TXDATA3 [31-24]								00h
64	TXDATA3 [23-16]								00h
65	TXDATA3 [15-8]								00h
66	TXDATA3 [7-0]								00h
67									00h
68	TXDATA4 [39-32]								00h
69	TXDATA4 [31-24]								00h
6A	TXDATA4 [23-16]								00h
6B	TXDATA4 [15-8]								00h
6C	TXDATA4 [7-0]								00h
6D	CAP_TX								00h
6E	DAT_TX								00h
6F	TXMODE		TX PELCO2	TX PELCO1	TXDAH	TXACP	TXIRQ EN	TXEN	00h
70	TXDPOL	TXIRQ MD	TX 2BYTE	TXMFR	TXLMD	TXLNUM			00h
71	ST1P5	FIFO IRQEN		DCKEX	TXFLD		TXHST [11-10]		00h
72						TXDAHBIT			00h
8A	RXDATA1 [47-40]								00h
8B	RXDATA1 [39-32]								00h
8C	RXDATA1 [31-24]								00h
8D	RXDATA1 [23-16]								00h
8E	RXDATA1 [15-8]								00h
8F	RXDATA1 [7-0]								00h
90	RXDATA2 [47-40]								00h
91	RXDATA2 [39-32]								00h
92	RXDATA2 [31-24]								00h
93	RXDATA2 [23-16]								00h
94	RXDATA2 [15-8]								00h
95	RXDATA2 [7-0]								00h

Index	7	6	5	4	3	2	1	0	Reset
96	RXDATA3 [47-40]								00h
97	RXDATA3 [39-32]								00h
98	RXDATA3 [31-24]								00h
99	RXDATA3 [23-16]								00h
9A	RXDATA3 [15-8]								00h
9B	RXDATA3 [7-0]								00h
9C	RXDATA4 [47-40]								00h
9D	RXDATA4 [39-32]								00h
9E	RXDATA4 [31-24]								00h
9F	RXDATA4 [23-16]								00h
A0	RXDATA4 [15-8]								00h
A1	RXDATA4 [7-0]								00h
A2	CAP_RX								00h
A3	DAT_RX								00h
A4	RXL8 DET	RXL7 DET	RXL6 DET	RXL5 DET	RXL4 DET	RXL3 DET	RXL2 DET	RXL1 DET	00h
A7	RX IRQMD2	RX STFALL	RXPWM	RX PELCO	RXDAH	RXACP	RXIRQ EN	RXEN	00h
A8	RXDAHBNUM		RX 2BYTE	RXMFR	RXLMD	RXLNUM			40h
AE		RXL2 CRC3	RXL2 CRC2	RXL2 CRC1		RXL1 CRC3	RXL1 CRC2	RXL1 CRC1	00h
AF		RXL4 CRC3	RXL4 CRC2	RXL4 CRC1		RXL3 CRC3	RXL3 CRC2	RXL3 CRC1	00h
B0		RXL6 CRC3	RXL6 CRC2	RXL6 CRC1		RXL5 CRC3	RXL5 CRC2	RXL5 CRC1	00h
C0	TXLINE2 [11-8]				TXLINE1 [11-8]				00h
C1	TXLINE4 [11-8]				TXLINE3 [11-8]				00h
C2	TXLINE1 [7-0]								0Bh
C3	TXLINE2 [7-0]								0Ch
C4	TXLINE3 [7-0]								00h
C5	TXLINE4 [7-0]								00h
C6		TXBITCKNUM							1Fh
C7	TXHST [7-0]								78h
C8	TXHST [9-8]			TXBITNUM					27h
C9	RXLINE2 [11-8]				RXLINE1 [11-8]				00h
CA	RXLINE4 [11-8]				RXLINE3 [11-8]				00h
CB	RXLINE1 [7-0]								07h
CC	RXLINE2 [7-0]								08h
CD	RXLINE3 [7-0]								00h
CE	RXLINE4 [7-0]								00h

Index	7	6	5	4	3	2	1	0	Reset
CF		RXFREQ [22-16]							04h
D0	RXFREQ [15-8]								00h
D1	RXFREQ [7-0]								00h
D2	RXTHLEVEL								60h
D3	RXDET MD	RXHINUM							10h
D4			RXHST [9-8]		RXHEND [11-8]				06h
D5	RXHST [7-0]								BE
D6	RXHEND [7-0]								39h
D7			RXBITNUM						27h

* Following Index can be read/write accessible when MPAGE=1.

Index	7	6	5	4	3	2	1	0	Reset
00	PWD12 BG	ISEL			VBG SELB	IPSEL			44h
01	CKHS BUF1	CKHS BUF0	CKLPBUF		CKINV SEL	CKPH			F0h
02					CKHINV SER	CKINV SER	PWD12 CK	MIPI CKEN	00h
03		D_PH1				D_PH0			00h
04		D_PH3				D_PH2			00h
06	HSTX3 BUF1	HSTX2 BUF1	HSTX1 BUF1	HSTX0 BUF1	HSTX3 BUF0	HSTX2 BUF0	HSTX1 BUF0	HSTX0 BUF0	FFh
07	LPTXBUF3		LPTXBUF2		LPTXBUF1		LPTXBUF0		FFh
08	PWD_3	PWD_2	PWD_1	PWD_0	MIPIEN3	MIPIEN2	MIPIEN1	MIPIEN0	00h
09	MIPITEST1								00h
0A	MIPITEST2								00h
10	RST_PLL _REG	PWDPLL	DIV_FIN		LOCK_ ENB	LOCK_VREF			08h
11	DIV_PRE_FB			DIV_POST_FB					54h
12	BG_ SELB	ISEL			ICP_SEL				47h
13			OUT_DIV _EN	BYPASS _27M	DIV_OUT_PRE		DIV_OUT_POST		24h
14	RST_CL K_GEN	DIV_CLK_PIX			RST_PLL	DIV_CLK_PHY			04h
15			DIV_CLK_DEC		DIV_CLK_VC		DIV_CLK_BYT		00h
20		NUM_CHANNELS			PSFM	NUM_LANES			12h
21				FSWAIT [11-8]					00h
22	FSWAIT [7-0]								00h
23		SKIP_FR AMING	FRAME_ NUM_ ENA	YC16BIT	PCLK POL	TP_ENA	STOP _CLK	ULPM _CLK	20h
24	ULPM				CLKESC				00h
25	T_LPX								04h
26	T_PREP								06h
27	T_TRAIL								03h
28	T_WAKE								18h
31	HACTIVE_LN [15-8]								00h
32	HACTIVE_LN [7-0]								00h
33					RST _PHY	RST _CSI		RST _BTG	00h
34	CH4_VCI		CH3_VCI		CH2_VCI		CH1_VCI		E4h
35			FE_WAIT						15h
36							FE_ADJ		01h
37								OVERFL OW	00h
38								UNDERF LOW	00h
39								PCLKMD	00h

7.1.1 Reserved Register

Index	7	6	5	4	3	2	1	0	Reset
00									11h

7.1.2 Video Input Status Register

Index	7	6	5	4	3	2	1	0	Reset
01	VDLOSS	VLOCK	HLOCK	SLOCK	VDET	EQDET	NINTL	CDET	-

7 Video Loss

Sensitivity can be controlled by MISSCNT

0 = Video present

1 = Video loss

6 Vertical PLL Lock

0 = Not lock

1 = Lock

5 Horizontal PLL Lock

0 = Not lock

1 = Lock

4 Carrier PLL Lock

0 = Not lock

1 = Lock

3 Video Detect

0 = No video

1 = Video detected

2 EQ or 50Hz (SD mode) Detect

0 = None

1 = Detected or 50Hz (SD mode)

1 Interlaced Video

0 = Interlaced video

1 = Progressive video

0 CDET

0 = carrier detected

1 = No carrier detected

7.1.3 Decoding Control Register

Index	7	6	5	4	3	2	1	0	Reset
02	MD1120	GMEN	OPLMT	F444	MD656	SD	P720	ITLC	**C2h**

7 Output mode

0 = 16-bit

1 = 8-bit

6 Y/C order control for 8-bit mode. Not valid for 16-bit mode.

0 = Y first

1 = C first

5 Output limit

0 = 1-254

1 = Limit output range based on standard, i.e. Y=16-235, Cb/Cr=16-240.

4 F444

0 = Even pixel count (Default)

1 = Odd/Even count

3 MD656

0 = BT.1120 format, double-byte header

1 = BT.656 format output, single-byte header

2 SD mode

0 = HD mode

1 = SD mode only

1 P720

0 = 1080p decoding

1 = 720p decoding

0 ITLC

0 = Progressive mode decoding

1 = Interlace mode decoding

7.1.4 Detection Status Register

Index	7	6	5	4	3	2	1	0	Reset
03	EQGAIN				SYWD	CVSTD			-

This is read only register

7-4 EQGAIN

The current adaptive equalizer gain value

3 SYWD

0 = TVI v1.0

1 = TVI v2.0

2-0 CVSTD

The detected standard of current input video assuming the FSL setting matches the SYSCLK selection.

0 = 720p/60

1 = 720p/50

2 = 1080p/30

3 = 1080p/25

4 = 720p/30

5 = 720p/25

6 = SD

7 = Other formats

Note: The standard detection is for reference only. The accuracy may be affected by the current invoked decoding standard. It is recommended to confirm by setting the decoder accordingly.

7.1.5 Internal Status Register

Index	7	6	5	4	3	2	1	0	Reset
04	Device Internal status								-

7-0 Device Internal Status

The device internal status can be accessed through this register with the control of status control register 0x2F. Read-only register. For internal use.

7.1.6 Reserved Register

Index	7	6	5	4	3	2	1	0	Reset
05									00h

7-0 Reserved

7.1.7 Reset Control Register

Index	7	6	5	4	3	2	1	0	Reset
06	SRESET	-	-	CKPLVD	-	AGC_EN	AGCGAIN [8]	EQRST	32h

7 SRESET

Writing '1' to this bit performs soft reset of the logics but not affecting the register value. The bit is self-resetting after written.

6-5 Reserved

4 CKPLVD

0 = Non-inverted

1 = Inverted clock phase

3 Reserved

2 AGC_EN

0 = Automatic Gain Control (AGC) function is enabled (Default)

1 = AGC is disabled

1 AGCGAIN [8]

Bit 8 of the 9-bit Programmable Gain Amplifier (PGA) control

0 EQRST

Writing "1" to this bit resets the adaptive EQ to its original state. This bit is self-resetting after written.

7.1.8 EQ2 Control Register

Index	7	6	5	4	3	2	1	0	Reset
07	BPASS2	EQ_EN	EQGAIN						40h

7 BPASS2

1 = Analog EQ2 is used

0 = Factory function

6 EQ_EN

0 = Adaptive EQ2 is disabled

1 = Adaptive EQ2 is enabled (Default)

5-0 EQGAIN

This bits set the EQ2 gain value when the adaptive gain control loop is disabled.

7.1.9 PGA Gain Control Register

Index	7	6	5	4	3	2	1	0	Reset
06		-	-		-	AGC_EN	AGCGAIN [8]		32h
08	AGCGAIN [7-0]								00h

7-0 AGCGAIN [8-0]

A 9-bit PGA gain control value. It allows manual gain control when AGC function is disabled. The default value is 100h.

7.1.10 EQ2 Reference Register

Index	7	6	5	4	3	2	1	0	Reset
09	MAXEN	DETEN	EQREF						24h

7 MAXEN

0 Enable EQ limiter function

1 Disable

6 DETEN

0 Enable EQ detection function

1 Disable

5-0 These bits set the Equalizer gain control loop reference threshold. The default is 24h. The control loop refers this value for operation.

7.1.11 EQ2 Hysteresis Register

Index	7	6	5	4	3	2	1	0	Reset
0A	MAXTH				EQHY				48h

7-4 These bits set the threshold to control the EQ limiter function

3-0 These bits control the EQ adaptive loop decision hysteresis value.

7.1.12 EQ1 Control Register

Index	7	6	5	4	3	2	1	0	Reset
0B	BPASS1	TL_EN	TFREQ	TLGAIN					40h

7 BPASS1

1 = Analog EQ is used

0 = Internal Test function

6 TL_EN

0 = Adaptive EQ1 is disabled

1 = Adaptive EQ1 is enabled (Default)

5 TFREQ Frequency control

0 = High (Default)

1 = Low

4-0 TLGAIN

This bits set the EQ1 gain value when the adaptive gain control loop is disabled.

7.1.13 EQ1 Hysteresis Register

Index	7	6	5	4	3	2	1	0	Reset
0C			EQSY	FSEL	TLHY				43h

5 Sync EQ control

0 = Off (Default) 1 = On

4 EQ clock frequency control

0 = 148M 1 = 74M

3-0 These bits control the EQ adaptive loop decision hysteresis value.

7.1.14 Comb Filter and SD Format control Register

Index	7	6	5	4	3	2	1	0	Reset
0D	FLT	PBW	FS4	COMB	YCMB	SDSTD			50h

7 FLT, Use as recommended.

6 PBW, Comb filter control. Internal use only.

5 FS4. It is used with SD=1 and SDSTD to control the comb filter operation.

0 = SD mode only 1 = special HD mode

4 Comb filter control

0 = Off 1 = On (Default)

3 Y control

0 = High 1 = Low

2-0 These bits control the SD/HD decoding format

0 = NTSC-M (720p30)

1 = PAL-B (720p25)

2 = PAL-M (1080p30)

3 = PAL-N (1080p25)

4 = PAL-60

5 = NTSC 4.43

6, 7 = Not supported

7.1.15 CMCP Register

Index	7	6	5	4	3	2	1	0	Reset
0E				CMCP					00h

7-5 Reserved

4-0 CMCP. Use as recommended.

7.1.16 U/V Offset Control Register

Index	7	6	5	4	3	2	1	0	Reset
0F	UOFFSET				VOFFSET				00h

7-4 UOFFSET. U or Cb offset control in 2's complement format

3-0 VOFFSET. V or Cr offset control in 2's complement format

7.1.17 Brightness Control Register

Index	7	6	5	4	3	2	1	0	Reset
10		BRIGHTNESS							00h

7 Reserved

6-0 Brightness

This register controls the Brightness of the video by controlling the black level. It is in 2's complement format with a range of –64 to +63.

7.1.18 Contrast Control Register

Index	7	6	5	4	3	2	1	0	Reset
11		CONTRAST							40h

7 Reserved

6-0 CONTRAST. It provides up to 6dB of luma gain control. The default 0 dB gain value is 40h

7.1.19 Saturation Control Register

Index	7	6	5	4	3	2	1	0	Reset
12		UVGAIN							40h

7 Reserved

6-0 Saturation

It provides up to 6dB of color gain control. The default 0 dB gain value is 40h

7.1.20 Hue Control Register

Index	7	6	5	4	3	2	1	0	Reset
13	HUE								00h

7-0 Hue

This value is represented in 2's complement value for both positive (reddish) and negative (greenish) color tone control. It provides +- 90 degree of color shift at roughly 2.9 degree per step.

7.1.21 Sharpness Control Register

Index	7	6	5	4	3	2	1	0	Reset
14	HGM	NMD		SHARPNESS					00h

7 HGM. EQ control. Internal use only.

6-5 NMD. Special filter mode control. Use as recommended.

4-0 Sharpness

It provides 31 levels of sharpness control from 0 up to 9 dB gain. The sharpness has a center frequency of about 15MHz.

7.1.22 Y/C delay Control Register

Index	7	6	5	4	3	2	1	0	Reset
15	HDELAY [11-8]				AO	YDLY			13h

7 Reserved

6-4 H delay [11-8]

3 AO, Reserved

2-0 YDLY

These bits adjust the luma data delay relative to the chroma data for Y/C alignment. Larger value represents larger delay.

7.1.23 Output H-delay Control Register

Index	7	6	5	4	3	2	1	0	Reset
15	HDELAY [11-8]								13h
16	HDELAY [7-0]								15h

H Delay [11-0]

It sets the distance from the internal sync reference point to the start of the active video output. This 11-bit value is in 2's complement format to have a control –1024 to +1023 pixels.

7.1.24 Output H Active Control Register

Index	7	6	5	4	3	2	1	0	Reset
1A					HACTIVE [11-8]				25h
17	HACTIVE [7-0]								00h

H Active [11-0]

It sets the horizontal output length in number of output pixels. The active length for different standards is as follow.

720p = 1280d or 500h

1080p = 1920d or 780h

7.1.25 Output Vertical Delay Register

Index	7	6	5	4	3	2	1	0	Reset
18	VDELAY [7-0]								19h

7-0 The Vertical Delay register controls the starting line of the display output from the vertical sync.

7.1.26 Output Vertical Active Control Register

Index	7	6	5	4	3	2	1	0	Reset
1A		VACTIVE [11-8]							25h
19	VACTIVE [7-0]								D0h

V Active [11-0]

This is the 12-bit register that defines the number of active output lines per frame. The standard values are

720p – 720d or 2D0h

1080p – 1080d or 438h

7.1.27 Read Selection Control Register

Index	7	6	5	4	3	2	1	0	Reset
1B			RDSEL		VSEL	VSEDG	VFLD2	HSE	00h

3 VSEL

2 VSEDG, VS output alignment control with respect to HS output. 1 = leading edge 0 = falling edge

1 VFLD2, VS output position control of field 2

0 HSE, HS output trailing edge position control

7.1.28 NPXL Register

Index	7	6	5	4	3	2	1	0	Reset
1C	YCM			NPXL [12-8]					06h
1D	NPXL [7-0]								72h

NPXL[12-0], Number of Pixels per line

This register needs to be set correctly for each decoding standard as following table.

Npxl	720p/60	720p/50	720p/30	720p/25	1080p/30	1080p/25	480i	576i
Decimal	1650	1980	3300* / 1650**	3960* / 1980**	2200	2640	4720* / 2360**	4752* / 2376**
Hex	672	7BC	CE4* / 672**	F78* / 7BC**	898	A50	1270* / 938**	1290* / 948**

* 148.5MHz **74.25MHz

7 YCM, reserved for special mode. Used with FS4.

7.1.29 Read H Position Control Register

Index	7	6	5	4	3	2	1	0	Reset
1E	HPXL								80h

Reserved

7.1.30 Read V Position Control Register

Index	7	6	5	4	3	2	1	0	Reset
1F	VLNN								80h

Reserved

7.1.31 Clamp Position Control Register

Index	7	6	5	4	3	2	1	0	Reset
20	PCLAMP								30h

7-0 It controls the clamping position in number pixels relative to the internal sync reference. Factory recommended value should be used.

7.1.32 Clamping Gain Control Register

Index	7	6	5	4	3	2	1	0	Reset
21	WPGN				CLPGN				86h

7-4 White Peak Gain

It controls the white peak function loop speed. Use factory recommended value.

3-0 Clamp Gain

It controls the clamping loop gain and speed. Use factory recommended value.

7.1.33 Sync Amplitude AGC Control Register

Index	7	6	5	4	3	2	1	0	Reset
22	SYHT								38h

7-0 Sync Amplitude

It is used as the target sync amplitude value for AGC control. Default 38h should be used.

7.1.34 Clamping Level Control Register

Index	7	6	5	4	3	2	1	0	Reset
23	CLMP								3Ch

7-0 Clamping Level

It is used as the target clamping level for clamping control loop. Default of 3Ch should be used.

7.1.35 AGC Loop Gain Control Register

Index	7	6	5	4	3	2	1	0	Reset
24	-	FR	FMT		NMGN				04h

7 Reserved

6 FR (Reserved)

5-4 FMT (Reserved)

3-0 AGC loop gain

It controls the AGC loop gain and speed. Use default unless noted otherwise.

7.1.36 Peak White Control Register

Index	7	6	5	4	3	2	1	0	Reset
25	PKWT								FFh

7-0 Peak White Level

It sets the peak white detection level. The function can be disabled by setting value of FFh.

7.1.37 Clamping Control Register

Index	7	6	5	4	3	2	1	0	Reset
26	CLEN	CKLY	GTST	SFLT	CBW		PSP	CLMD	**05h**

7 Clamp Enable

0 = Enable (Default)

1 = Disable

6 Clamp Current Control

0 = 1X

1 = 2X

5 GTST

Internal use only. Default should be used.

4 SFLT, Sync filter bandwidth selection

0 = High (Default)

1 = Low.

3-2 CBW

Color bandwidth control for SD decoding. Internal use only.

1 PSP (Reserved)

0 Clamping control

1 = Normal mode 0 = Detection mode.

7.1.38 Reserved Register

Index	7	6	5	4	3	2	1	0	Reset
27	MP	UE	UG						**2Dh**

7-0 Reserved

7.1.39 Vertical Synchronization Control Register

Index	7	6	5	4	3	2	1	0	Reset
28	VLCKOUT		VLCKIN		VMODE	DETV	AFLD	VINT	00h

7-6 Vertical lock out count

Number of losing lock frames before the vertical PLL is locked out.

5-4 Vertical lock in count

Number of in-sync frames before the vertical PLL is locked in.

3 Vertical Synchronization mode

0 = Count down mode (Default)

1 = Continue search mode

2 DETV

0 = PLL is used to vertical synchronization (Default)

1 = Special synchronization mode not for normal use.

1 Reserved

0 Vertical Sync detection pulse width

0 = normal (Default)

1 = long (for SD input use)

7.1.40 Video Detection Control Register

Index	7	6	5	4	3	2	1	0	Reset
29	LOSSCNT				HSWIN				48h

7-4 Video Loss Count

These bits control the video loss detection sensitivity. Larger value has longer detection time.

3-0 HSWIN

Reserved

7.1.41 Color, H PLL and Free Run Control Register

Index	7	6	5	4	3	2	1	0	Reset
2A	CKLM	CFQ			FCS	LCS	HPM		30h

7 Color Killer Control

0 = Color killer enabled (Default)

1 = Color killer disabled

6-4 Color PLL lock detection threshold. For internal use only.

3 Force free run mode

0 = Disabled

1 = Forced free-run

2 Free run mode color control

0 = Normal input video data

1 = Blue screen

1-0 Horizontal PLL Control

0,1 = Normal operating mode (Default)

2,3h = special operating mode

7.1.42 Color Killer Threshold Control Register

Index	7	6	5	4	3	2	1	0	Reset
2B	CKILLHY		CGAINMAX						4Ah

7-6 Color Killer Hysteresis

Larger value represents larger hysteresis

5-0 Color Killer Threshold

It is implemented as color loop gain control. Larger value represents smaller color killer level. The default setting is for HD mode with EQ. It is recommended to set 70h for SD modes.

7.1.43 Color PLL Control Register

Index	7	6	5	4	3	2	1	0	Reset
2C	FQEN	CHLOK	SPR		ACCT		SPM		0Ah

7 Color Carrier Frequency Detection

0 = Disabled

1 = Enabled

*Should be 0 for best result.

6 Color PLL reset while H is not locked

0 = Disabled

1 = Enabled

5-4 Color PLL Pull-in Range Control (Follow factory recommendation)

0 = small (Default)

1 = Normal

2 = medium

3 = Wide

3-2 Color Gain Loop Speed Control

0 = Fixed gain

1 = slow

2 = medium (Default)

3 = fast

1-0 Color PLL Bandwidth

0 = Small

1 = Medium

2 = Normal

3 = Fast

7.1.44 Color Burst Gate Control Register

Index	7	6	5	4	3	2	1	0	Reset
2D	PGATE								30h

7-0 Color Burst Gate Position

These bits control the color burst gate position relative to the internal horizontal sync position. Set as directed.

7.1.45 Color Gain Reference Register

Index	7	6	5	4	3	2	1	0	Reset
2E	CGAINTH								70h

7-0 Color Gain Loop Reference

These bits define the color gain control loop reference value. Internal use only.

7.1.46 Test Register

Index	7	6	5	4	3	2	1	0	Reset
2F	TEST								00h

7-0 Reserved for debug use

7.1.47 Color Carrier DDS Control Register

Index	7	6	5	4	3	2	1	0	Reset
30	BFSTD [27-20]								48h
31	BFSTD [19-12]								BAh
32	BFSTD [11-4]								2Eh
33	BFSTD [3-0]				HS	HPRNG	FGAP		90h

27-0 BFSTD. For internal use only. Set as recommended.

3 HS, Horizontal PLL control for special operation. Set as recommended.

2 HPRNG, Horizontal PLL control. Use as recommended.

1-0 FGAP, These bits control the output for non-orthogonal sampling mode. Use as recommended. 0 is for normal mode.

7.1.48 CHID Control Register

Index	7	6	5	4	3	2	1	0	Reset
34				CIDEN	CHID				00h

7-5 Reserved Function.

4 CIDEN

1 = Enable 0 = Disable

3-0 CHID

Select one of 16 possible CHID

7.1.49 MISC Control Register

Index	7	6	5	4	3	2	1	0	Reset
35	A135	DS2	FSL	VPM					**05h**

7 A135 – Averaging. Reserved

6 DS2, special output mode

1 = Enable 0 = Disable

5 FSL

1 = status readouts reflect 74.25MHz system clock 0 = status reflects 148.5MHz system clock

4 Internal use

7.1.50 AFE Control Register

Index	7	6	5	4	3	2	1	0	Reset
38	CL_ISET	AFE_ISET			DIF_EN	DIFCM		IB_ISET	**40h**

7 CL_ISET, reserved.

6-4 AFE ISET, AFE current control

000 = 30uA (low power default)

001 = 35uA

010 = 40uA

011 = 45uA

100 = 50uA (default)

101 = 55uA

110 = 60uA

111 = 65uA

3 DIF_EN

0 = Single-end mode (Default)

1 = Differential mode

2-1 DIFCM, Common mode control for differential mode.

00, 01 = Disabled

10 = Enabled

11 = Enabled with double clamping strength

0 IB_ISET

0 = BG bias mode

1 = Vdd bias mode

7.1.51 LPF Control Register

Index	7	6	5	4	3	2	1	0	Reset
39	LPF_VM	LPF_S2	EQ_SEL		LPF_SEL		VCOM_SEL		0Eh

7 LPF_VM. It controls the LPF common mode. Use as recommended.

6 LPF_S2. It is the bit 2 of LPF_SEL [2-0].

5-4 EQ_SEL. These are for special EQ mode control.

0, 2 = normal EQ gain

1, 3 = boosted EQ gain

3-2 LPF_SEL

000: Bypass 001: 10MHz 010: 25MHz 011: 50MHz 100: 70MHz 110: 74MHz

1-0 VCOM_SEL

00 = 1.13V

01 = 1.02V

10 = 1.24V

11 = 1.33V

7.1.52 EQ Control Register

Index	7	6	5	4	3	2	1	0	Reset
3A	EQ1BP	EQ1FQ			EQ2BP	EQ2FQ			32h

7 EQ1 Bypass Control

1 = Bypass 0 = Enabled

6-4 EQ1 Response Control

000 = lowest corner frequency

…

111 = highest corner frequency

3 EQ2 Bypass Control

1 = Bypass 0 = Enabled

2-0 EQ2 Response Control

000 = lowest corner frequency

…

111 = highest corner frequency with 6dB additional mid gain.

7.1.53 ADC Control Register

Index	7	6	5	4	3	2	1	0	Reset
3B	ADC_CTL								26h

7 Analog test control

1 = ATST0 BIASP (0.8V), BIASN (0.4V)

0 = REFP (0.9V), Vcm (0.6V)

6-5

00 = Vcm=0.55V, V_fscale=0.89V (default)

01 = Vcm=0.58V, V_fscale=0.94V

10 = Vcm=0.55V, V_fscale=0.98V

11 = Vcm=0.65V, V_fscale=1.04V

4 Bandgap referenced biasing

0 = bandgap referenced

1= Vdd referenced biasing

3-2 ADC opamp bias current setting.

00 = current -40%

01 = -25%

10 = default

11 = current +25%

1-0 ADC global bias current setting.

00 = all -20%

01 = all current -10%

10 = default current

11 = all current +10%

7.1.54 Analog Power Down Control Register

Index	7	6	5	4	3	2	1	0	Reset
3D	ADC_PD	T_PD_B	PD_CLP		PD_BUF	PD_LPF	PD_EQ	PDA	60h

7 ADC Power Down
0 = Normal operation (Default)
1 = Power down

6 Test buffer PD
Reserved

5-4 Clamp Power Down
0 = Normal operation
1 = PD
2 = N/A

3 Buffer Power Down
Reserved

2 LPF Power Down
Reserved

1 EQ Power Down
Reserved

0 Analog Power Down
0 = Normal operation (Default)
1 = PD

7.1.55 Analog Test Control Register

Index	7	6	5	4	3	2	1	0	Reset
3E	AFE_CTL				T_AFE			TO_EN	00h

7-4 AFE_CTL

3-1 Test AFE
0 = Normal operation (Default)
1 = Test

0 Test Output Enable
0 = Enable (Default)
1 = Disable

7.1.56 Page Register

Index	7	6	5	4	3	2	1	0	Reset
40					MPAGE				00h

7-4 Reserved

3 MPAGE

0 = disable MIPI register access

1 = enable MIPI register access

2-0 Reserved

7.1.57 AFE Test Register

Index	7	6	5	4	3	2	1	0	Reset
41	DIAG_SEL		PTZ TEST	OENAFE	AIN_SEL				00h

7-5 DIAG_SEL. Diagnostic Input selection

0 = DIAG0

1 = DIAG1

2 = DIAG0/1

3 = N/A

5 PTZTEST

0 = normal operation

1 = IRQ input is used to Video AFE P_PTZ_OUTA/B/C/D input.Test purpose only.

4 OENAFE

Reserved

3-0 AIN_SEL. Input control

0 = VIN1

1 = VIN2

2 = VIN3

3 = VIN4

4 = N/A

5 = N/A

6 = Differential Input using VIN1P and VIN1N

7 = Differential Input using VIN2P and VIN2N

8-F = N/A

7.1.58 HS-VS output Selection Register

Index	7	6	5	4	3	2	1	0	Reset
4C	VSMUX		VSPOL	HSPOL	HSMUX		VSOE	HSOE	40h

7-6 VSMUX VS output signal select

0= HS

1= VS

2= FLD

3= DE

5 VSPOL

0 = VS signal polarity is not inversed

1 = VS signal polarity is inversed

4 HSPOL

0 = HS signal polarity is not inversed

1 = HS signal polarity is inversed

3-2 HSMUX HS output signal select

0= HS

1= VS

2= FLD

3= DE

1 VSOE

0 = VS pin output is tri-state

1 = VS pin output enable

0 HSOE

0 = HS pin output is tri-state

1 = HS pin output enable

7.1.59 Clock Data Pin Output Control Register

Index	7	6	5	4	3	2	1	0	Reset
4E		VD1DS	CK2DS	CK1DS		VD1OE	CK2OE	CK1OE	00h

7 Reserved

6 VD1DS

0 = VD1_7-0 pad is 8mA mode

1 = VD1_7-0 pad is 12mA mode

5 CK2DS

0 = CKN pad is 8mA mode

1 = CKN pad is 12mA mode

4 CK1DS

0 = CKP pad is 8mA mode

1 = CKP pad is 12mA mode

3 Reserved

2 V1DOE

0 = VD1_7-0 pin output tri-state (Default)

1 = VD1_7-0 pin output enable

1 CK2OE

0 = CKN pin output tri-state (Default)

1 = CKN pin output enable

0 CK1OE

0 = CKP pin output tri-state (Default)

1 = CKP pin output enable

7.1.60 IRQ pin Output Control Register

Index	7	6	5	4	3	2	1	0	Reset
4F			HSVSDS					IRQOE	00h

7-6 Reserved

5 HSVSDS

0 = HS/VS pad is 8mA mode

1 = HS/VS pad is 12mA mode

4-1 Reserved

0 IRQEN

0 = IRQ pin output tri-state

1 = IRQ pin output enable

7.1.61 4x Mux Video Data Selection Register

Index	7	6	5	4	3	2	1	0	Reset
50	VD1X4	VD14SEL				VD13SEL			00h

Reserved for internal use.

7 VD1X4

0 = none or 2 video data multiplexed mode.

1 = enable four video data multiplexed mode or

74.25MHz 2 video data multiplexed mode with PLL297=1

6-4 VD14SEL

These bits select the 4th video data source in channel multiplexed mode for VD1 bus, respectively.

0h = VIN1 Video Y (or 4:2:2 YCbCr) output data

4h = VIN1 Video C (CbCr) output data

3 Reserved

2-0 VD13SEL

These bits select the 3rd video data source in channel multiplexed mode for VD1 bus, respectively.

0h = VIN1 Video Y (or 4:2:2 YCbCr) output data

4h = VIN1 Video C (CbCr) output data

7.1.62 VD1 pin Output Control Register

Index	7	6	5	4	3	2	1	0	Reset
54								VD1SWP	00h

7-1 Reserved

0 VD1SWP

0 = VD1_7-0 pin output is video bus {bit7,bit6,bit5,bit4,bit3,bit2,bit1,bit0} order

1 = VD1_7-0 pin output is video bus {bit0,bit1,bit2,bit3,bit4,bit5,bit6,bit7} order

7.1.63 IRQ Length Register

Index	7	6	5	4	3	2	1	0	Reset
B3	IRQLEN								FAh

7-0 IRQLEN

When IRQEDGE=1, self-reset edge interrupt mode is used. This register determines the length of IRQ pin active period. IRQ pin output (IRQLEN+1) 74.25MHz/4 clock period active signal. If IRQLEN=00h, self-reset edge interrupt mode is disabled.

7.1.64 Video IRQ Status Register

Index	7	6	5	4	3	2	1	0	Reset
B5				V1HIRQ				V1IRQ	00h

All bits are reset to 0 after this index B5 register data are read when IRQCLRMD=1.These bits are read only when IRQCLRMD=1.

Each bit is reset to 0 after bit value 1 is written into each bit when IRQCLRMD=0.

When more than one bit of Index B5-B7 register are 1,IRQ pin output active state.

7-5 Reserved

4 V1HIRQ

0 = VIN HLOCK changed interrupt is not activated.

1 = VIN HLOCK changed interrupt is activated.

3-1 Reserved

0 V1IRQ

0 = VIN video lost/detect interrupt is not activated

1 = VIN video lost/detect interrupt is activated

7.1.65 Data IRQ Status Register

Index	7	6	5	4	3	2	1	0	Reset
B6				V1RXIRQ				V1TXIRQ	00h

All bits are reset to 0 after this index B6 register data are read when IRQCLRMD=1.These bits are read only when IRQCLRMD=1.

Each bit is reset to 0 after bit value 1 is written into each bit when IRQCLRMD=0.

When more than one bit of Index B5-B7 register are 1,IRQ pin output active state.

7-5 Reserved

4 V1RXIRQ

0 = VIN RX receive data interrupt is not activated

1 = VIN RX receive data interrupt is activated

3-1 Reserved

0 V1TXIRQ

0 = VIN TX transmit data interrupt is not activated

1 = VIN TX transmit data interrupt is activated

7.1.66 STG-STB IRQ Status Register

Index	7	6	5	4	3	2	1	0	Reset
B7			STG1 IRQ	STG0 IRQ			STB1 IRQ	STB0 IRQ	00h

All bits are reset to 0 after this index B7 register data are read when IRQCLRMD=1.These bits are read only when IRQCLRMD=1.

Each bit is reset to 0 after bit value 1 is written into each bit when IRQCLRMD=0.

When more than one bit of Index B5-B7 register are 1,IRQ pin output active state.

7-6 Reserved

5 STG1IRQ

0 = STG1 Short-to-Ground interrupt is not activated

1 = STG1 Short-to-Ground interrupt is activated

4 STG0IRQ

0 = STG0 Short-to-Ground interrupt is not activated

1 = STG0 Short-to-Ground interrupt is activated

3-2 Reserved

1 STB1IRQ

0 = STB1 Short-to-Battery interrupt is not activated

1 = STB1 Short-to-Battery interrupt is activated

0 STB0IRQ

0 = STB0 Short-to-Battery interrupt is not activated

1 = STB0 Short-to-Battery interrupt is activated

7.1.66 HLOCK IRQ Enable Control Register

Index	7	6	5	4	3	2	1	0	Reset
B9								HL1IRQ EN	00h

7-1 Reserved

0 HL1IRQEN

0 = Disable HLOCK status changed interrupt

1 = Enable HLOCK status changed interrupt

7.1.67 VD1_7-0 00h Output Control Register

Index	7	6	5	4	3	2	1	0	Reset
BA								VD100H	00h

7-1 Reserved

0 VD100H

0 = 8bit video output is normal clock operation

1 = 8bit video output is always 00h

7.1.68 Video Lost-Detect IRQ Control Register

Index	7	6	5	4	3	2	1	0	Reset
BC							V1IRQMD		00h

7-1 Reserved

1-0 V1IRQMD

0h = VIN Video Lost-Detect interrupt disabled

1h = the interrupt is generated when VIN input video status changes from detected to lost.

2h = the interrupt is generated when VIN input video status changes from lost to detected.

3h = the interrupt is generated when VIN input video status is changed.

7.1.69 IRQ Control Register

Index	7	6	5	4	3	2	1	0	Reset
BE	IRQCLRMD		IRQ EDGE	IRQPOL	SYSLOAD	MBIST			**00h**

7 IRQCLRMD

0 = Index B5/B6/B7 each IRQ bit is reset to 0 when bit value 1 is written in each bit.

1 = Index B5/B6/B7 data are reset to 00h when Index B5/B6/B7 data are read.

6 Reserved

5 IRQEDGE

0 = active state output and software IRQ clear mode.

When any IRQ status bit in index B5, B6 and B7 status register is set to 1, the IRQ pin continues output active status until all bits in B5, B6 and B7 registers are read (cleared).

1 = self reset edge interrupt mode.

When more than one bit in Index Index B5 Video IRQ Status Register and Index B6 Data IRQ Status Register and Index B7 STB-STG IRQ Status Register are set to 1, IRQ pin output active status for a period of time determined by the Index B3 IRQ Length register.

4 IRQPOL

0 = Low active interrupt output on IRQ pin (Default)

1 = High active interrupt output on IRQ pin

3 SYSLOAD

2 MBIST

0 = normal operation

1 = Memory BIST test mode. Test purpose only

1-0 Reserved

7.1.70 STG-STB IRQ Enable Control Register

Index	7	6	5	4	3	2	1	0	Reset
E6				STG IRQEN				STB IRQEN	00h

7-5 Reserved

4 STGIRQEN

0 = DIAG STG IRQ disable

1 = DIAG STG IRQ enable

3-1 Reserved

0 STBIRQEN

0 = DIAG STB IRQ disable

1 = DIAG STB IRQ enable

7.1.71 VIN STG Control Register

Index	7	6	5	4	3	2	1	0	Reset
E7			PWD_STB_A		STG_REF_A				13h

7-6 Reserved

5 PWD_STB_A. DIAG detection hysteresis control.

0 = default

1 = smaller

4 Reserved

3-0 STG_REF_A

7.1.72 VIN STB-HTA Control Register

Index	7	6	5	4	3	2	1	0	Reset
E8						STB_REF_A			03h

7-3 Reserved

2-0 STB_REF_A

7.1.73 VIN STB/STG Status Register

Index	7	6	5	4	3	2	1	0	Reset
EF					STG_OUT_A		STB_OUT_A		00h

7-4 Reserved

3-2 STG_OUT_A

Status of STGOUT[1-0]

1-0 STB_OUT_A

Status of STBOUT[1-0]

7.1.74 PTZ Drive Control Register

Index	7	6	5	4	3	2	1	0	Reset
F0			PTZ_DRV_EN		STG_EN_A		STB_EN_A		00h

7-6 Reserved

5-4 PTZ_DRV_EN[1-0] for [PTZ2,PTZ1]

0 = PTZ Drive disable

1 = PTZ Drive enable

3-2 STG_EN_A[1-0] for [DIAG2,DIAG1]

1-0 STB_EN_A[1-0] for [DIAG2,DIAG1]

7.1.75 Clock Output Delay Control Register

Index	7	6	5	4	3	2	1	0	Reset
F3					CLKDLY				00h

7-4 Reserved

3-0 CLKDLY

CKP/CKN pin output delay control.

00h is 0ns delay. +1 increment makes above 0.2ns more delay on CKP/CKN pin.

7.1.76 Video Clock Power Down Control Register

Index	7	6	5	4	3	2	1	0	Reset
F4	VCKRST	OCK148	PLL297					SYSCLK PD	20h

7 VCKRST

Writing '1' to this bit performs soft reset of video clock timing logics. The bit is self-resetting after written.

6 OCK148

0 = 148.5MHz clock output sync to rising edge of 297MHz clock.

1 = 148.5MHz clock output sync to falling edge of 297MHz clock.

5 PLL297

0 = reserved

1 = DDR 148.5MHz mode. PLL registers need to be set up for 297MHz output in this setting.

4-1 Reserved

0 SYSCLKPD

0 = VIN HDTV Decoder is in normal clock operation.

1 = VIN HDTV Decoder is in clock power down mode.

7.1.77 System Clock Control Register

Index	7	6	5	4	3	2	1	0	Reset
F5				VADCKPOL				SYSCLK MD	10h

7-5 Reserved

4 VADCKPOL

0 = Not inverse VIN ADC clock polarity

1 = Inverse VIN ADC clock polarity

3-1 Reserved

0 SYSCLKMD

0 = VIN HDTV Decoder system clock is 148.5MHz.

1 = VIN HDTV Decoder system clock is 74.25MHz.

7.1.78 Video Data Output Selection Register

Index	7	6	5	4	3	2	1	0	Reset
F6		VD12SEL				VD11SEL			00h

Reserved for internal use. Use default value for normal operation.

7 Reserved

6-4 VD12SEL

VD12SEL selects the 2nd data source to be output to VD1 bus

0h = VIN Video Y (or 4:2:2 YCbCr) output data

4h = VIN Video C (CbCr) output data

3 Reserved

2-0 VD11SEL

VD11SEL selects the first data to be output to VD1 bus

0h = VIN Video Y (or 4:2:2 YCbCr) output data

4h = VIN Video C (CbCr) output data

7.1.79 Clock Output Control Register

Index	7	6	5	4	3	2	1	0	Reset
FA					CLK POL		CLKMD		08h

7-4 Reserved

3 CLKPOL controls final CKP pin output polarity

0 = not inversed

1 = inversed

2-0 CLKMD controls CKP output

These registers select one of following clocks to be output

0h = 148.5MHz clock

1h = 74.25MHz clock sync to rising edge of 148.5MHz

2h = 74.25MHz clock sync to falling edge of 148.5MHz

3h = VIN VD1120CKO

7h = PLL CLK_DEC2X clock.Test purpose only.

7.1.80 Test Mode Register

Index	7	6	5	4	3	2	1	0	Reset

FB				TESTIRQ	EXTCK	TEST_MODE	00h

7-5 Reserved

4 TESTIRQ

0 = IRQ pin is normal operation

1 = IRQ pin output test signal TESTOUTSEL.Test purpose only

TESTOUTSEL	IRQ pin
00h	VDLOSS
01h	HLOCK
02h	EQDET
03h	VLOCK
04h	SLOCK
05h	NINTL
06h	MONO
07h	VDET
08h	TXD1
09h	STB_OUT_A[1]
0Ah	STB_OUT_A[0]
0Bh	STG_OUT_A[1]
0Ch	STG_OUT_A[0]
0Dh	PLLSYNC
0Eh	FLD
0Fh	CLKOUT

3 EXTCK

0 = normal 148.5MHz system clock mode with PLL module.(Default)

1 = XTI pin input becomes 148.5MHz system clock source

2-0 TEST_MODE

0 = normal operation mode. This value must be selected in normal operation.(Default)

1 = digital test mode 1

10bit digital test data can be input from [SAD,D1P,D1N,D0P,D0N,CKP,CKN,IRQ,HS,VS] pin

2 = digital test mode 2

10bit digital test data can be input from [VD1_5-2,D1P,D1N,D0P,D0N,CKP,CKN] pin

3 = reserved

4 = ADC test mode

10bit ADC data can be output to [VD1_7-0.HS,VS] pin

5 = clamp test mode.

Clamp control ports in AFE module have following pin input connection.

DN_CLAMPH = VD1_3

DN_CLAMPL = VD1_2

UP_CLAMPH = VD1_1

UP_CLAMPL = VD1_0

7.1.81 Test Data Output Selection Register

Index	7	6	5	4	3	2	1	0	Reset
FC	TESTO SWP	TEST OUT	TESTOUTSEL						00h

7 TESTOSWP This is test purpose only

0 = output test signal bit9-0 on [VD1_7,VD1_6,VD1_5,VD1_4,VD1_3,VD1_2,VD1_1,VD1_0,HS,VS]

1 = output test signal bit9-0 on [VS,HS,VD1_0,VD1_1,VD1_2,VD1_3,VD1_4,VD1_5,VD1_6,VD1_7]

6 TESTOUT

0 = normal operation (Default)

1 = Reserved for test purpose only

5-0 TESTOUTSEL

TESTOUTSEL	Bit9 (MSB) – Bit0 (LSB) [VD1_7,VD1_6,VD1_5,VD1_4,VD1_3,VD1_2,VD1_1,VD1_0,HS,VS]
00h	ADC9-0
01h	GVAL8-0,PLLSYNC
02h	HEQOUT9-0
03h	VDET,SLOCK,VCLOCK,HLOCK,VDLOSS,PLLSYNC, CLMPDNX,CLMPUPX,CLMPDN,CLMPUP
04h	VDET,SLOCK,VCLOCK,HLOCK,VDLOSS,PLLSYNC, FLD,NINTL,MONO,EQDET
05h	VDET,SLOCK,VCLOCK,HLOCK,VDLOSS,PLLSYNC, FLD,CVSTD
06h	STB1IRQ,STB0IRQ,STG1IRQ,STG0IRQ,RXIRQ,TXIRQ,VIRQ,3'h0
07h	VDYO
08h	VDCBO
09h	VDCRO
0Ah	VLDCYC,START_STOP,BIT_ACK,SDATO,SDATI,SCLK,RCOUNT

0Bh	RXLD,TXLD,ID_PHASE,SDATO,SDATI,SCLK,RCOUNT
0Ch	RXLD,TXLD,ID_PHASE,VLDCYC,START_STOP,BIT_ACK, SDATO,SDATI,SCLK,1'b0
0Dh	COMB4_TST_DONE,COMB4_FAIL_H,COM4_RST_L,COM4_TST_H, OUTIF_TST_DONE,OUTIF_FAIL_H, MBIST_TST_H,MBIST_RST_L,MBIST_CLK,1'b0
0Eh	STB1IRQ,STB0IRQ,STG1IRQ,STG0IRQ,TXD1,HS,4'h0
0Fh	LCNT[11-2]
10h	LCNT[9-0]
11h	STLCNT[11-2]
12h	STLCNT[9-0]
13h	HCT[11-2]
14h	HCT[9-0]
15h	STB_OUT_A,STG_OUT_A,6'h00

7.1.82 Revision Register

Index	7	6	5	4	3	2	1	0	Reset
FD	SACNTN	BO4M	BOHM	BO7	REVISION				00h

7 SACNTN

0 = normal SCL/SDA bus mode.(Default)

1 = test SCL/SDA bus mode. Test purpose only.

6 BO4M

Reserved for future use.

5 BOHM

Reserved for future use.

4 BO7

Reserved for future use.

3-0 REVISION.

These bits show the revision number of this chip. These bits are read only.

7.1.83 DEVICE_ID Register

Index	7	6	5	4	3	2	1	0	Reset
FE	DEVICE_ID [15-8]								28h

FF	DEVICE_ID [7-0]	50h

These registers are read only.

***Following show Data registers. These registers can be read/write accessible when MPAGE=0.**

7.1.84 Video Line 1 Transmit Data Register

Index	7	6	5	4	3	2	1	0	Reset
55	TXDATA1 [47-40]								00h
56	TXDATA1 [39-32]								00h
57	TXDATA1 [31-24]								00h
58	TXDATA1 [23-16]								00h
59	TXDATA1 [15-8]								00h
5A	TXDATA1 [7-0]								00h

47-0 TXDATA1

These register are effective when TXMFR=0.Sets first TX data line value to be transmitted. The MSB o any TX data value defined by TXBITNUM register must be 1. For example, in default 40bits transmi mode, TXDATA1 [39]=1 need to be set up if TXDATA1 is transmitted. If all TXDATA1 bits are 0 TXDATA1 transmit is disabled.

7.1.85 Video Line 2 Transmit Data Register

Index	7	6	5	4	3	2	1	0	Reset
5B	TXDATA2 [47-40]								00h
5C	TXDATA2 [39-32]								00h
5D	TXDATA2 [31-24]								00h
5E	TXDATA2 [23-16]								00h
5F	TXDATA2 [15-8]								00h
60	TXDATA2 [7-0]								00h

47-0 TXDATA2

These register are effective when TXMFR=0.Sets second TX data line value to be transmitted. The MSB of any TX data value defined by TXBITNUM register must be 1. For example, in default 40bits transmit mode, TXDATA2 [39]=1 need to be set up if TXDATA2 is transmitted. If all TXDATA2 bits are 0, TXDATA2 transmit is disabled.

7.1.86 Video Line 3 Transmit Data Register

Index	7	6	5	4	3	2	1	0	Reset
62	TXDATA3 [39-32]								00h
63	TXDATA3 [31-24]								00h
64	TXDATA3 [23-16]								00h
65	TXDATA3 [15-8]								00h
66	TXDATA3 [7-0]								00h

39-0 TXDATA3

These registers are effective when TXMFR=0.Sets third TX data line value to be transmitted. The MSB of any TX data value defined by TXBITNUM register must be 1. For example, in default 40bits transmit mode, TXDATA3 [39]=1 need to be set up if TXDATA3 is transmitted. If all TXDATA3 bits are 0, TXDATA3 transmit is disabled.

7.1.87 Video Line 4 Transmit Data Register

Index	7	6	5	4	3	2	1	0	Reset
68	TXDATA4 [39-32]								00h
69	TXDATA4 [31-24]								00h
6A	TXDATA4 [23-16]								00h
6B	TXDATA4 [15-8]								00h
6C	TXDATA4 [7-0]								00h

39-0 TXDATA4

These registers are effective when TXMFR=0.Sets fourth TX data line value to be transmitted. The MSB of any TX data value defined by TXBITNUM register must be 1. For example, in default 40bits transmit mode, TXDATA4 [39]=1 need to be set up if TXDATA4 is transmitted. If all TXDATA4 bits are 0, TXDATA4 transmit is disabled.

7.1.88 Transmit Data FIFO Status Register

Index	7	6	5	4	3	2	1	0	Reset
6D	CAP_TX								00h

7-0 CAP_TX

This register is effective when TXMFR=1.This register shows the number of TX data bytes stored in Transmit Data FIFO. Transmit Data FIFO can have up to 16 data bytes per one time. When software write one data byte in DAT_TX register, the value of CAP_TX is incremented. When TX transmit logic is read first-in first-out data byte in Transmit Data FIFO, the value of CAP_TX is decremented.

7.1.89 Transmit Data FIFO Write Register

Index	7	6	5	4	3	2	1	0	Reset
6E	DAT_TX								00h

7-0 DAT_TX

This register is effective when TXMFR=1.When software write one data byte in this index register, that one data byte is stored in Transmit Data FIFO by first-in first-out byte order. When software reac DAT_TX, the value of this register shows the value of next first-out data byte to be read by TX transmit logic.

7.1.90 TX Control Register

Index	7	6	5	4	3	2	1	0	Reset
6F	TXMODE		TX PELCO2	TX PELCO1	TXDAH	TXACP	TXIRQ EN	TXEN	00h

7 TXMODE

0 = VINn TX data is transferred only once after TXEN=0 at first and TXEN=1 at next

1 = The value of Transmit Data Register is transferred per each frame when TXEN=1.

6 Reserved.

5-2

(1)TXDAH=0 mode with TXMFR=0,TXLMD=0

REGISTERS	TP MODE TECHPOINT TVI GENERAL	PELCO1 MODE PELCO FIRST EXPANSION EXTENDED 15 BIT COAXITRON	PELCO2 MODE PELCO SECOND EXPANSION 32 BIT COAXITRON	ACP MODE HD ACP COAXITRON
TXPELCO2	0	0	1	0
TXPELCO1	0	1	0	0
TXDAH	0	0	0	0
TXACP	0	0	0	1
TXLINE1	Bh	Fh	Fh	11h
TXLINE2	Ch	0h	10h	12h
TXLINE3	Dh for 4 line mode 0h for 2 line mode	0h	0h	13h for 4 line mode 0h for 2 line mode
TXLINE4	Eh for 4 line mode 0h for 2 line mode	0h	0h	14h for 4 line mode 0h for 2 line mode
TXBITCKNUM	1Fh	49h	49h	24h
TXBITNUM	27h	2Ch	2Fh	17h
TXHST	78h for TVI 1.0 DFh for TVI 2.0	214h	214h	215h

TP MODE transmission bit order is MSB at first and bit0 last.

TXDATAn [MSB], TXDATAn [MSB-1]…TXDATAn [1], TXDATAn [0]

In PELCO1, PELCO2 and ACP MODE, one unit data is START, DATA, STOP 3 bit encoding.

START	DATA	STOP
1	TXDATAn[x]	0

TXDATAn [x] is transmitted with START DATA STOP format from TXDATAn LSB bit0 at first.

PELCO1 MODE transmission bit setup and transmission bit order.

Set up TXDATA1 [14:0]

TXDATA1 [0], TXDATA1 [1]…TXDATA1 [13], TXDATA1 [14]

PELCO2 MODE transmission bit setup and transmission bit order.

Set up TXDATA1 [15:0] and TXDATA2 [15:0]

TXDATAn [0], TXDATAn [1]…TXDATAn [14], TXDATAn [15]

ACP MODE transmission bit setup and transmission bit order.

Set up TXDATA1 [7:0], TXDATA2 [7:0], TXDATA3 [7:0] and TXDATA4 [7:0]

TXDATAn [0], TXDATAn [1]…TXDATAn [6], TXDATAn [7]

(2)TXDAH=1 mode

REGISTERS	HDCVI MODE
TXPELCO2	0
TXPELCO1	0
TXDAH	1
TXACP	0
TXLMD	1
TXLNUM	5
TXLINE1	10h
TXBITCKNUM	15h
TXBITNUM	17h
TXHST	25Bh

1 TXIRQEN

0 = Disable VIN TX transmit data interrupt

1 = Enable VIN TX transmit data interrupt

0 TXEN

0 = Disable VIN TX data transfer.

1 = Enable VIN TX data transfer.

7.1.91 TX Multi Frame Control Register

Index	7	6	5	4	3	2	1	0	Reset
70	TXDPOL	TXIRQ MD	TX 2BYTE	TXMFR	TXLMD	TXLNUM			00h

7 TXDPOL TXD1 signal polarity control

0 = not inverse TXD1 signal polarity

1 = inverse TXD1 signal polarity

6 TXIRQMD

0 = VIN TX data interrupt is generated only once when VIN TX data transfer.

1 = VIN TX data interrupt is generated per each frame when VIN TX data transfer.

5 TX2BYTE

0 = 1 data byte transfer when TXDAH=1 or TXACP=1

1 = 2 data bytes transfer when TXDAH=1 or TXPELCO1=1 or TXPELCO2=1

4 TXMFR

0 = TX data transfer is non multi frame transfer (Default)

1= TX data transfer is multi frame transfer with Transmit Data FIFO control by CAP_TX and DAT_TX.

3-0 TXLMD=0 mode. Independent TX 4 line control

Register TXLINE1, TXLINE2, TXLINE3 and TXLINE4 decide any TX data transfer line.

TXLMD=1 mode. Continuous start line to end line control

TX start line number is TXLINE1.TX end line number is TXLINE1 + TXLNUM.In this mode,all lines from start line number to end line number are all TX data transfer active line.

7.1.92 TX Field Control Register

Index	7	6	5	4	3	2	1	0	Reset
71	ST1P5	FIFO IRQEN		DCKEX	TXFLD		TXHST [11-10]		00h

7 ST1P5

0 = start bit is normal 1bit 1

1 = start bit is 1 bit 1 and 0.5bit 0

6 FIFOIRQEN

0 = disable DAT_TX FIFO IRQ

1 = enable DAT_TX FIFO IRQ

5 Reserved

4 DCKEX

0 = Data clock enable is controlled by only SYSCLKMD.This is original mode.

1 = Data clock enable is expanded in SYSCLKMD=1.This is optional mode.

3-2 VIN TX field control in SD video mode

0,3 = transmit TX data in both field1 (odd) and field2 (even)

1 = transmit TX data in only field1 (odd)

2 = transmit TX data in only field2 (even)

1-0 TXHST [11-10]

TX H start register bit11-10.

7.1.93 TXDAHBIT Register

Index	7	6	5	4	3	2	1	0	Reset
72						TXDAHBIT			00h

7-3 Reserved

2-0 TXDAHBIT

Number of bits per line when TXDAH=1 (CVI) mode is enable.

0 = 32bits

1 = 24bits

2 = 21bits

3 = 18bits

4 = 16bits

7.1.94 RX Line 1 Data Register

Index	7	6	5	4	3	2	1	0	Reset
8A	RXDATA1 [47-40]								00h
8B	RXDATA1 [39-32]								00h
8C	RXDATA1 [31-24]								00h
8D	RXDATA1 [23-16]								00h
8E	RXDATA1 [15-8]								00h
8F	RXDATA1 [7-0]								00h

47-0 RXDATA1

These registers are effective when RXMFR=0.RX data received on the vertical line RXLINE1 can be read out from these registers.

7.1.95 RX Line 2 Data Register

Index	7	6	5	4	3	2	1	0	Reset
90	RXDATA2 [47-40]								00h
91	RXDATA2 [39-32]								00h
92	RXDATA2 [31-24]								00h
93	RXDATA2 [23-16]								00h
94	RXDATA2 [15-8]								00h
95	RXDATA2 [7-0]								00h

47-0 RXDATA2

These registers are effective when RXMFR=0.RX data received on the vertical line RXLINE2 can be read out from these registers.

7.1.96 RX Line 3 Data Register

Index	7	6	5	4	3	2	1	0	Reset
96	RXDATA3 [47-40]								00h
97	RXDATA3 [39-32]								00h
98	RXDATA3 [31-24]								00h
99	RXDATA3 [23-16]								00h
9A	RXDATA3 [15-8]								00h
9B	RXDATA3 [7-0]								00h

47-0 RXDATA3

These registers are effective when RXMFR=0.RX data received on the vertical line RXLINE3 can be read out from these registers.

7.1.97 RX Line 4 Data Register

Index	7	6	5	4	3	2	1	0	Reset
9C	RXDATA4 [47-40]								00h
9D	RXDATA4 [39-32]								00h
9E	RXDATA4 [31-24]								00h
9F	RXDATA4 [23-16]								00h
A0	RXDATA4 [15-8]								00h
A1	RXDATA4 [7-0]								00h

47-0 RXDATA4

These registers are effective when RXMFR=0.RX data received on the vertical line RXLINE4 can be read out from these registers.

7.1.98 RX Data FIFO Status Register

Index	7	6	5	4	3	2	1	0	Reset
A2	CAP_RX								00h

7-0 CAP_RX

This register is effective when RXMFR=1.This register shows the number of data bytes stored in RX Data FIFO. When RX logic store new received one data byte, this register value is incremented. Wher software read DAT_RX RX Data FIFO register, this register value is decremented.

7.1.99 RX Data FIFO Register

Index	7	6	5	4	3	2	1	0	Reset
A3	DAT_RX								00h

7-0 DAT_RX

This register is effective when RXMFR=1.This register shows the value of new RX data byte stored in RX Data FIFO by first-in first-out order after RX logic received new RX data byte.

7.1.100 RXLINE Status Register

Index	7	6	5	4	3	2	1	0	Reset
A4	RXL8 DET	RXL7 DET	RXL6 DET	RXL5 DET	RXL4 DET	RXL3 DET	RXL2 DET	RXL1 DET	00h

These registers are read only. Bit4-7 are effective when RXMFR=1,RXLMD=1 and RXLNUM=7.

7 RXL8DET

0 = Data is not received in 8th RXLINE.

1 = Data is received in 8th RXLINE.

6 RXL7DET

0 = Data is not received in 7th RXLINE.

1 = Data is received in 7th RXLINE.

5 RXL6DET

0 = Data is not received in 6th RXLINE.

1 = Data is received in 6th RXLINE.

4 RXL5DET

0 = Data is not received in 5th RXLINE.

1 = Data is received in 5th RXLINE.

3 RXL4DET

0 = Data is not received in 4th RXLINE.

1 = Data is received in 4th RXLINE.

2 RXL3DET

0 = Data is not received in 3rd RXLINE.

1 = Data is received in 3rd RXLINE.

1 RXL2DET

0 = Data is not received in 2nd RXLINE.

1 = Data is received in 2nd RXLINE.

0 RXL1DET

0 = Data is not received in 1st RXLINE.

1 = Data is received in 1st RXLINE.

7.1.101 RX Control Register

Index	7	6	5	4	3	2	1	0	Reset
A7	RX IRQMD2	RX STFALL	RXPWM	RX PELCO	RXDAH	RXACP	RXIRQ EN	RXEN	00h

7 RXIRQMD2

0 = Disable RXIRQMD2

1 = RXIRQ is generated when RX detection counter has more than 1 value.

6 RXSTFALL

0 = RX data bits are received from first rising edge

1 = RX data bits are received from first falling edge

5 RXPWM

0 = Disable PWM Pulse Width modulation receive mode

1 = Enable PWM Pulse Width modulation receive mode for RXPECLO and RXACP

4-2

REGISTERS	TP MODE TECHPOINT TVI RX	HDCVI RX MODE	PELCO RX MODE	ACP RX MODE
RXPELCO	0	0	1	0
RXDAH	0	1	0	0
RXACP	0	0	0	1

1 RXIRQEN

0 = Disable VIN RX receive data interrupt

1 = Enable VIN RX receive data interrupt

0 RXEN

0 = Disable VIN RX data receive

1 = Enable VIN RX data receive

7.1.102 RX Multi Frame Control Register

Index	7	6	5	4	3	2	1	0	Reset
A8	RXDAHBNUM		RX 2BYTE	RXMFR	RXLMD	RXLNUM			40h

7-6 RXDAHBNUM

Number of byte per line when RXDAH=1 (CVI) mode is enable

0 = 1 byte 1 = 2 byte 2 = 3 byte

5 RX2BYTE

0 = 1 data byte receive per line when RXDAH=1 or RXACP=1

1 = 2 data bytes receive per line when RXDAH=1 or RXPELCO=1

4 RXMFR

0 = RX data receive is non multi frame receive(Default)

1 = RX data receive is multi frame receive with Receive Data FIFO control by CAP_RX and DAT_RX.

3-0 RXLMD=0 mode. Independent RX 4 line control

Register RXLINE1, RXLINE2, RXLINE3 and RXLINE4 decide any RX data receive line.

RXLMD=1 mode. Continuous start line to end line control

RX start line number is RXLINE1.RX end line number is RXLINE1 + RXLNUM. In this mode, all lines from start line number to end line number are all RX data receive active line.

7.1.103 RX Line1-2 CRC Status Register

Index	7	6	5	4	3	2	1	0	Reset
AE		RXL2 CRC3	RXL2 CRC2	RXL2 CRC1		RXL1 CRC3	RXL1 CRC2	RXL1 CRC1	00h

These registers are read only. These registers are effective when RXDAH=1.

7 Reserved

6 RXL2CRC3

This bit shows third byte CRC value in 2ND RXLINE

5 RXL2CRC2

This bit shows second byte CRC value in 2ND RXLINE

4 RXL2CRC1

This bit shows first byte CRC value in 2ND RXLINE

3 Reserved

2 RXL1CRC3

This bit shows third byte CRC value in 1ST RXLINE

1 RXL1CRC2

This bit shows second byte CRC value in 1ST RXLINE

0 RXL1CRC1

This bit shows first byte CRC value in 1ST RXLINE

7.1.104 RX Line3-4 CRC Status Register

Index	7	6	5	4	3	2	1	0	Reset
AF		RXL4 CRC3	RXL4 CRC2	RXL4 CRC1		RXL3 CRC3	RXL3 CRC2	RXL3 CRC1	00h

These registers are read only. These registers are effective when RXDAH=1.

7 Reserved

6 RXL4CRC3

This bit shows third byte CRC value in 4TH RXLINE

5 RXL4CRC2

This bit shows second byte CRC value in 4TH RXLINE

4 RXL4CRC1

This bit shows first byte CRC value in 4TH RXLINE

3 Reserved

2 RXL3CRC3

This bit shows third byte CRC value in 3RD RXLINE

1 RXL3CRC2

This bit shows second byte CRC value in 3RD RXLINE

0 RXL3CRC1

This bit shows first byte CRC value in 3RD RXLINE

7.1.105 RX Line5-6 CRC Status Register

Index	7	6	5	4	3	2	1	0	Reset
B0		RXL6 CRC3	RXL6 CRC2	RXL6 CRC1		RXL5 CRC3	RXL5 CRC2	RXL5 CRC1	00h

These registers are read only. These registers are effective when RXDAH=1.

7 Reserved

6 RXL6CRC3

This bit shows third byte CRC value in 6TH RXLINE

5 RXL6CRC2

This bit shows second byte CRC value in 6TH RXLINE

4 RXL6CRC1

This bit shows first byte CRC value in 6TH RXLINE

3 Reserved

2 RXL5CRC3

This bit shows third byte CRC value in 5TH RXLINE

1 RXL5CRC2

This bit shows second byte CRC value in 5TH RXLINE

0 RXL5CRC1

This bit shows first byte CRC value in 5TH RXLINE

7.1.106 TX Data Line 1 Control Register

Index	7	6	5	4	3	2	1	0	Reset
C0					TXLINE1 [11-8]				00h
C2	TXLINE1 [7-0]								0Bh

11-0 TXLINE1

Set up first TX transmitting data line number.

If 000h is set up, this line doesn't execute TX function.

7.1.107 TX Data Line 2 Control Register

Index	7	6	5	4	3	2	1	0	Reset
C0	TXLINE2 [11-8]								00h
C3	TXLINE2 [7-0]								0Ch

11-0 TXLINE2

This register is effective when TXLMD=0.Set up second TX transmitting data line number.

If 000h is set up, this line doesn't execute TX function.

7.1.108 TX Data Line 3 Control Register

Index	7	6	5	4	3	2	1	0	Reset
C1					TXLINE3 [11-8]				00h
C4	TXLINE3 [7-0]								00h

11-0 TXLINE3

This register is effective when TXLMD=0.Set up third TX transmitting data line number.

If 000h is set up, this line doesn't execute TX function.

7.1.109 TX Data Line 4 Control Register

Index	7	6	5	4	3	2	1	0	Reset
C1	TXLINE4 [11-8]								00h
C5	TXLINE4 [7-0]								00h

11-0 TXLINE4

This register is effective when TXLMD=0.Set up 4th TX transmitting data line number.

If 000h is set up, this line doesn't execute TX function.

7.1.110 TX Data Bit Clock Number Register

Index	7	6	5	4	3	2	1	0	Reset
C6		TXBITCKNUM							1Fh

7 Reserved

6-0 TXBITCKNUM

(TXBITCKNUM+1) shows the number of 74.25MHz clocks per one data bit for VIN.

7.1.111 TX Data H Start Control Register

Index	7	6	5	4	3	2	1	0	Reset
71							TXHST [11-10]		00h
C7	TXHST [7-0]								78h
C8	TXHST [9-8]								27h

11-0 TXHST [11-0]

It controls the VIN TX transmit data horizontal start position.

7.1.112 TX Data Bit Number Register

Index	7	6	5	4	3	2	1	0	Reset
C8			TXBITNUM						27h

5-0 TXBITNUM

(TXBITNUM+1) shows the number of data bit including first start bit 1 per line for VIN.

7.1.113 RX Data Line 1 Control Register

Index	7	6	5	4	3	2	1	0	Reset
C9					RXLINE1 [11-8]				00h
CB	RXLINE1 [7-0]								07h

11-0 RXLINE1

Set up vertical line number to receive first line RX data for VIN.

If 000h is set up, this line doesn't execute RX function.

7.1.114 RX Data Line 2 Control Register

Index	7	6	5	4	3	2	1	0	Reset
C9	RXLINE2 [11-8]								00h
CC	RXLINE2 [7-0]								08h

11-0 RXLINE2

This register is effective when RXLMD=0.Set up vertical line number to receive second line RX data for VIN. If 000h is set up, this line doesn't execute RX function.

7.1.115 RX Data Line 3 Control Register

Index	7	6	5	4	3	2	1	0	Reset
CA					RXLINE3 [11-8]				00h
CD	RXLINE3 [7-0]								00h

11-0 RXLINE3

This register is effective when RXLMD=0.Set up vertical line number to receive third line RX data for VIN. If 000h is set up, this line doesn't execute RX function.

7.1.116 RX Data Line 4 Control Register

Index	7	6	5	4	3	2	1	0	Reset
CA	RXLINE4 [11-8]								00h
CE	RXLINE4 [7-0]								00h

11-0 RXLINE4

This register is effective when RXLMD=0.Set up vertical line number to receive 4th line RX data for VIN. If 000h is set up, this line doesn't execute RX function.

7.1.117 RX Bit Frequency Register

Index	7	6	5	4	3	2	1	0	Reset
CF		RXFREQ [22-16]							04h
D0	RXFREQ [15-8]								00h
D1	RXFREQ [7-0]								00h

22-0 RXFREQ

VIN RX data bit frequency control

2 ^23 / 32 =23'h040000 (Default)

Default bit frequency for RX receiving data is 74.25MHz/32=2.3203125MHz.

7.1.118 RX Data Threshold Register

Index	7	6	5	4	3	2	1	0	Reset
D2	RXTHLEVEL								60h

7-0 RXTHLEVEL

Define RX receiving data threshold level for VIN

7.1.119 RX High Detection Control Register

Index	7	6	5	4	3	2	1	0	Reset
D3	RXDETMD	RXHINUM							10h

7 RXDETMD

0 = Once RX data received in RXLINEn line, keep RXLnDET=1 until RXLINEn=000h is written.

1 = Update RX data received status RXLnDET in RXLINEn line in every frame if RXLINEn is not 000h.

6-0 RXHINUM

Sets the data detection threshold for VIN. If the high-level detection per RX received bit is more than RXHINUM, that bit is treated as 1, otherwise, it is treated as 0. Unit 1 number corresponds to one 74.25MHz clock.

7.1.120 RX Horizontal Start Register

Index	7	6	5	4	3	2	1	0	Reset
D4			RXHST [9-8]						06h
D5	RXHST [7-0]								BEh

9-0 RXHST

Define the horizontal detection start position of RX receiving data for VINn

7.1.121 RX Horizontal End Register

Index	7	6	5	4	3	2	1	0	Reset
D4					RXHEND [11-8]				06h
D6	RXHEND [7-0]								39h

11-0 RXHEND

Define the horizontal detection end position of RX receiving data for VINn

7.1.122 RX Bit Number Register

Index	7	6	5	4	3	2	1	0	Reset
D7			RXBITNUM						27h

7-6 Reserved

5-0 RXBITNUM

(RXBITNUM+1) sets the total data bit number including first start bit 1 per line for VIN.

***Following MIPI registers can be read/write accessible when MPAGE=1**

7.1.123 Bias Gen & VTG Control Register

Index	7	6	5	4	3	2	1	0	Reset
00	PWD12 BG	ISEL			VBG SELB	IPSEL			44h

7 PWD12BG

0 = BANDGAP is normal operation

1 = BANDGAP is power down

6-4 ISEL

Bias Current Adjust

3 VBGSELB

Bandgap select

2-0 IPSEL

Driver Reference DC Adjust

7.1.124 Clock Lane Control Register

Index	7	6	5	4	3	2	1	0	Reset
01	CKHS BUF1	CKHS BUF0	CKLPBUF		CKINV SEL	CKPH			F0h

7 CKHSBUF1

Driving Capability control 1

6 CKHSBUF0

Driving Capability control 0

5-4 CKLPBUF

Clock Lane Slew rate control for Low power Clock driver

00 : 0pF 01 : 5pF 10 : 20pF 11 : 70pF

3 CKINVSEL

Clock output invert select

2-0 CKPH

Clock output delay control

7.1.125 MIPICKEN Register

Index	7	6	5	4	3	2	1	0	Reset
02					CKHINVSER	CKINVSER	PWD12CK	MIPICKEN	00h

7-4 Reserved

3 CKHINVSER

Half Full Speed Clock invert for Serializer

0 = not inversed

1 = inversed

2 CKINVSER

Full Speed Clock invert for Serializer

0 = not inversed

1 = inversed

1 PWD12CK

0 = CK Lane is normal operation

1 = CK Lane is power down

0 MIPICKEN

0 = disable MIPI Clock output

1 = enable MIPI Clock output

7.1.126 Lane0-1 Data Latch Clock Phase Select Register

Index	7	6	5	4	3	2	1	0	Reset
03		D_PH1				D_PH0			00h

7 Reserved

6-4 D_PH1

Lane1 data Latch clock phase select for Serializer

3 Reserved

2-0 D_PH0

Lane0 data Latch clock phase select for Serializer

7.1.127 Lane2-3 Data Latch Clock Phase Select Register

Index	7	6	5	4	3	2	1	0	Reset
04		D_PH3				D_PH2			00h

7 Reserved

6-4 D_PH3. Reserved for future use.
Lane3 data Latch clock phase select for Serializer

3 Reserved

2-0 D_PH2. Reserved for future use.
Lane2 data Latch clock phase select for Serializer

7.1.128 HS Driver Capability Select Register

Index	7	6	5	4	3	2	1	0	Reset
06	HSTX3 BUF1	HSTX2 BUF1	HSTX1 BUF1	HSTX0 BUF1	HSTX3 BUF0	HSTX2 BUF0	HSTX1 BUF0	HSTX0 BUF0	FFh

7 HSTX3BUF1. Reserved for future use.
Lane3 HS Driver capability select1

6 HSTX2BUF1. Reserved for future use.
Lane2 HS Driver capability select1

5 HSTX1BUF1
Lane1 HS Driver capability select1

4 HSTX0BUF1
Lane0 HS Driver capability select1

3 HSTX3BUF0. Reserved for future use.
Lane3 HS Driver capability select0

2 HSTX2BUF0. Reserved for future use.
Lane2 HS Driver capability select0

1 HSTX1BUF0
Lane1 HS Driver capability select0

0 HSTX0BUF0
Lane0 HS Driver capability select0

7.1.129 Low Power mode Slew Rate Control Register

Index	7	6	5	4	3	2	1	0	Reset
07	LPTXBUF3		LPTXBUF2		LPTXBUF1		LPTXBUF0		FFh

7-6 LPTXBUF3. Reserved for future use.

Lane3 PHY Driver Low Power mode slew rate control

00: 0pF 01: 5pF 10: 20pF 11: 70pF

5-4 LPTXBUF2. Reserved for future use.

Lane2 PHY Driver Low Power mode slew rate control

00: 0pF 01: 5pF 10: 20pF 11: 70pF

3-2 LPTXBUF1

Lane1 PHY Driver Low Power mode slew rate control

00: 0pF 01: 5pF 10: 20pF 11: 70pF

1-0 LPTXBUF0

Lane0 PHY Driver Low Power mode slew rate control

00: 0pF 01: 5pF 10: 20pF 11: 70pF

7.1.130 MIPI Output Enable Control Register

Index	7	6	5	4	3	2	1	0	Reset
08	PWD_3	PWD_2	PWD_1	PWD_0	MIPIEN3	MIPIEN2	MIPIEN1	MIPIEN0	00h

7 PWD_3 (Reserved for future use)

0 = Lane3 is disable (power down) for Serializer

1 = Lane3 is enable for Serializer

6 PWD_2 (Reserved for future use)

0 = Lane2 is disable (power down) for Serializer

1 = Lane2 is enable for Serializer

5 PWD_1

0 = Lane1 is disable (power down) for Serializer

1 = Lane1 is enable for Serializer

4 PWD_0

0 = Lane0 is disable (power down) for Serializer

1 = Lane0 is enable for Serializer

3 MIPIEN3 (Reserved for future use)

0 = Lane3 MIPI Output disable

1 = Lane3 MIPI Output enable

2 MIPIEN2 (Reserved for future use)

0 = Lane2 MIPI Output disable

1 = Lane2 MIPI Output enable

1 MIPIEN1

0 = Lane1 MIPI Output disable

1 = Lane1 MIPI Output enable

0 MIPIEN0

0 = Lane0 MIPI Output disable

1 = Lane0 MIPI Output enable

7.1.131 MIPITEST1 Register

Index	7	6	5	4	3	2	1	0	Reset
09	MIPITEST1								00h

Reserved

7.1.132 MIPITEST2 Register

Index	7	6	5	4	3	2	1	0	Reset
0A	MIPITEST2								00h

Reserved

7.1.133 PLL Control Register 1

Index	7	6	5	4	3	2	1	0	Reset
10	RST_PLL_REG	PWDPLL	DIV_FIN		LOCK_ENB	LOCK_VREF			08h

7 RST_PLL_REG

0 = normal

1 = register controlled reset

6 PWDPLL

0 = normal

1 = register controlled PLL power down

5-4 DIV_FIN

00 = 1

01 = 1/2

10 = 1/4

11 = stay at low

3 LOCK_ENB. When disabled, the PLL lock output stays high.

0 = lock detector enabled

1 = disabled

2-0 LOCK_VREF. PLL lock detector duty cycle threshold selection (2.27% per step)

000 = 81.8%

001 = 84.07%

…

111 = 97.7%

7.1.134 PLL Control Register 2

Index	7	6	5	4	3	2	1	0	Reset
11	DIV_PRE_FB			DIV_POST_FB					54h

7-6 DIV_PRE_FB PLL, First feedback divider control

00 = 1

01 = 1/2

10 = 1/4

11 = stay at low

5 Reserved

4-0 DIV_POST_FB, Second feedback divider control

00000= 1/2

…

11110= 1/32

11111= 1

Total feedback divider = DIV_PRE_FB x (2 + DIV_POST_FB) (except DIV_POST_FB=11111)

7.1.135 PLL Control Register 3

Index	7	6	5	4	3	2	1	0	Reset
12	BG _SELB	ISEL			ICP_SEL				47h

7 BG_SELB, reference control

0 = bandgap referenced

1 = VDD referenced

6-4 ISEL, bias current control at 5uA per step

000 = 30uA

…

100 = 50uA (default)

…

111 = 65uA

3-0 ICP_SEL, charge pump current control at 2.5uA per step

0000 = 2.5uA

…

1111 = 40uA

7.1.136 PLL Control Register 4

Index	7	6	5	4	3	2	1	0	Reset
13			OUT_ DIV_EN	BYPASS _27M	DIV_OUT_PRE		DIV_OUT_POST		24h

PLL output circuit contains additional dividers and selection logics. The output can be directly from VCO, Xin or the divider. The divider ratio is DIV_OUT_PRE x DIV_OUT_POST

7-6 Reserved

5 OUT_DIV_EN, main output control

0 = VCO output

1 = divider output or Xin

4 BYPASS_27M

0 = divider output

1 = Xin bypass

3-2 DIV_OUT_PRE

00 = 1

01 = 1/2

10 = 1/4

11 = no clock, stay low

1-0 DIV_OUT_POST

00 = 1

01 = 1/2

10 = 1/4

11 = no clock, stay low

7.1.137 PLL Control Register 5

Index	7	6	5	4	3	2	1	0	Reset
14	RST_CLK_GEN	DIV_CLK_PIX			RST_PLL	DIV_CLK_PHY			04h

This register controls the clock selection for each internal block.

7 RST_CLK_GEN Divider Reset

0 = dividers are in normal operation

1 = reset all the dividers

6-4 DIV_CLK_PIX, This controls the PIX clock frequency with respect to the VCO frequency

0xx = 1

100 = 1/2

101 = 1/4

110 = 1/8

111 = 1/16

3 RST_PLL

Reserved

2-0 DIV_CLK_PHY, This controls the PHY clock frequency with respect to the VCO frequency

0xx = 1

100 = 1/2

101 = 1/4

110 = 1/8

111 = 1/16

7.1.138 PLL Control Register 6

Index	7	6	5	4	3	2	1	0	Reset
15			DIV_CLK_DEC		DIV_CLK_VC		DIV_CLK_BYT		00h

This register controls the clock selection for each internal block.

7-6 Reserved

5-4 DIV_CLK_DEC, This controls the DEC clock frequency with respect to the VCO frequency

00 = 1/8

01 = 1/16

10 = 1/32

11 = 1/64

3-2 DIV_CLK_VC, This controls the VC clock frequency with respect to the VCO frequency

00 = 1/8

01 = 1/16

10 = 1/32

11 = 1/64

1-0 DIV_CLK_BYT, This controls the Byte clock frequency with respect to the VCO frequency

00 = 1/8

01 = 1/16

10 = 1/32

11 = 1/64

7.1.139 NUM_LANES Register

Index	7	6	5	4	3	2	1	0	Reset
20		NUM_CHANNELS			PSFM	NUMLANES			44h

7 Reserved

6-4 NUM_CHANNELS

Number of video channels to be processed

3 PSFM

Pseudo-Single Frame Mode

2-0 NUM_LANES

Number of MIPI data lanes to use for Tx

7.1.140 FSWAIT Register

Index	7	6	5	4	3	2	1	0	Reset
21					FSWAIT [11-8]				00h
22	FSWAIT [7-0]								00h

FSWAIT [11-0]

Frame start wait time from EAV to FS packet (in pixels)

7.1.141 STOPCLK Register

Index	7	6	5	4	3	2	1	0	Reset
23		SKIP_FRAMING	FRAME_NUM_ENA	YC16BIT	PCLKPOL	TP_ENA	STOPCLK	ULPMCLK	00h

7 Reserved

6 SKIP_FRAMING

0 = disable SKIP_FRAMING

1 = enable SKIP_FRAMING

5 FRAME_NUM_ENA

0 = disable FRAME_NUM_ENA

1 = enable FRAME_NUM_ENA

3 PCLKPOL

0 = PCLK clock polarity is not inversed

1 = PCLK clock polarity is inversed

2 TP_ENA

0 = normal operation

1 = Test function to enable BT.1120 test pattern output to MIPI module

1 STOPCLK

0 = normal operation

1 = Force DPHY clock lane into STOP state

0 UPMCLK

0 = normal operation

1 = Put clock lane into Ultra Low Power Mode

7.1.142 CLKESC Register

Index	7	6	5	4	3	2	1	0	Reset
24	ULPM				CLKESC				00h

7-4 ULPM [3-0]

0 = normal operation

1 = Put data lanes into ULPM (1-bit per lane)

3-0 CLKESC [3-0]

0 = normal operation

1 = Data lane Clock Escape request (1-bit per lane)

7.1.143 T_LPX Register

Index	7	6	5	4	3	2	1	0	Reset
25	T_LPX								04h

T_LPX All lanes. Low Power state transition time control (in mclk cycles)

7.1.144 T_PREP Register

Index	7	6	5	4	3	2	1	0	Reset
26	T_PREP								06h

T_PREP All lanes. Lanes preparation time control (in mclk cycles)

7.1.145 T_TRAIL Register

Index	7	6	5	4	3	2	1	0	Reset
27	T_TRAIL								03h

T_TRAIL All lanes. It controls the HS trail time after the final Tx bit and the HS ZERO time (in mclk cycles)

7.1.146 T_WAKE Register

Index	7	6	5	4	3	2	1	0	Reset
28	T_WAKE								18h

T_WAKE All lanes. ULPM wake up time control (in mclk cycles)

7.1.147 HACTIVE_LN Register

Index	7	6	5	4	3	2	1	0	Reset
31	HACTIVE_LN [15-8]								00h
32	HACTIVE_LN [7-0]								00h

HACTIVE_LN

Detected horizontal active line length in pixels (optional status register per Virtual Channel)

These bits are read only

7.1.148 Digital MIPI Reset Register

Index	7	6	5	4	3	2	1	0	Reset
33					RST _PHY	RST _CSI		RST _BTG	00h

7-4 Reserved

3 RST_PHY

0 = clk_dig module is normal operation

1 = clk_dig module is in reset condition

2 RST_CSI

0 = csi2tx module is normal operation

1 = csi2tx module is in reset condition

1 Reserved

0 RST_BTG

0 = bt1120tx module is normal operation

1 = bt1120tx module is in reset condition

7.1.149 Vertual Channel ID Register

Index	7	6	5	4	3	2	1	0	Reset
34	CH4_VCI		CH3_VCI		CH2_VCI		CH1_VCI		E4h

7-6 CH4_VCI

Virtual Channel ID for video channel 4

5-4 CH3_VCI

Virtual Channel ID for video channel 3

3-2 CH2_VCI

Virtual Channel ID for video channel 2

1-0 CH1_VCI

Virtual Channel ID for video channel 1

7.1.150 FE_WAIT Register

Index	7	6	5	4	3	2	1	0	Reset
35			FE_WAIT						15h

7-6 Reserved

5-0 FE_WAIT

Frame End wait in lines after VACTIVE fall (PSFM mode)

7.1.151 FE_ADJ Register

Index	7	6	5	4	3	2	1	0	Reset
36							FE_ADJ		01h

7-2 Reserved

1-0 FE_ADJ

Frame End wait adjustment for odd field (-2 to 1)

7.1.152 OVERFLOW Register

Index	7	6	5	4	3	2	1	0	Reset
37								OVERFLOW	00h

7-1 Reserved

0 OVERFLOW

FIFO overflow indicator

These bits are read only

7.1.153 UNDERFLOW Register

Index	7	6	5	4	3	2	1	0	Reset
38								UNDERFLOW	00h

7-1 Reserved

0 UNDERFLOW

FIFO overflow indicator

These bits are read only

7.1.154 PCLK Mode Register

Index	7	6	5	4	3	2	1	0	Reset
39								PCLKMD	00h

7-1 Reserved

0 PCLKMD

0 = pclk is VD1120CKO from HDDEC module

1 = pclk is CLK_BYT from PLL module

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12/17/2018	Update pin description and power supply table
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