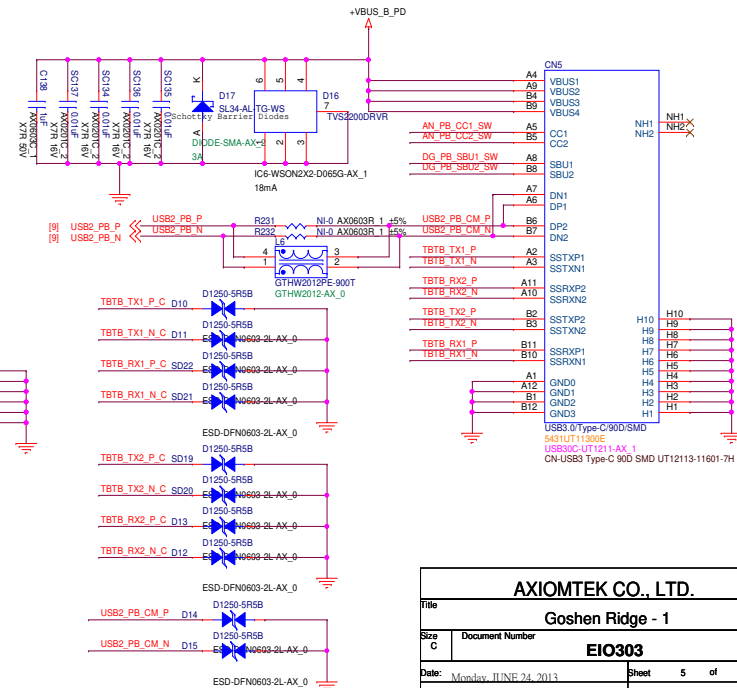
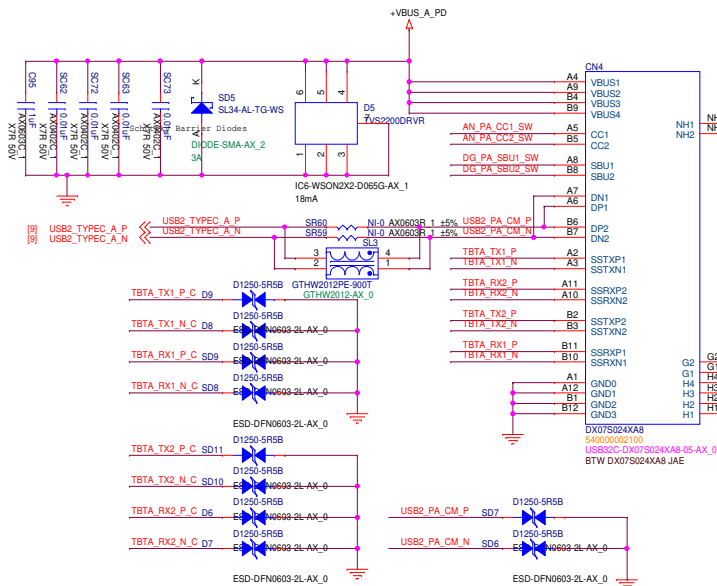
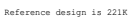
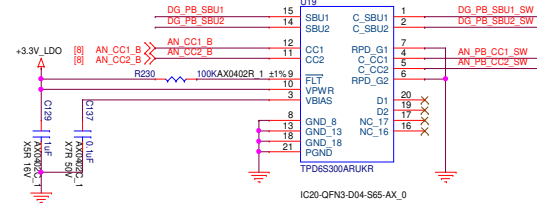
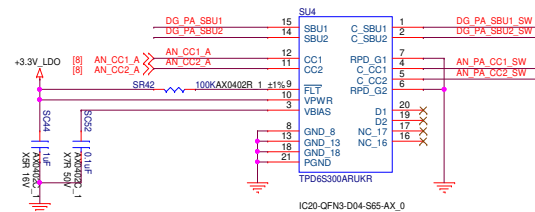
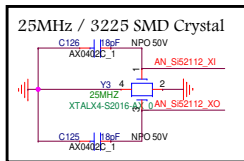
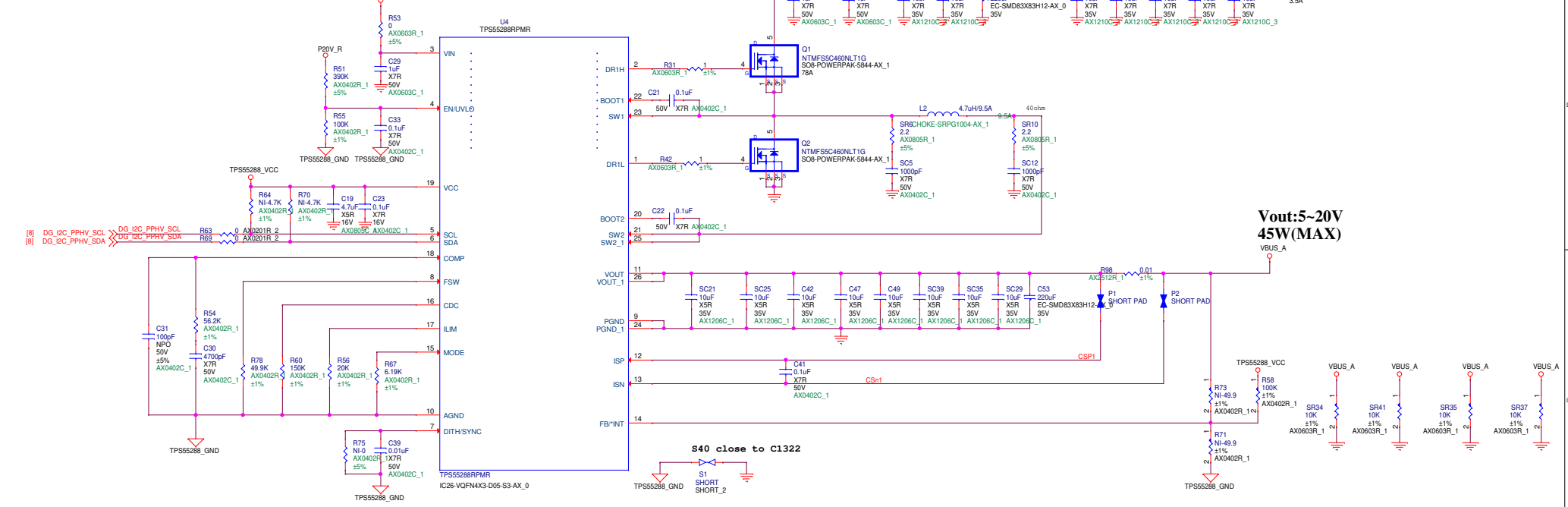




AXIOMTEK CO., LTD.				
Goshen Ridge - 1				
EIO303		Rev A00		
Date: Monday, JUNE 24, 2013		Sheet 5 of 15		
Designed by: Oden Chang		Checked by: James Chang		

P20V -> VBUS_A (5V,9V,15V)

Max: 2.5A Max: 3A



Vout:5-20V
45W(MAX)

P20V -> VBUS_B (5V)

Max: 0.775A Max: 3A

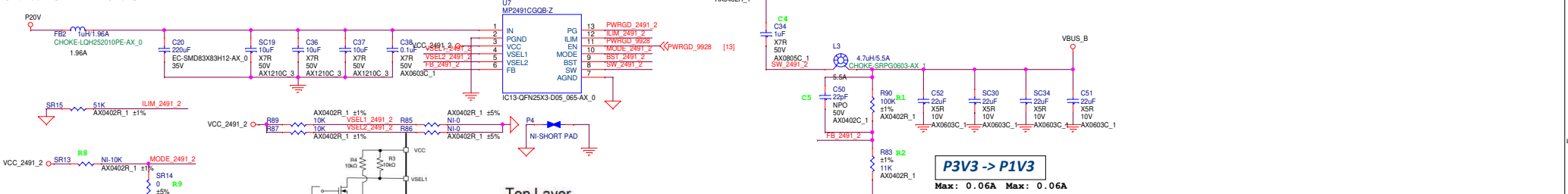
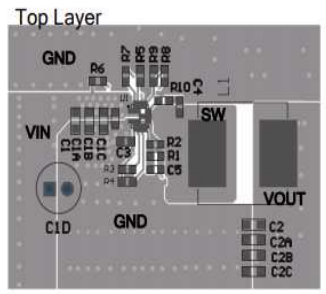


Figure 8: Output Adjust Configuration
Table 2 shows details for the reference voltage setting.

Table 2: VSEL1, VSEL2 Truth Table

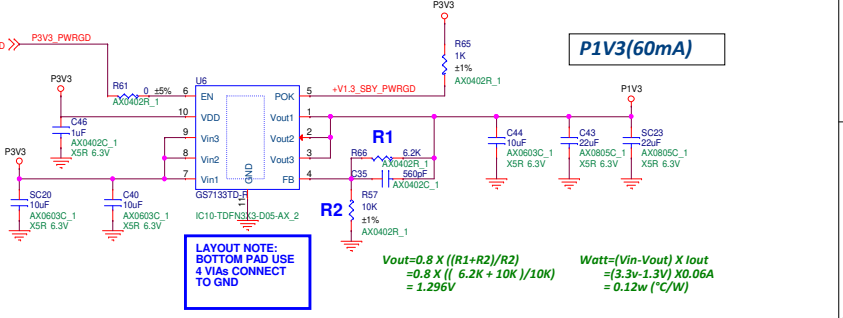
VSEL1	VSEL2	V _{REF}	V _{OUT}
0	0	2V	20V
0	1	1.5V	15V
0	0	0.9V	9V
1/2 V _{CC}	0	1.2V	12V
V _{CC}	V _{CC}	0.5V	5V

There is a 20µs delay time for each VSEL pin logic voltage change.



P3V3 -> P1V3

Max: 0.06A Max: 0.06A



LAYOUT NOTE:
BOTTOM PAD USE
4 VIAS CONNECT
TO GND

$$V_{out} = 0.8 \times ((R1 + R2) / R2)$$
$$= 0.8 \times ((6.2K + 10K) / 10K)$$
$$= 1.296V$$
$$Watt = (V_{in} - V_{out}) \times I_{out}$$
$$= (3.3V - 1.3V) \times 0.06A$$
$$= 0.12W \text{ (} ^\circ C/W \text{)}$$