Schematic Review Form

Customer/Project

Pin #	Name	Info	Violations	*Description*
1	DP0	need 1.5k pullup to 3.3v		upstream USB port DP
2	DM0			upstream USB port DM
3	VCC		need cap on each supply	3.3V SUPPLY
4	RESET			RESET is an active low TTL input,Generally, a reset with a pulse width between 100 µs and 1 ms is recommended after 3.3-V VCC reaches its 90%
5	EECLK			EEPROM serial clock
6	EEDATA/GANGED			EEPROM serial data/power-management mode indicator
7	GND			GND
8	BUSPWR	pullup is bus powered mode		Power source indicator

9	PWRON1			Power-on/-off control signals for port 1. active low
10	OVRCUR1			Overcurrent input. active low
11	DM1	has 15k pulldown		DM for downstream port 1
12	DP1	has 15k pulldown		DP for downstream port 1
13	PWRON2			Power-on/-off control signals. active low
14	OVRCUR2			Overcurrent input FOR PORT2 . active low
15	DM2	has 15k pulldown		DM for downstream port 2
16	DP2	has 15k pulldown		DP for downstream port 2
17	PWRON3			Power-on/-off control signals for port 3. active low
18	OVRCUR3			Overcurrent input FOR PORT3 . active low

19	DM3	has 15k pulldown		DM for downstream port 3
20	DP3	has 15k pulldown		DP for downstream port 3
21	PWRON4			Power-on/-off control signals for port 4. active low
22	OVRCUR4			Overcurrent input FOR PORT3 . active low
23	DM4	not used		DM for downstream port 4
24	DP4	not used		DP for downstream port 4
25	VCC		need cap on each supply	3.3V SUPPLY
26	EXTMEM	pullup : no EEPROM		When EXTMEM is high, the serial EEPROM interface of the device is disabled
27	TSTPLL/ 48MCLK			EXTERNAL 48kHz tomorrow
28	GND			GND

29	XTAL2			XTAL2 is a 6-MHz crystal output.
30	XTAL1			XTAL1 is a 6-MHz crystal input
31	TSTMODE			Test/mode terminal.
32	SUSPND			SUSPND STATUS

Comments

is port 4 used?