

Schematic Review Form

Customer/Project

TI Confidential - NDA Restrictions

Pin #	Name	Info	Violations	Description
1	VDD3V3	We recommend a 100nF cap per VDD3V3 pin, and a 1uF cap. See two 100nF caps and two 10nF caps.		3.3V supply voltage
2	EQ0	PD to GND, okay.	Please ensure EQ settings match the loss between the repeater and the connector.	(See Table 5-2)
3	VIOSEL	PU to 1.8V, okay.	PD cap is not needed.	VIOSEL is used to select digital I/O input voltage for GPIOs, CROSS and I2C VIOSEL = VSS sets device into 1.2V I/O mode VIOSEL = VDD1V8 sets device into 1.8V I/O mode VIOSEL pin is real time control and not only latched at powered on reset. Be careful when this pin changes dynamically after power-on reset because the output voltage can change from 1.2V to 1.8V.
4	EQ1	PD to GND, okay.	Please ensure EQ settings match the loss between the repeater and the connector.	(See Table 5-2)
5	RESETB	PU to 1.8V with a 100nF PD cap, okay.		Active Low Reset. After the RESETB deassertion, both repeaters are enabled and in eUSB2 default mode awaiting configuration from eDSPr or eUSPr.
6	DPB	If present, we recommend against CMCs. Otherwise, okay.	What are these SH components for? Are these shunts? Recommend against shunts in the trace if possible.	USB port B D+ pin
7	DNB	If present, we recommend against CMCs. Otherwise, okay.	What are these SH components for? Are these shunts? Recommend against shunts in the trace if possible.	USB port B D- pin
8	GND	Okay.		GND
9	DNA	If present, we recommend against CMCs. Otherwise, okay.	What are these SH components for? Are these shunts? Recommend against shunts in the trace if possible.	USB port A D- pin
10	DPA	If present, we recommend against CMCs. Otherwise, okay.	What are these SH components for? Are these shunts? Recommend against shunts in the trace if possible.	USB port A D+ pin
11	VDD1V8	We recommend a 100nF cap and a 1uF cap.		1.8V analog supply voltage
12	EQ2/INT	PD to GND, okay.	Please ensure EQ settings match the loss between the repeater and the connector.	I2C Mode: Open Drain active low level sensitive interrupt output to system non-I2C Mode: (See Table 5-2)
13	SCL	Floating. Please confirm I2C use is not intended.		I2C clock Open drain I/O.
14	SDA	Floating. Please confirm I2C use is not intended.		Bidirectional I2C data. Open drain I/O. Pulled up to I2C rail through an external resistor
15	VDD3V3	We recommend a 100nF cap per VDD3V3 pin, and a 1uF cap. See two 100nF caps and two 10nF caps.		3.3V supply voltage
16	eDP0	Okay.	What are these SH components for? Are these shunts? Recommend against shunts in the trace if possible.	eUSB2 port 0 D+ pin
17	eDN0	Okay.	What are these SH components for? Are these shunts? Recommend against shunts in the trace if possible.	eUSB2 port 0 D- pin
18	GND	Okay.		GND
19	eDN1	Okay.	What are these SH components for? Are these shunts? Recommend against shunts in the trace if possible.	eUSB2 port 1 D- pin
20	eDP1	Okay.	What are these SH components for? Are these shunts? Recommend against shunts in the trace if possible.	eUSB2 port 1 D+ pin

Comments