

Schematic Review Form

Pin #	Name	Info	Violations	Description
1	CC1	I see DNP resistors on the CC lines. In general we recommend connecting the CC pins directly to the connector, so this is okay.		Type-C configuration channel signal 1
2	CC2	I see DNP resistors on the CC lines. In general we recommend connecting the CC pins directly to the connector, so this is okay.		Type-C configuration channel signal 2
3	PORT	Pulled down for UFP functionality. Please ensure UFP mode is intended.		Tri-level input pin to indicate port mode. The state of this pin is sampled when EN_N is asserted low and VDD is active. This pin is also sampled following a I2C_SOFT_RESET. H - DFP (Pull-up to VDD if DFP mode is desired) NC - DRP (Leave unconnected if DRP mode is desired) L - UFP (Pull-down or tie to GND if UFP mode is desired)
4	VBUS_DET		Please ensure VBUS_DET is connected to the incoming VBUS from the type-C port. It does not look like it is at the moment going by the net names.	5- to 28-V VBUS input voltage. VBUS detection determines UFP attachment. One 900-kΩ external resistor required between system VBUS and VBUS_DET pin.
5	ADDR	Floating for GPIO mode. Please confirm this is intended.		Tri-level input pin to indicate I2C address or GPIO mode: H - I2C is enabled and I2C 7-bit address is 0x61. NC - GPIO mode (I2C is disabled) L - I2C is enabled and I2C 7-bit address is 0x60. ADDR pin should be pulled up to VDD if high configuration is desired
6	INT_EN/OUT3	Floating, okay if audio accessory mode is not intended.		The INT_N/OUT3 is a dual-function pin. When used as the INT_N, the pin is an open drain output in I2C control mode and is an active low interrupt signal for indicating changes in I2C registers. When used as OUT3, the pin is in audio accessory detect in GPIO mode: no detection (H), audio accessory connection detected (L).
7	SDA/OUT1	Confirm I2C is not being used.	I would recommend a 200KOhm pull-up for OUT1/2 rather than a 10KOhm pull-up.	The SDA/OUT1 is a dual-function pin. When I2C is enabled (ADDR pin is high or low), this pin is the I2C communication data signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the TUSB320 device is in UFP mode: Refer to Table 7-3 for more details.
8	SCL/OUT2	Confirm I2C is not being used.	I would recommend a 200KOhm pull-up for OUT1/2 rather than a 10KOhm pull-up.	The SCL/OUT2 is a dual function pin. When I2C is enabled (ADDR pin is high or low), this pin is the I2C communication clock signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the TUSB320 device is in UFP mode: Refer to Table 7-3 for more details.
9	ID	Floating, okay if DRP/DFP is not being used.		Open drain output; asserted low when the CC pins detect device attachment when port is a source (DFP), or dual-role (DRP) acting as source (DFP).
10	GND			Ground
11	EN_N		EN_N should be pulled down to ground. If this pin is pulled-up, there will be no device functionality.	Enable signal; active low. Pulled up to VDD internally to disable the TUSB320 device. If controlled externally, must be held high at least for 50 ms after VDD has reached its valid voltage level.
12	VDD	100nF cap, okay.		Positive supply voltage. VDD must ramp within 25 ms or less.

Comments