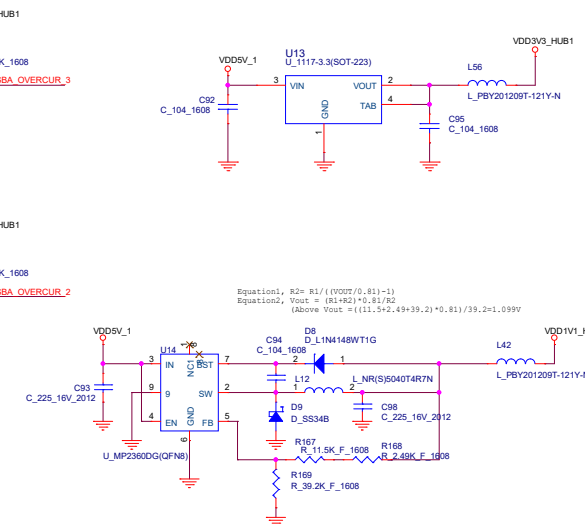
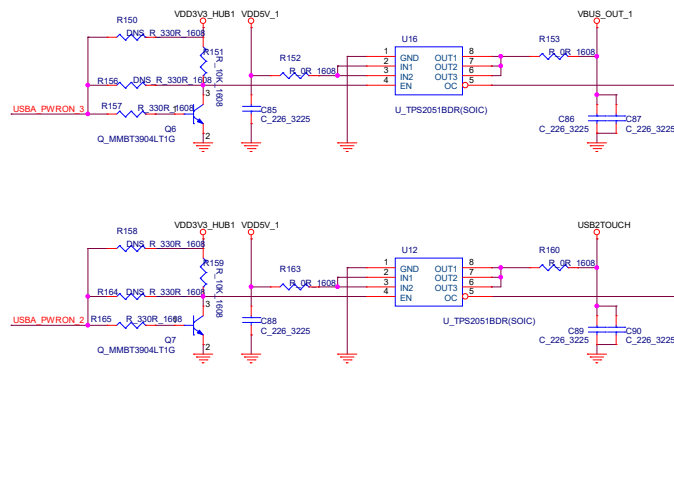
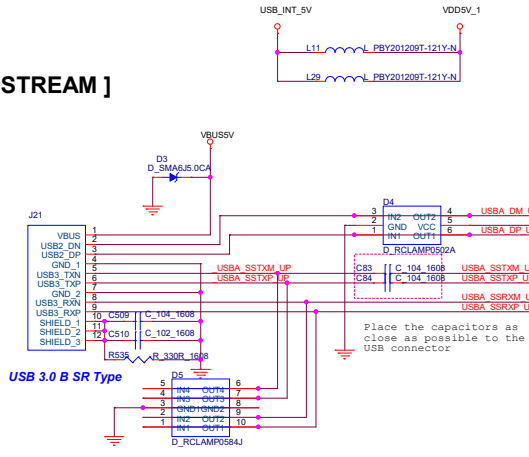


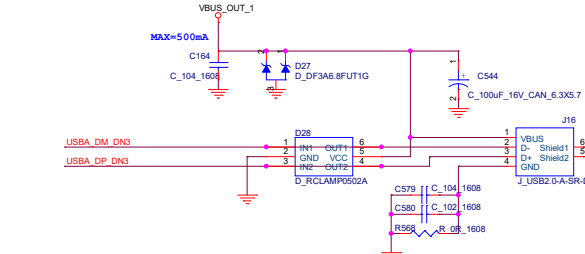
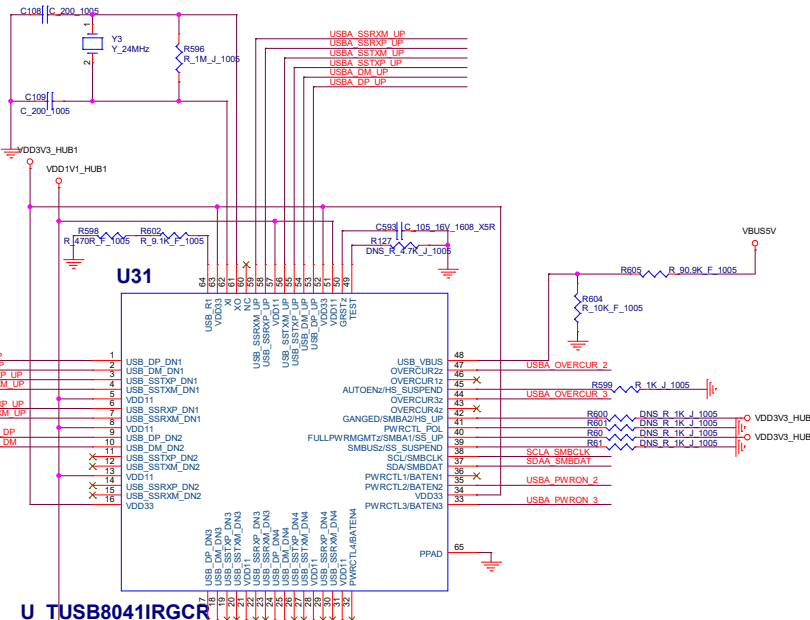
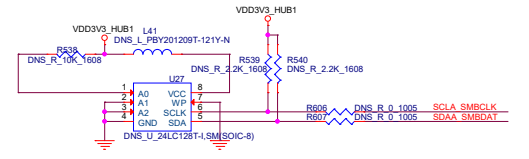
USB 3.0 HUB 1

USB signal line trace:
 1. Keep traces of USB bus D+ and D- the same length.
 2. Achieve 90 ohm differential characteristic impedance.
 3. Achieve 45 ohm common characteristic impedance.
 4. Maintain parallelism between D+ and D-.
 5. Do not route USB2.0 D+ and D- over the power plane split.
 6. Do not route USB2.0 D+ and D- over the other high frequency signals.

[USB UP STREAM]

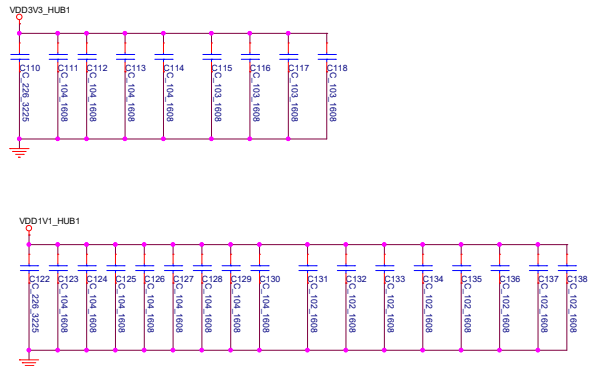


[USB DOWN STREAM_1 - Lower OP Panel USB]

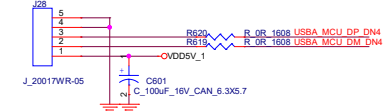


[TO. USB HUB 2]

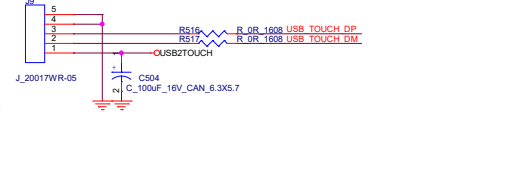
Power bypass capacitor



[MICOM]

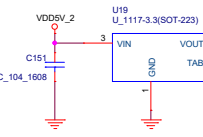


[TOUCH PANEL]



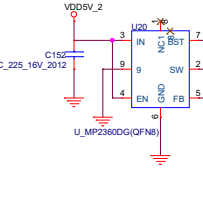
Place the capacitors as close as possible to the USB connector

USB 3.0 HUB 2

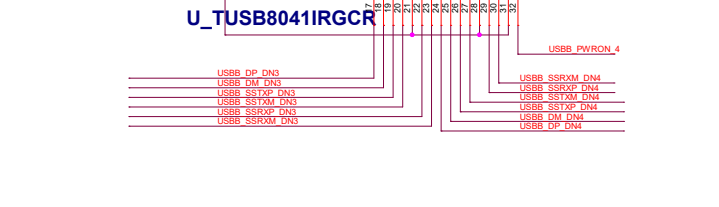
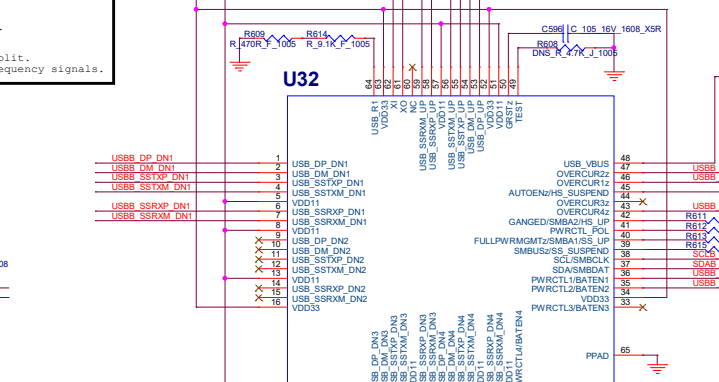
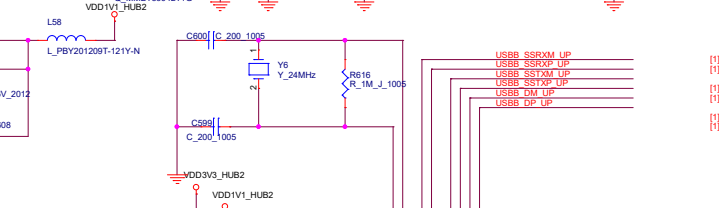
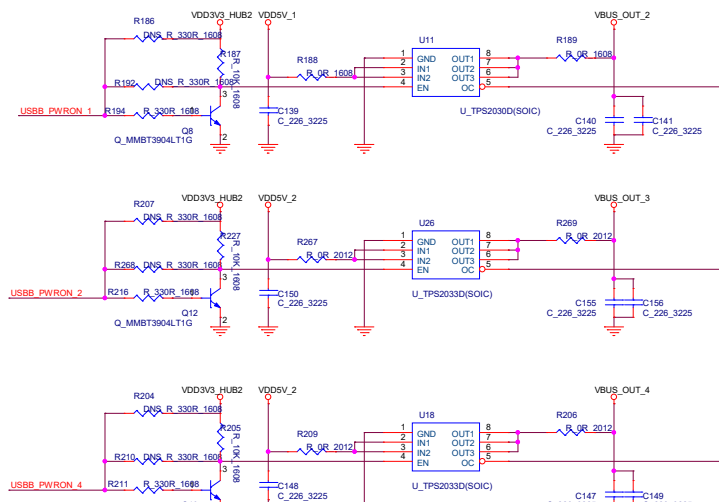
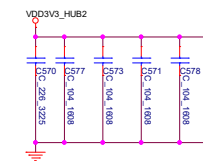
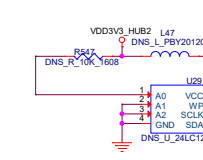


* Place the LDO as far away as possible from the IC, X-tal and USB-lines
(LDO는 가능한 IC, X-tal 및 USB라인과 떨어져어임.)

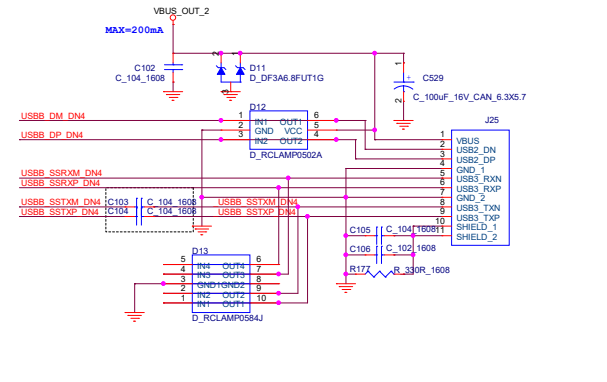
Equation1: $R2 = R1 / ((VOUT / 0.81) - 1)$
Equation2: $Vout = (0.81 * R2) / (R1 + R2)$
(Above Vout = $((11.5 + 2.49 * 39.2) * 0.81) / (39.2 + 10.99V)$)



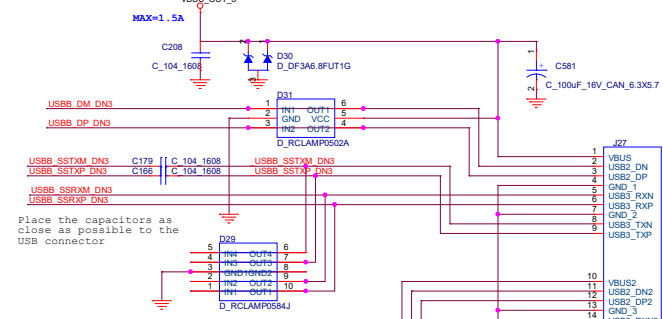
USB signal line trace:
1.Keep traces of USB bus D+ and D- the same length.
2.Achieve 90 ohm differential characteristic impedance.
3.Achieve 45 ohm common characteristic impedance.
4.Maintain parallelism between D+ and D-
5.Do not route USB2.0 D+ and D- over the power plane split.
6.Do not route USB2.0 D+ and D- over the other high frequency signals.



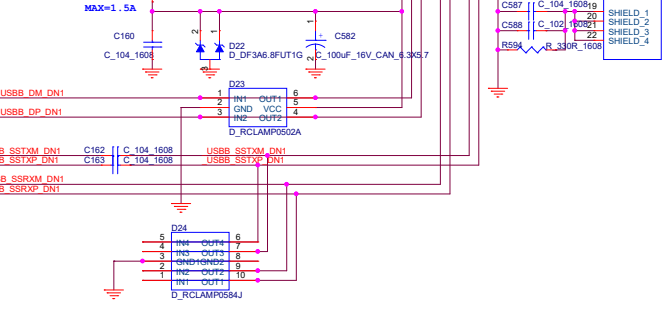
[USB DOWN STREAM1 - Main Display USB Power]



[USB DOWN STREAM_3 -Customer Port USB1]



[USB DOWN STREAM_4 -Customer Port USB2]



FROM. USB HUB 1

- (1) USBB_DM_UP >>> USBB_DM_UP
- (1) USBB_DP_UP >>> USBB_DP_UP
- (1) USBB_SSTXM_UP >>> USBB_SSTXM_UP
- (1) USBB_SSTXP_UP >>> USBB_SSTXP_UP
- (1) USBB_SSRXM_UP >>> USBB_SSRXM_UP
- (1) USBB_SSRXP_UP >>> USBB_SSRXP_UP