Application Note
10 Dec 2014

TUSB9261 SATA BIST Test Configuration

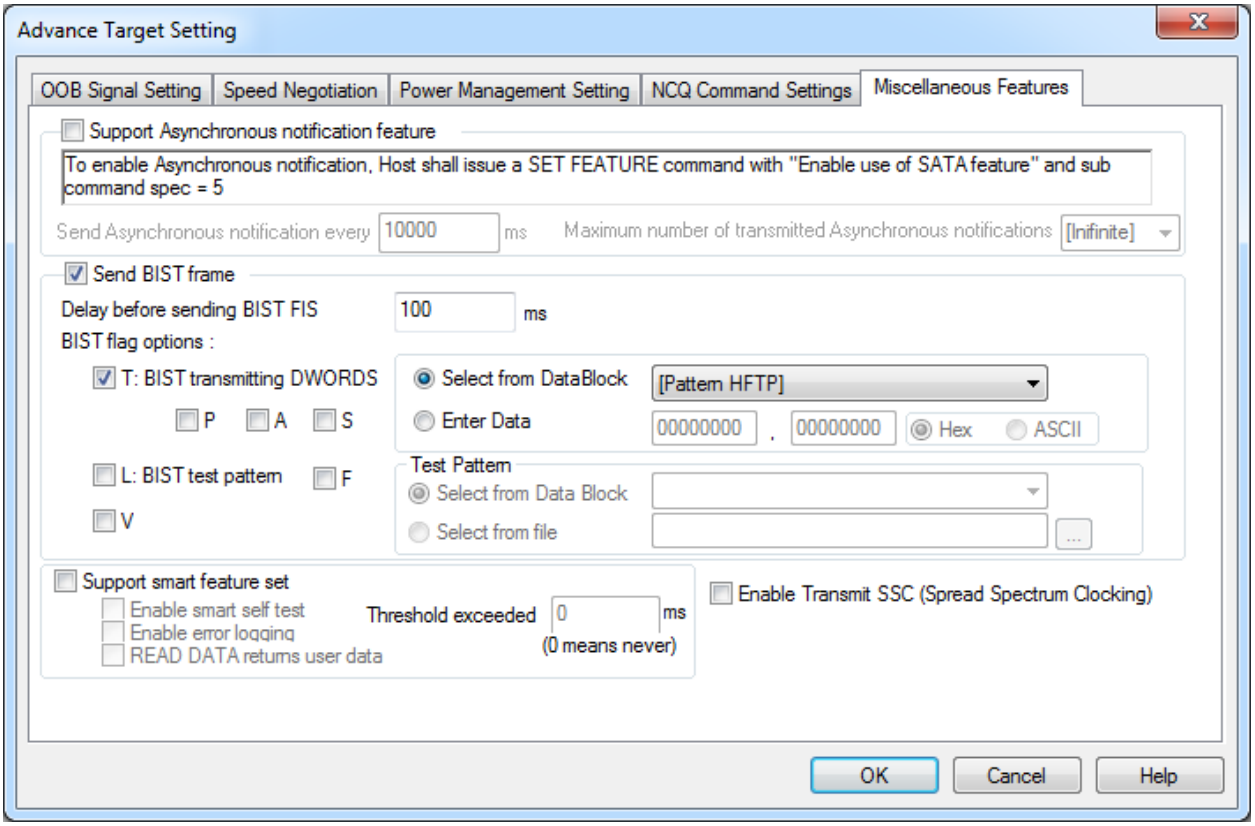
High-Speed Interface

There are two methods to enable SATA loopback and pattern transmission for testing.

METHOD 1 (PREFERRED): Use SATA device emulator to send BIST FIS.

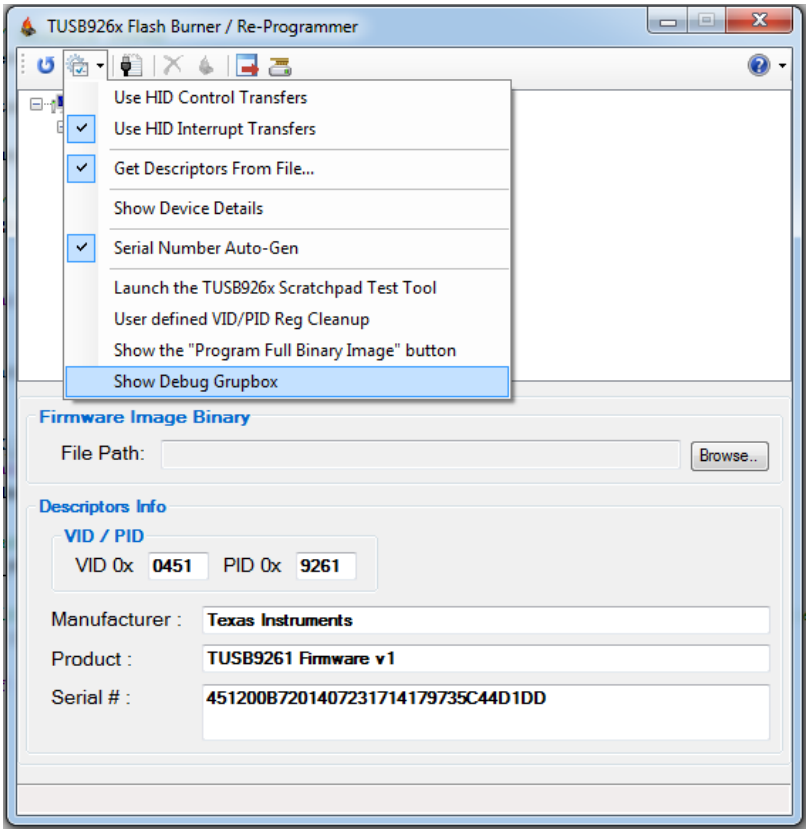
The SATA emulator must be able to negotiate SATA Gen1/2 connection and respond to IDENTIFY DEVICE command sent by the TUSB9261 before any BIST FIS can be sent. SATA test equipment that cannot respond to the IDENTIFY DEVICE command is not supported. TUSB9261 must be power cycled when changing test modes or patterns.

Sample setup for BIST-T (HFTP pattern) from LeCroy STX-231 SATA Analyzer/Emulator:

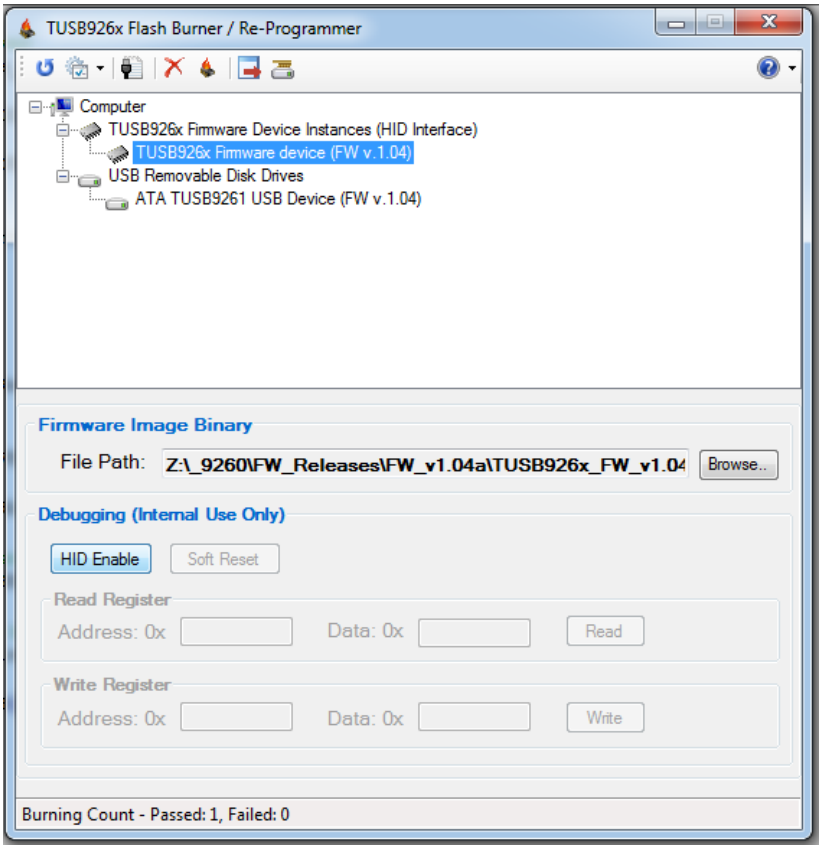


METHOD 2: Enable HID (by programming firmware with HID-enabled USB descriptors) on TUSB9261 and use FlashBurner tool to manually configure registers via HID commands. See FlashBurner help for instructions on programming.

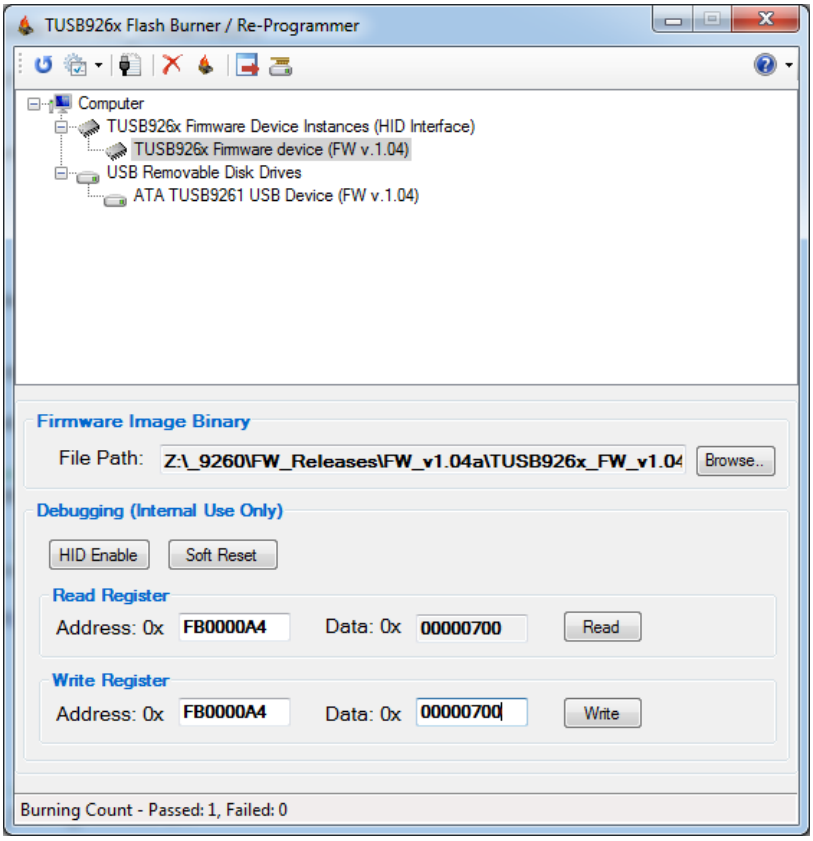
1. Open FlashBurner application.
2. Hold “CTRL + SHIFT” keys and enter ‘TI’ to enable “Show Debug GrupBox” option in the menu.
3. Select “Show Debug GrupBox” from menu.



4. Select HID Instance of TUSB926x and click on “HID Enable” button.



5. Use Flash Burner debugging to Read/Write the desired registers. To prevent modifying any unintended bits, read the original register value before determining the new value to write.



BIST Control Register

Address: 0xFB00 00A4

Default Value: 0x0000 0700

Once this register is written to, the TUSB9261 must be power cycled or global reset must be asserted before it can be written again.

Field	Bit ID	Description	Access	Reset
31:21		**Reserved**	RO	0
20	FERLB	**Far-end Retimed Loopback** When set, this bit is used to put the DWC_ahsata Link into Far-end Retimed mode, without the BIST Activate FIS, regardless whether the device is connected or disconnected (Link in NOCOMM state). This field is one-shot type and reads returns 0.	WO	0
19		**Reserved**	RO	0
18	TXO	**Transmit Only** This bit is used to initiate transmission of one of the non-compliant patterns defined by the BISTCR.PATTERN value when the device is disconnected.	WO	0
17	CNTCLR	**Counter Clear** This bit clears BIST error count registers. This field is one-shot type and reads returns 0. 1: Clear BISTFCTR, BISTSR, and BISTDECR registers.	WO	0
16	NEALB	**Near-End Analog Loopback** This bit places the Port PHY into near-end analog loopback mode. This field is one-shot type and reads returns 0: 1: Near-end analog loopback request. BISTCR.PATTERN field contains the appropriate pattern. This mode should be initiated either in the PARTIAL or SLUMBER power mode, or with the device disconnected from the Port PHY (Link NOCOMM state). BIST Activate FIS is not sent to the device in this mode.	WO	0
15:13		**Reserved**	RO	0

Field	Bit ID	Description	Access	Reset
12	SDFE	**Signal Detect Feature Enable** **Reset:** PHY_INTERFACE_TYPE 1: Link layer feature to handle unstable/absent phy_sig_det signal is enabled 0: Link layer feature to handle unstable/absent phy_sig_det signal is disabled. This bit is set on power-up or asynchronous reset if PHY_INTERFACE_TYPE==Synopsys (1), otherwise, the bit is cleared until it is set via programming. It is not affected by a Global reset or COMRESET. **Note:** For special handling in systems where phy_sig_det may not be present or stable after OOB signalling and during normal operation, refer to Section 3.4.4.2.2 on page 62. For these systems, phy_rx_data_vld must not be tied high and must go low when no data is detected on the wires.	RW	See Description
11		**Reserved**	RO	0
10:8	LLC	**Link Layer Control** This field controls the Port Link Layer functions: scrambler, de-scrambler, and repeat primitive drop. Note the different meanings for normal and BIST modes of operation: • Bit8—SCRAM The options for this field are: - 0: Scrambler disabled in normal mode, enabled in BIST mode - 1: Scrambler enabled in normal mode, disabled in BIST mode • Bit9—DESCRAM The options for this field are: - 0: Descrambler disabled in normal mode, enabled in BIST mode - 1: Descrambler enabled in normal mode, disabled in BIST mode • Bit10—RPD The options for this field are: - 0: Repeat primitive drop function disabled in normal mode, NA in BIST mode. - 1: Repeat primitive drop function enabled in normal mode, NA in BIST mode. The SCRAM bit is cleared (enabled) by the Port when the Port enters a responder far-end transmit BIST mode with scrambling enabled (BISTAFR.PD=0x80). In normal mode, the functions scrambler, descrambler, or RPD can be changed only during Port reset (P#SCTL.DET=0x1)	RW	111b
7		**Reserved**	RO	0
6	ERREN	**Error Enable** This bit is used to allow or filter (disable) PHY internal errors outside the FIS boundary to set corresponding P#SERR bits. The options for this field are: • 0: Filter errors outside the FIS, allow errors inside the FIS; • 1: Allow errors outside or inside the FIS.	RW	0

Field	Bit ID	Description	Access	Reset
5	FLIP	**Flip Disparity** This bit is used to change disparity of the current test pattern to the opposite every time its state is changed by the software.	RW	0
4	PV	**Pattern Version** This bit is used to select either short or long version of the SSOP, HTDP, LTDP, LFSCP, COMP patterns. The options for this field are: • 0: Short pattern version • 1: Long pattern version	RW	0
3:0	PATTERN	This field defines one of the following SATA compliant patterns for far-end retimed/ far-end analog/ near-end analog initiator modes, or non-compliant patterns for transmit-only responder mode when initiated by the software writing to the BISTCR.TXO bit. The options for this field are: • 0000b: Simultaneous switching outputs pattern (SSOP) • 0001b: High transition density pattern (HTDP) • 0010b: Low transition density pattern (LTDP) • 0011b: Low frequency spectral component pattern (LFSCP) • 0100b: Composite pattern (COMP) • 0101b: Lone bit pattern (LBP) • 0110b: Mid frequency test pattern (MFTP) • 0111b: High frequency test pattern (HFTP) • 1000b: Low frequency test pattern (LFTP) All other values are reserved and should not be used. If the value is none of the listed above, Composite pattern (COMP) is transmitted by default.	RW	000b