Schematic Review Form

Jimmy/Arrow

Pin #	Name	Info	Violations	*Description*
4	GRSTz	Actively controlled by TUSB9261_RST. A minimum reset duration of 2 ms is required. This is defined as the time when the power supplies are in the recommended operating range to the deassertion of GRSTz.		Global power reset. This reset brings all of the TUSB9261 internal registers to their default states. When GRSTz is asserted , the device is completely nonfuncitonal.
52	XI	Connected to 1Mohm resistor and 18pF cap. Ensure crystal matches datasheet spec.		Crystal input. This terminal is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal, a 1-Mohm feedback resistor is required between XI and XO.
54	XO	Connected to 1Mohm resistor and 18pF cap. Ensure crystal matches datasheet spec.		Crystal output. This terminal is the crystal output for the internal oscillator. If XI is driven by an external oscillator, this pin may be left unconnected. When using a crystal, a 1-Mohm feedback resistor is required between XI and XO.
31, 30	FREQSEL[1:0]	100K pullup to 3.3V. 40MHz. Recommend using lower value pullup resistors if possible. EVM uses 4.7K		Frequency select. These terminals indicate the oscillator input frequency and are used to configure the correct PLL multiplier. The field encoding is as follows: FREQSEL[1]=1, FREQSEL[0]=1, Input clock frequency=40Mhz.

57	SATA_TXP	OK. Swapped with TXM at connector, matches EVM. 10nF caps.		Serial ATE transmitter differential pair (positive)
56	SATA_TXM	OK. Swapped with TXP at connector, matches EVM. 10nF caps.		Serial ATE transmitter differential pair (negative)
60	SATA_RXP	OK. 10nF caps.		Serial ATE receiver differential pair (positive)
59	SATA_RXM	OK. 10nF caps.		Serial ATE receiver differential pair (negative)
43	USB_SSTXP	100nF caps.		SuperSpeed USB transmitter differential pair (positive)
42	USB_SSTXM	100nF caps.		SuperSpeed USB transmitter differential pair (negative)
46	USB_SSRXP	Do not recommend including 0ohm resistors unless needed. It can negatively affect signal integrity.		SuperSpeed USB transmitter differential pair (positive)
45	USB_SSRXM	Do not recommend including 0ohm resistors unless needed. It can negatively affect signal integrity.		SuperSpeed USB receiver differential pair (negative)
36	USB_DP	OK.		USB high-speed differential transceiver (positive)
35	USB_DM	OK.		USB high-speed differential transceiver (negative)
50	USB_VBUS	Connected to 90.9kohm and 10Kohm voltage divider.		USB bus power

38	USB_R1	Connected to 10Kohm resistor		Precision resistor reference. A 10-kohm +1% resistor should be connected between R1 and R1RTN.
39	USB_R1RTN	Connected to 10Kohm resistor.		Precision resistor reference return.
17	SPI_SCLK	Connected to flash memory. Confirm flash memory is compatible with TUSB9261. Micron M25P10A Winbond W25X20CL Onsemi LE25U20AMB Renesas AT25XE021A		SPI clock
18	SPI_DATA_OUT	Connected to flash memory. Confirm flash memory is compatible with TUSB9261.		SPI master data out
20	SPI_DATA_IN	Connected to flash memory. Confirm flash memory is compatible with TUSB9261.		SPI master data in
21	SPI_CS0	Connected to flash memory. Confirm flash memory is compatible with TUSB9261.		Primary SPI chip select for flash RAM
23	SPI_CS2/GPIO11	SATA drive power enable output		SPI chip select for additional peripherals. When not used for SPI chip select, this pin may be used as a general-purpose I/O.
22	SPI_CS1/GPIO10	Power fault indicator		SPI chip select for additional peripherals. When not used for SPI chip select, this pin may be used as a general-purpose I/O.
25	JTAG_TCK	floating		JTAG test clock
26	JTAG_TDI	floating		JTAG test data in

27	JTAG_TDO	floating		JTAG test data out
28	JTAG_TMS	floating		JTAG test mode select
29	JTAG_TRSTz	floating		JTAG test reset
6	GPIO9/UART_TX	connected to test point		GPIO/UART transmitter. This terminal can be configured as a GPIO or as the transmitter for a UART channel. This pin defaults to a general-purpose output.
5	GPIO8/UART_RX	connected to test point		GPIO/UART receiver. This terminal can be configured as a GPIO or as the receiver for a UART channel. This pin defaults to a general-purpose output.
16	GPIO7	floating		Configurable as a general-purpose inputs/outputs.
15	GPIO6	floating		Configurable as a general-purpose inputs/outputs.
14	GPIO5	floating		Configurable as a general-purpose inputs/outputs.
13	GPIO4	floating		Configurable as a general-purpose inputs/outputs.
11	GPIO3	floating		Configurable as a general-purpose inputs/outputs.
10	GPIO2	floating		Configurable as a general-purpose inputs/outputs.
9	GPIO1	floating		Configurable as a general-purpose inputs/outputs.
8	GPIO0	floating		Configurable as a general-purpose inputs/outputs.
2	PWM0	Hard drive status LED.		Pulse-width modulation (PWM). Can be used to drive status LEDs.

3	PWM1	floating		Pulse-width modulation (PWM). Can be used to drive status LEDs.
1, 12, 19, 32, 33, 42, 47, 49, 55, 61, 63	VDD	Tied to 1.1V with pi power filter.		1.1-V power rail
7, 24, 51	VDD33	Tied to 3.3V with pi power filter.		3.3-V power rail
34, 40, 48, 62	VDDA33	Tied to analog 3.3V with pi power filter.		3.3-V analog power rail
53	VSSOSC	Tied to GND.		Oscillator ground. If using a crystal, this should not be connected to a PCB ground plane. If using an oscillator, this should be connected to PCB ground. See Clock Source Requirements for more details.
44, 58	VSS	Tied to GND.		Ground
65	VSS	Tied to GND.	Do not see thermal pad in symbol.	Ground - Thermal pad
37, 64	NC	floating.		No connect, leave floating

Comments