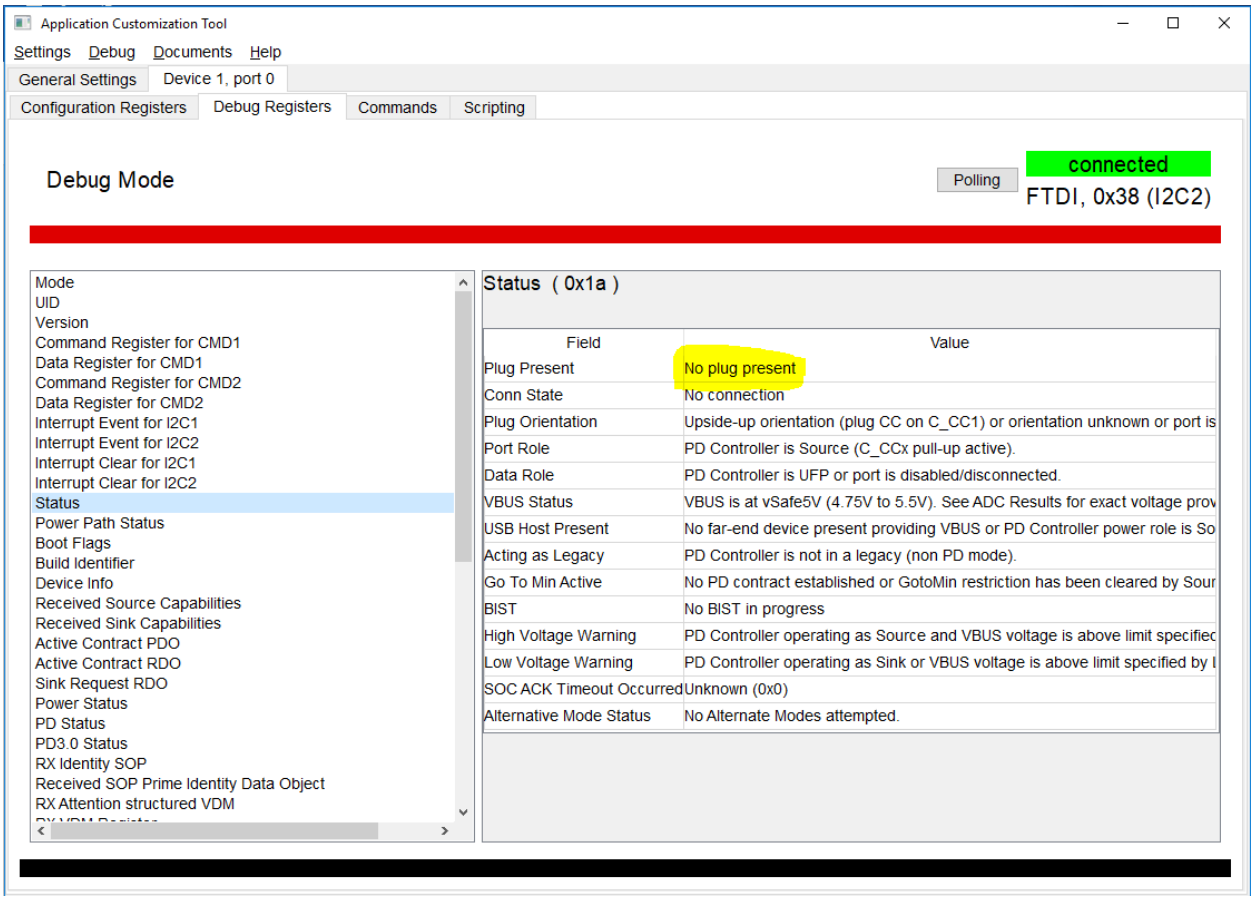
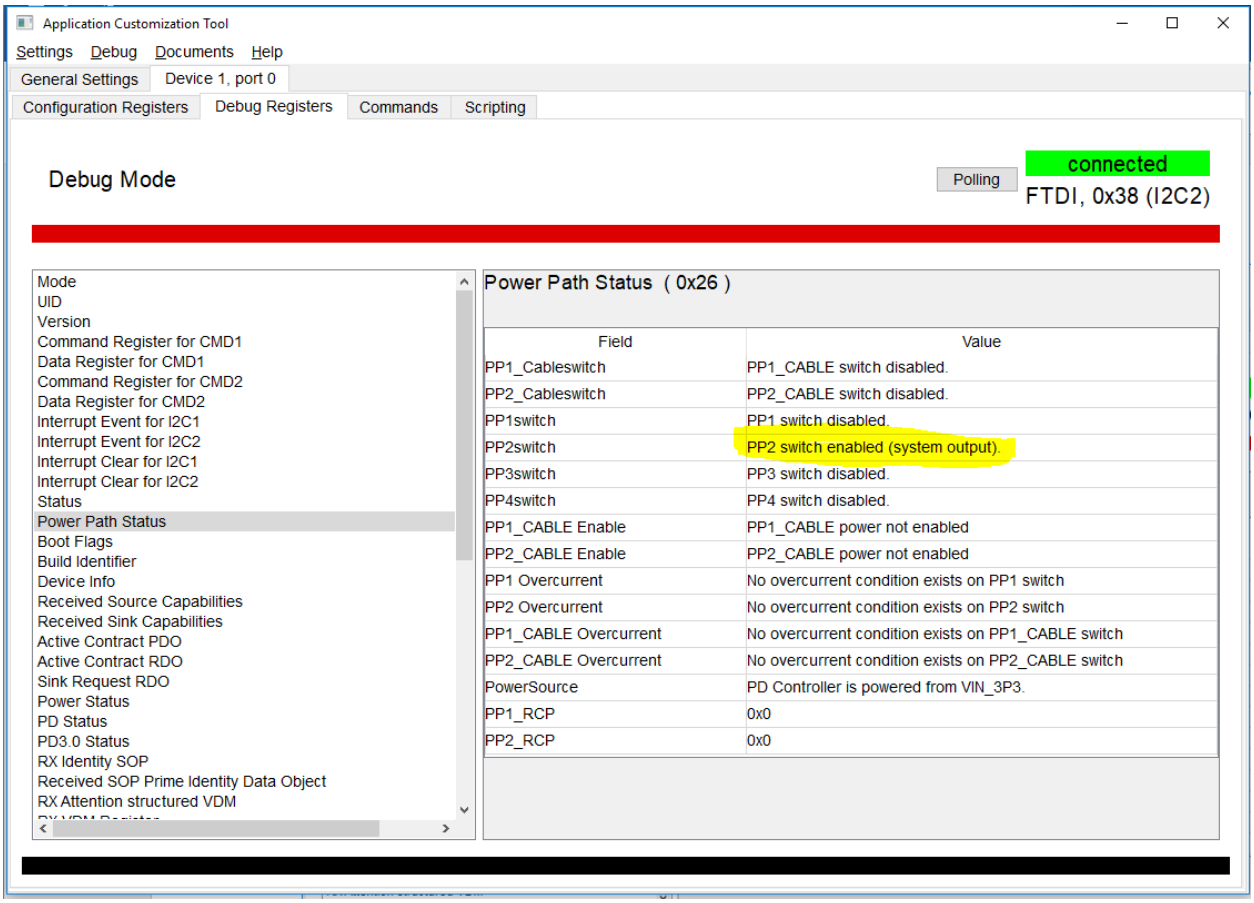
USB-port with PD-ctrl TPS65987D

Status after connection of device with sink 5V, thereafter disconnection of cable.

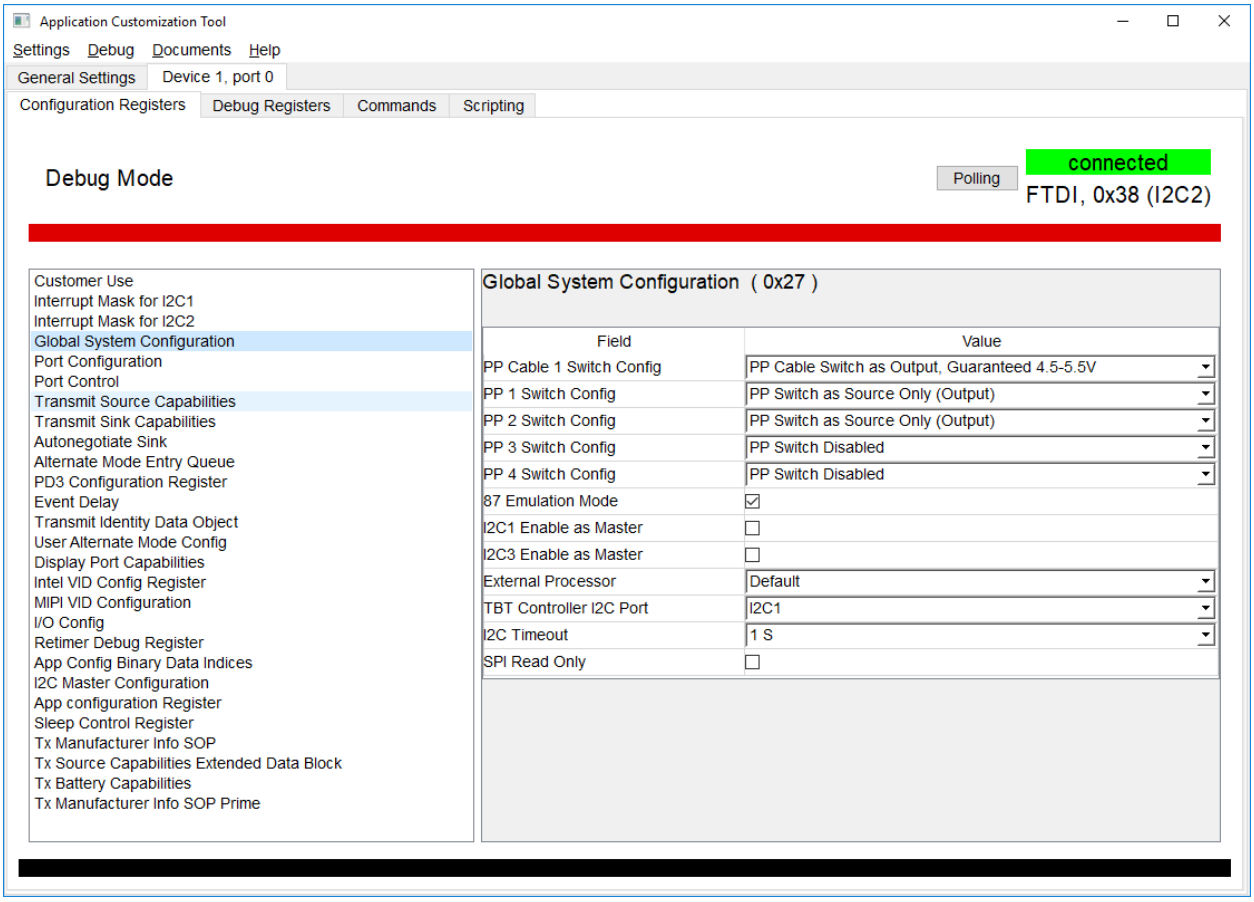
- VBUS = +5V
- 3.3V on CC-signals.

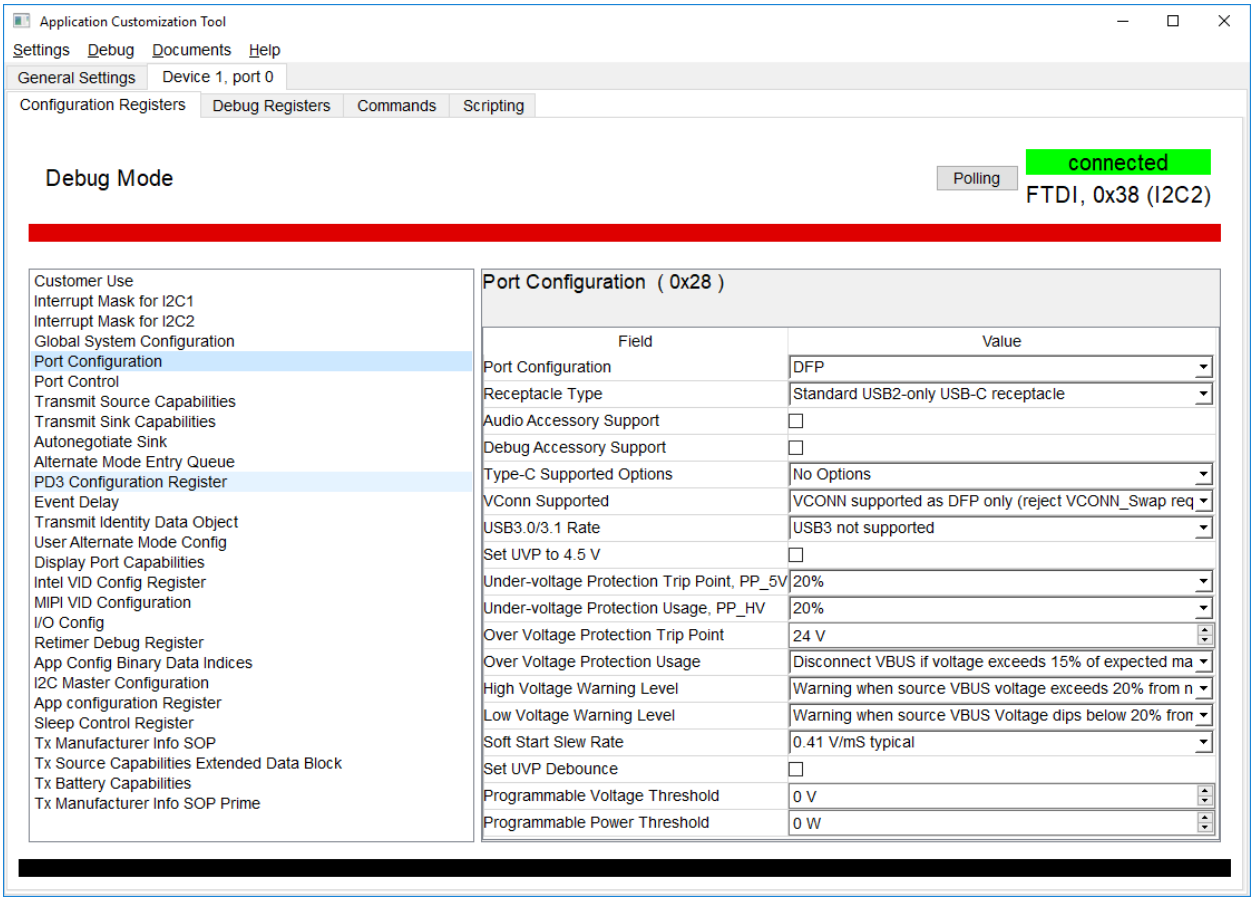



Application Customization Tool
Settings Debug Documents Help
General Settings
Device 1, port 0
Configuration Registers
Debug Registers
Commands
Scripting
Debug Mode
Polling
connected
FTDI, 0x38 (I2C2)
Mode
UID
Version
Command Register for CMD1
Data Register for CMD1
Command Register for CMD2
Data Register for CMD2
Interrupt Event for I2C1
Interrupt Event for I2C2
Interrupt Clear for I2C1
Interrupt Clear for I2C2
Status
Power Path Status
Boot Flags
Build Identifier
Device Info
Received Source Capabilities
Received Sink Capabilities
Active Contract PDO
Active Contract RDO
Sink Request RDO
Power Status
PD Status
PD3.0 Status
RX Identity SOP
Received SOP Prime Identity Data Object
RX Attention structured VDM
Power Path Status (0x26)
Field
Value
PP1_Cableswitch
PP1_CABLE switch disabled.
PP2_Cableswitch
PP2_CABLE switch disabled.
PP1switch
PP1 switch disabled.
PP2switch
PP2 switch enabled (system output).
PP3switch
PP3 switch disabled.
PP4switch
PP4 switch disabled.
PP1_CABLE Enable
PP1_CABLE power not enabled
PP2_CABLE Enable
PP2_CABLE power not enabled
PP1 Overcurrent
No overcurrent condition exists on PP1 switch
PP2 Overcurrent
No overcurrent condition exists on PP2 switch
PP1_CABLE Overcurrent
No overcurrent condition exists on PP1_CABLE switch
PP2_CABLE Overcurrent
No overcurrent condition exists on PP2_CABLE switch
PowerSource
PD Controller is powered from VIN_3P3.
PP1_RCP
0x0
PP2_RCP
0x0

Configuration status.

(Configuration downloaded from CPU, flash empty.)




Application Customization Tool
Settings Debug Documents Help
General Settings
Device 1, port 0
Configuration Registers
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Scripting
Debug Mode
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connected
FTDI, 0x38 (I2C2)
Customer Use
Interrupt Mask for I2C1
Interrupt Mask for I2C2
Global System Configuration
Port Configuration
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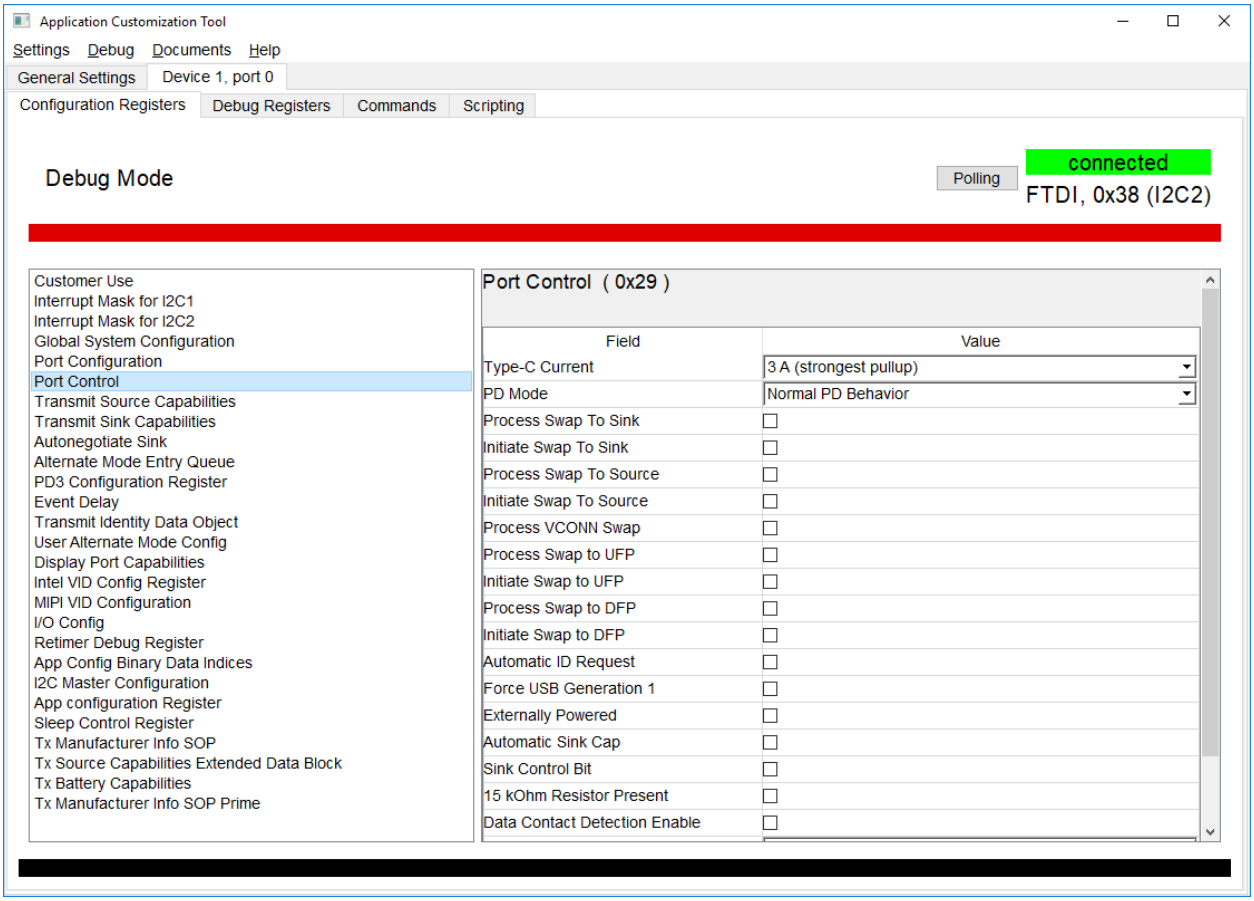
Transmit Source Capabilities
Transmit Sink Capabilities
Autonegotiate Sink
Alternate Mode Entry Queue
PD3 Configuration Register
Event Delay
Transmit Identity Data Object
User Alternate Mode Config
Display Port Capabilities
Intel VID Config Register
MIPI VID Configuration
I/O Config
Retimer Debug Register
App Config Binary Data Indices
I2C Master Configuration
App configuration Register
Sleep Control Register
Tx Manufacturer Info SOP
Tx Source Capabilities Extended Data Block
Tx Battery Capabilities
Tx Manufacturer Info SOP Prime
Port Configuration (0x28)
Field
Value
Port Configuration
DFP
Receptacle Type
Standard USB2-only USB-C receptacle
Audio Accessory Support
Debug Accessory Support
Type-C Supported Options
No Options
VConn Supported
VCONN supported as DFP only (reject VCONN_Swap req
USB3.0/3.1 Rate
USB3 not supported
Set UVP to 4.5 V
Under-voltage Protection Trip Point, PP_5V
20%
Under-voltage Protection Usage, PP_HV
20%
Over Voltage Protection Trip Point
24 V
Over Voltage Protection Usage
Disconnect VBUS if voltage exceeds 15% of expected ma
High Voltage Warning Level
Warning when source VBUS voltage exceeds 20% from n
Low Voltage Warning Level
Warning when source VBUS Voltage dips below 20% fron
Soft Start Slew Rate
0.41 V/mS typical
Set UVP Debounce
Programmable Voltage Threshold
0 V
Programmable Power Threshold
0 W


Application Customization Tool
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Device 1, port 0
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Scripting
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connected
FTDI, 0x38 (I2C2)
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Interrupt Mask for I2C2
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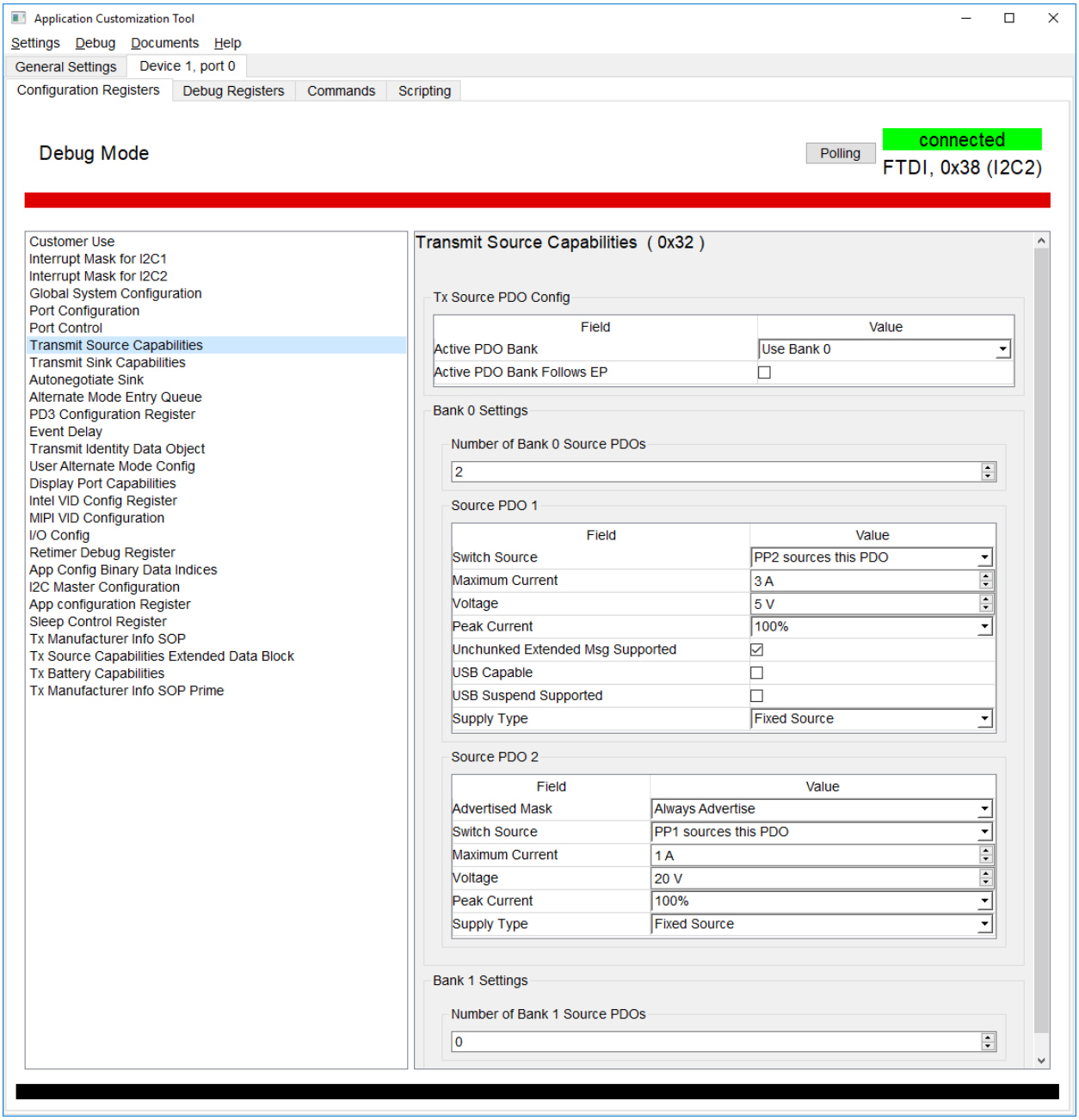
Transmit Sink Capabilities
Autonegotiate Sink
Alternate Mode Entry Queue
PD3 Configuration Register
Event Delay
Transmit Identity Data Object
User Alternate Mode Config
Display Port Capabilities
Intel VID Config Register
MIPI VID Configuration
I/O Config
Retimer Debug Register
App Config Binary Data Indices
I2C Master Configuration
App configuration Register
Sleep Control Register
Tx Manufacturer Info SOP
Tx Source Capabilities Extended Data Block
Tx Battery Capabilities
Tx Manufacturer Info SOP Prime
Port Control (0x29)
Field
Value
Type-C Current
3 A (strongest pullup)
PD Mode
Normal PD Behavior
Process Swap To Sink
Initiate Swap To Sink
Process Swap To Source
Initiate Swap To Source
Process VCONN Swap
Process Swap to UFP
Initiate Swap to UFP
Process Swap to DFP
Initiate Swap to DFP
Automatic ID Request
Force USB Generation 1
Externally Powered
Automatic Sink Cap
Sink Control Bit
15 kOhm Resistor Present
Data Contact Detection Enable


Application Customization Tool
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General Settings
Device 1, port 0
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Scripting
Debug Mode
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connected
FTDI, 0x38 (I2C2)
Customer Use
Interrupt Mask for I2C1
Interrupt Mask for I2C2
Global System Configuration
Port Configuration
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Transmit Source Capabilities
Transmit Sink Capabilities
Autonegotiate Sink
Alternate Mode Entry Queue
PD3 Configuration Register
Event Delay
Transmit Identity Data Object
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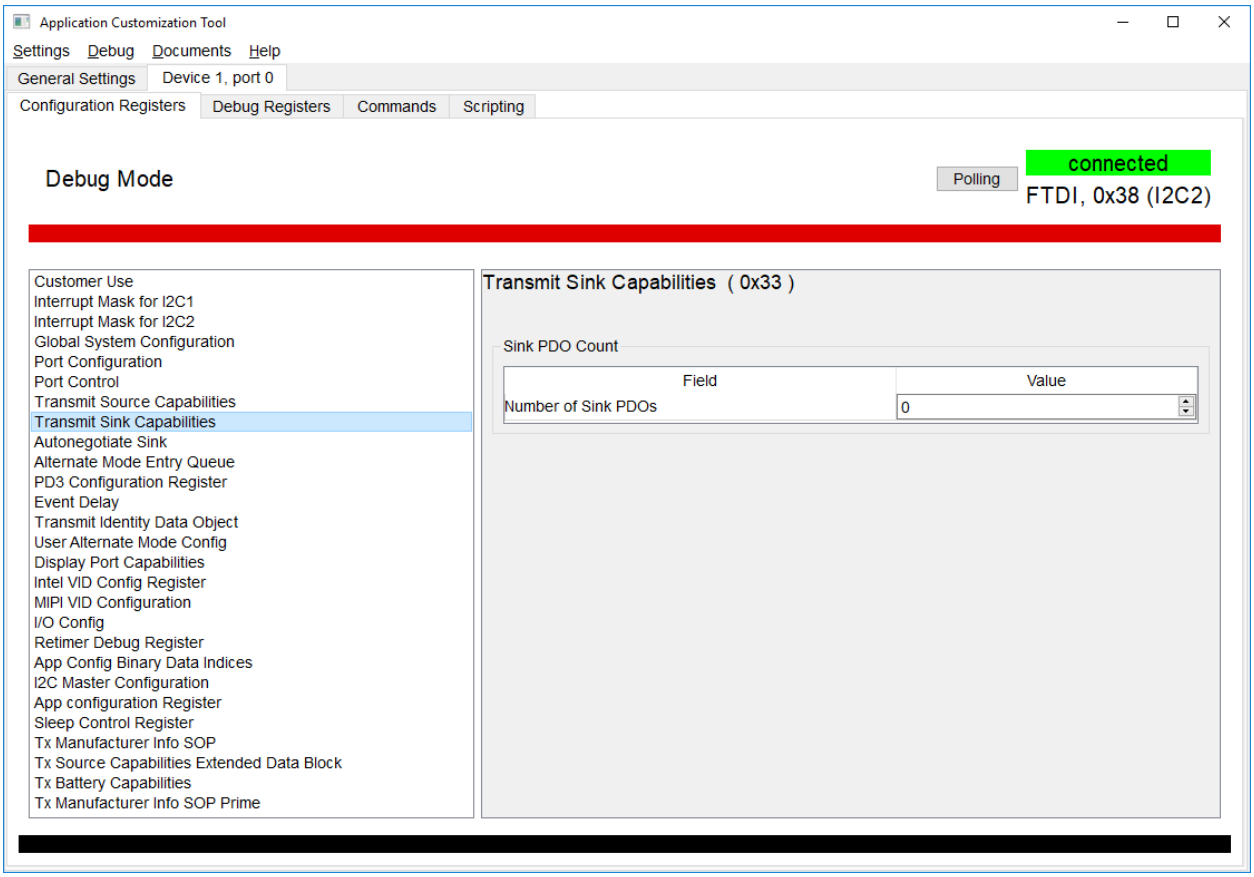
Display Port Capabilities
Intel VID Config Register
MIPI VID Configuration
I/O Config
Retimer Debug Register
App Config Binary Data Indices
I2C Master Configuration
App configuration Register
Sleep Control Register
Tx Manufacturer Info SOP
Tx Source Capabilities Extended Data Block
Tx Battery Capabilities
Tx Manufacturer Info SOP Prime
Transmit Source Capabilities (0x32)
Tx Source PDO Config
Field
Value
Active PDO Bank
Use Bank 0
Active PDO Bank Follows EP
Bank 0 Settings
Number of Bank 0 Source PDOs
2
Source PDO 1
Field
Value
Switch Source
PP2 sources this PDO
Maximum Current
3 A
Voltage
5 V
Peak Current
100%
Unchunked Extended Msg Supported
USB Capable
USB Suspend Supported
Supply Type
Fixed Source
Source PDO 2
Field
Value
Advertised Mask
Always Advertise
Switch Source
PP1 sources this PDO
Maximum Current
1 A
Voltage
20 V
Peak Current
100%
Supply Type
Fixed Source
Bank 1 Settings
Number of Bank 1 Source PDOs
0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Device 1, port 0
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Debug Registers
Commands
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Polling
connected
FTDI, 0x38 (I2C2)
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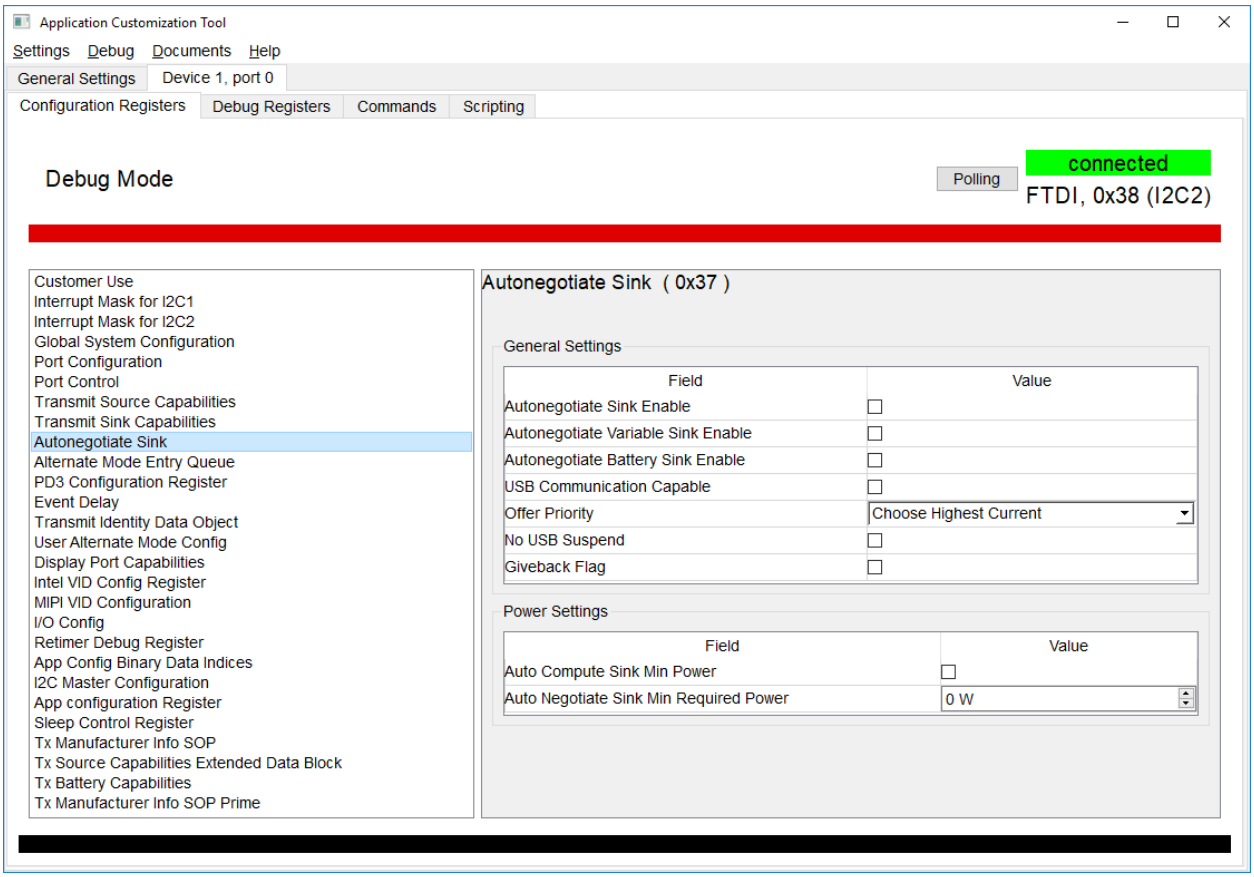
Interrupt Mask for I2C1
Interrupt Mask for I2C2
Global System Configuration
Port Configuration
Port Control
Transmit Source Capabilities
Transmit Sink Capabilities
Autonegotiate Sink
Alternate Mode Entry Queue
PD3 Configuration Register
Event Delay
Transmit Identity Data Object
User Alternate Mode Config
Display Port Capabilities
Intel VID Config Register
MIPI VID Configuration
I/O Config
Retimer Debug Register
App Config Binary Data Indices
I2C Master Configuration
App configuration Register
Sleep Control Register
Tx Manufacturer Info SOP
Tx Source Capabilities Extended Data Block
Tx Battery Capabilities
Tx Manufacturer Info SOP Prime
Transmit Sink Capabilities (0x33)
Sink PDO Count
Field
Value
Number of Sink PDOs
0


Application Customization Tool
Settings Debug Documents Help
General Settings
Device 1, port 0
Configuration Registers
Debug Registers
Commands
Scripting
Debug Mode
Polling
connected
FTDI, 0x38 (I2C2)
Customer Use
Interrupt Mask for I2C1
Interrupt Mask for I2C2
Global System Configuration
Port Configuration
Port Control
Transmit Source Capabilities
Transmit Sink Capabilities
Autonegotiate Sink
Alternate Mode Entry Queue
PD3 Configuration Register
Event Delay
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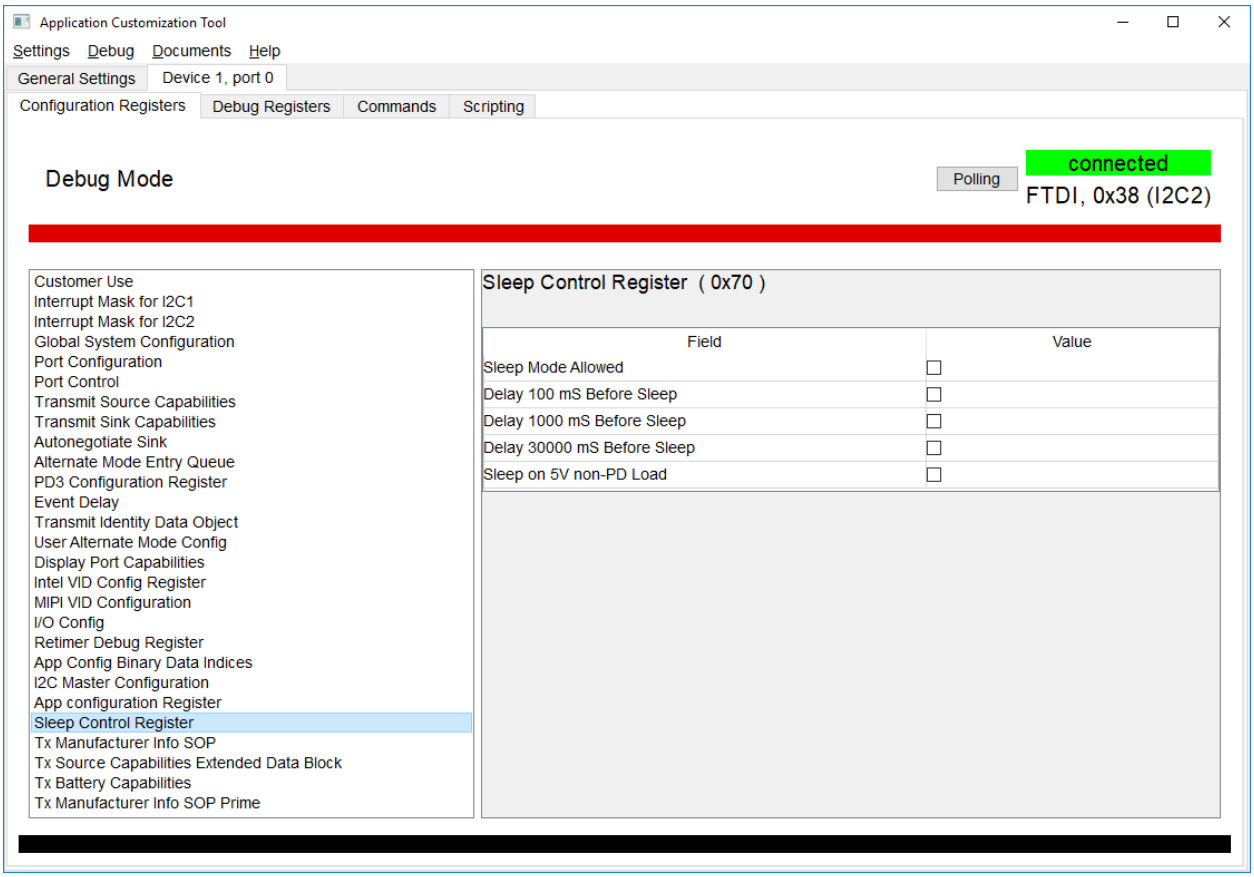
Display Port Capabilities
Intel VID Config Register
MIPI VID Configuration
I/O Config
Retimer Debug Register
App Config Binary Data Indices
I2C Master Configuration
App configuration Register
Sleep Control Register
Tx Manufacturer Info SOP
Tx Source Capabilities Extended Data Block
Tx Battery Capabilities
Tx Manufacturer Info SOP Prime
Autonegotiate Sink (0x37)
General Settings
Field
Value
Autonegotiate Sink Enable
Autonegotiate Variable Sink Enable
Autonegotiate Battery Sink Enable
USB Communication Capable
Offer Priority
Choose Highest Current
No USB Suspend
Giveback Flag
Power Settings
Field
Value
Auto Compute Sink Min Power
Auto Negotiate Sink Min Required Power
0 W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Interrupt Mask for I2C2
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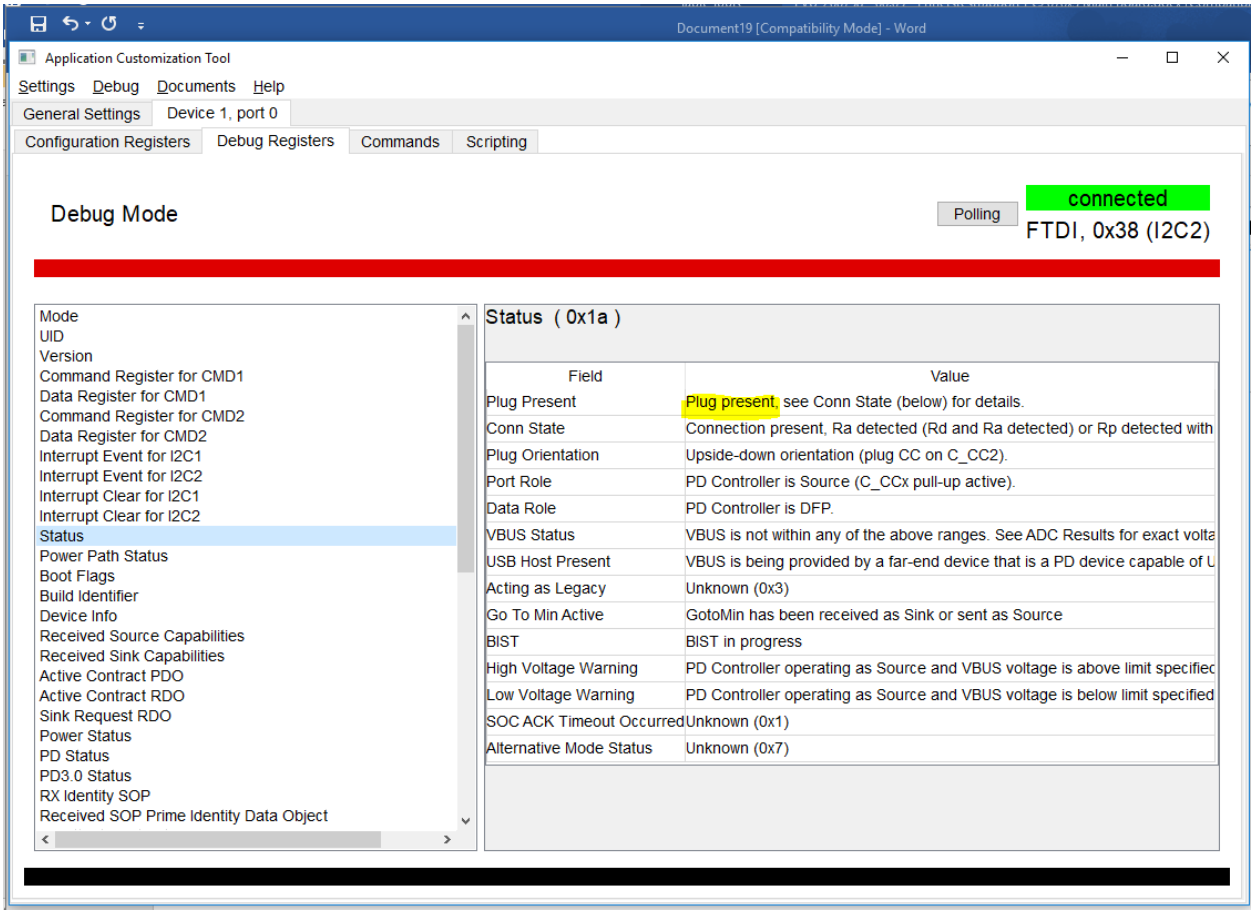
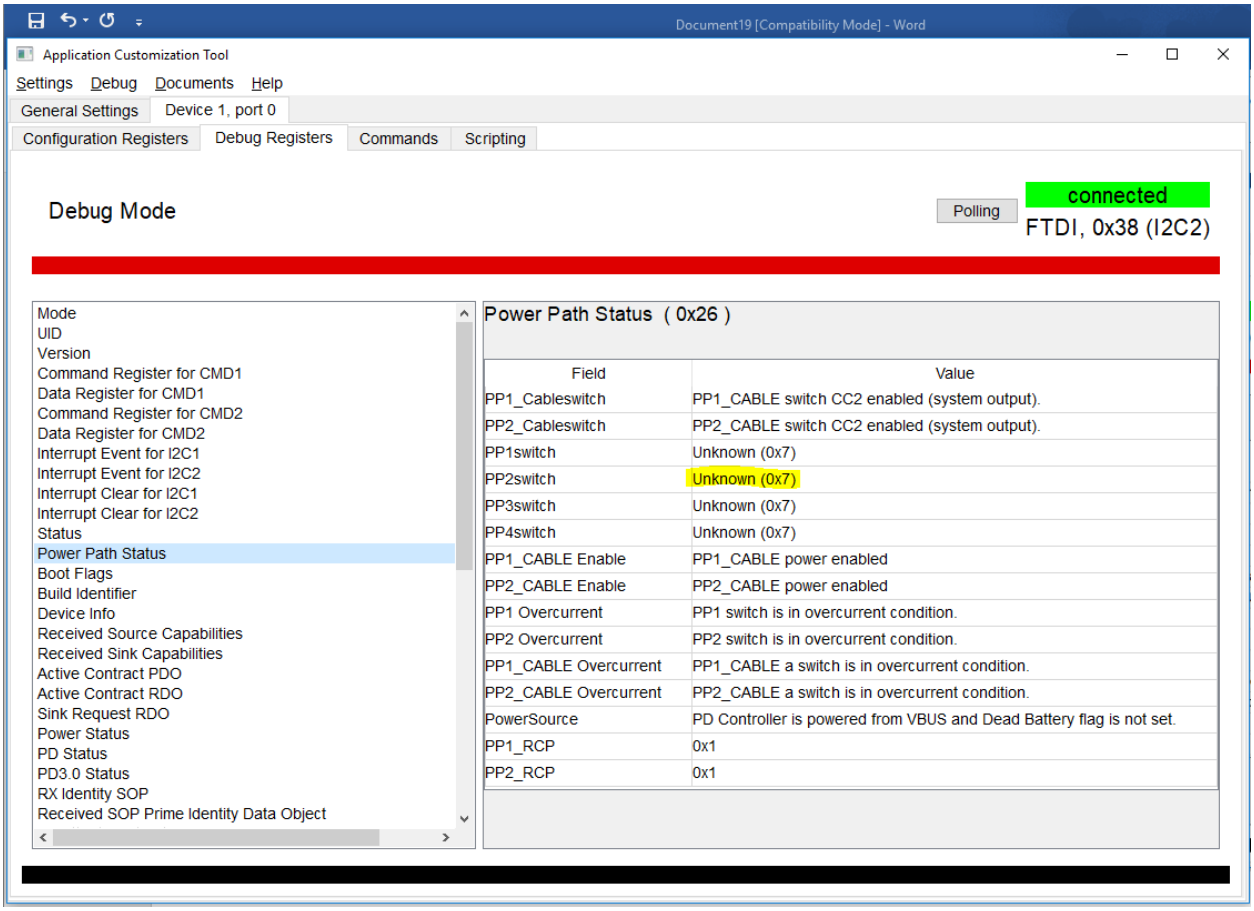
Port Configuration
Port Control
Transmit Source Capabilities
Transmit Sink Capabilities
Autonegotiate Sink
Alternate Mode Entry Queue
PD3 Configuration Register
Event Delay
Transmit Identity Data Object
User Alternate Mode Config
Display Port Capabilities
Intel VID Config Register
MIPI VID Configuration
I/O Config
Retimer Debug Register
App Config Binary Data Indices
I2C Master Configuration
App configuration Register
Sleep Control Register
Tx Manufacturer Info SOP
Tx Source Capabilities Extended Data Block
Tx Battery Capabilities
Tx Manufacturer Info SOP Prime
Sleep Control Register (0x70)
Field
Value
Sleep Mode Allowed
Delay 100 mS Before Sleep
Delay 1000 mS Before Sleep
Delay 30000 mS Before Sleep
Sleep on 5V non-PD Load

If USB-cable is connected in this status, C1-signal is 3.3V and C2-signal 1.7V, VBUS +5V.

Status




Document19 [Compatibility Mode] - Word
Application Customization Tool
Settings Debug Documents Help
General Settings
Device 1, port 0
Configuration Registers
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Commands
Scripting
Debug Mode
Polling
connected
FTDI, 0x38 (I2C2)
Mode
UID
Version
Command Register for CMD1
Data Register for CMD1
Command Register for CMD2
Data Register for CMD2
Interrupt Event for I2C1
Interrupt Event for I2C2
Interrupt Clear for I2C1
Interrupt Clear for I2C2
Status
Power Path Status
Boot Flags
Build Identifier
Device Info
Received Source Capabilities
Received Sink Capabilities
Active Contract PDO
Active Contract RDO
Sink Request RDO
Power Status
PD Status
PD3.0 Status
RX Identity SOP
Received SOP Prime Identity Data Object
Power Path Status (0x26)
Field
Value
PP1_Cableswitch
PP1_CABLE switch CC2 enabled (system output).
PP2_Cableswitch
PP2_CABLE switch CC2 enabled (system output).
PP1switch
Unknown (0x7)
PP2switch
Unknown (0x7)
PP3switch
Unknown (0x7)
PP4switch
Unknown (0x7)
PP1_CABLE Enable
PP1_CABLE power enabled
PP2_CABLE Enable
PP2_CABLE power enabled
PP1 Overcurrent
PP1 switch is in overcurrent condition.
PP2 Overcurrent
PP2 switch is in overcurrent condition.
PP1_CABLE Overcurrent
PP1_CABLE a switch is in overcurrent condition.
PP2_CABLE Overcurrent
PP2_CABLE a switch is in overcurrent condition.
PowerSource
PD Controller is powered from VBUS and Dead Battery flag is not set.
PP1_RCP
0x1
PP2_RCP
0x1