Using EDID in FPD-Link Devices

FPD-Link™ Product Line

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TEXAS INSTRUMENTS

What is EDID

- **EDID** (Extended Display Identification Data) is the information provided by a display to the video source describing the display's capabilities. This allows the video source to then send out a video signal that is supported by that display.

- The DS90Ux949/929 supports several options for delivering display identification (EDID) information to the HDMI source:
  1. Internal pre-programmed EDID
  2. Internal EDID loaded into device memory
  3. External local EDID (EEPROM)
  4. Remote EDID connected to I2C bus at Deserializer side

- The selected EDID mode should be configurable from either the MODE_SEL pins or from internal control registers. For all modes, the EDID information should be accessible at the default address of 0xA0 (8-bit address = 0x50 in 7-bit format).

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Supported EDID Options

1) Internal pre-programmed EDID

• The Fuse Rom includes 256 bytes of data to store a default program for the EDID SRAM. The value is automatically loaded from the fuse ROM to the EDID SRAM at initialization.

• The default EDID stored in the DS90Ux949/929 works with a range of video sources. This information is provided to the HDMI source over the HDMI DDC and comply with the DDC and EDID requirements given in the HDMI v1.4b specification.

2) Internal EDID memory (SRAM)

• The DS90Ux949/929 also allows uploading a specific EDID information into the device internal memory, telling the video source to provide the required output, or adding a custom resolution or timing that is not in the default EDID.

• This SRAM storage is volatile and requires loading from an external I2C master (local or remote).

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Supported EDID Options

- The new EDID information must be allowable by the HDMI v1.4b and DVI 1.0 standards

- The internal EDID is loadable and readable (local/remote) from control registers during normal operation.

3) External local EDID (EEPROM)

- The DS90Ux949/929 can be configured to allow a local EEPROM EDID device. The local EDID device may implement any EDID configuration allowable by the HDMI v1.4b and DVI 1.0 standards.

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Supported EDID Options

4) External remote EDID

- The DS90Ux949/929 can be configured to automatically accesses the Bidirectional Control Channel to search for an EDID EEPROM located at the downstream Deserializer's local I2C bus. If so enabled, the Serializer automatically search for the EDID information at the default EDID I2C address 0xA0 (8-bit address). Once found, the Serializer copies the remote EDID information into the local EDID SRAM.

- The remote EDID device can be a standalone I2C EEPROM, or integrated into the digital display panel.

- In this mode, to load external EDID from the EEPROM at the remote display, set the Serializer's MODE_SEL0 = 1. For MODE_SEL1, REM_EDID_LOAD = 1 and EXT_CTL = 1 must be set as well.

- Remote EDID Load is disabled by setting Register 0x54[5] = 1. Note: this is a strap bit, so the value is loaded from the MODE_SEL1 pin at power-up.

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Remote EDID access's Impact on Display system

- When using the Remote EDID option, the Serializer automatically search for the EDID information at the default EDID I2C address 0xA0 (8-bit address) on the downstream Deserializer's local I2C bus and copies the remote EDID information into the local EDID SRAM.

- *What does that means for the Deserialize's board designer?*

- The Deserializer's board designer needs to know that once the Deserializer is powered-on, i.e. PDB is enabled, the Serilaizer will access the Deserializer's local I2C bus within less than 1ms, looking for the address 0xA0 (8-bit address).

- At this point the local I2C master must be made aware of this remote access to avoid any I2C collisions.

- The other option to avoid collisions is to ensure that all I2C masters on the bus support multi-master arbitration, as mentioned in the data sheets.

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Accessing EDID SRAM via I2C

- EDID SRAM data is accessible from the I2C interface on the device through an indirect register access mechanism provided by the APB Interface registers.

- The APB Interface registers consist of a control register (Reg 0x48), address registers (Reg 0x49, 0x4A) and data registers (Reg 0x4B – 0x4E).

- The address registers provide the byte offset to the EDID SRAM.

- When accessing EDID SRAM, only the first data register (Reg 0x4B) is used since the interface is 8-bits.

- When using the APB interface, the APB must be enabled in reg 0x48[0]. If desired, automatic incrementing of the register address may be enabled by setting reg 0x48[2]. This will cause the APB address to be incremented by 1 following an APB read or write.

- For EDID SRAM accesses, Reg 0x48[4:3] should be set to a value of 01 to select EDID SRAM.

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Accessing EDID SRAM via I2C

The process for <u>reading</u> EDID SRAM is as follows:

1) Write to Reg 0x49 to set the 8-bit register address.

2) Set Reg 0x48[1]. This will initiate the APB Interface read. Reg 0x48[0] must also be set during any write to reg 0x48, while the Reg 0x48[4:3] must be set to 01. If desired, the APB auto increment bit (Reg 0x48[2]) may be set to enable the auto-increment function.

3) Read the first APB data register (Reg 0x4B).

4) If APB auto increment bit was set, the next register location may be read by repeating steps 2 and 3, otherwise repeat steps 1-3 to read another register location.

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Accessing EDID SRAM via I2C

The process for <u>writing</u> the EDID SRAM is as follows:

1) Set Reg 0x48[0] to enable APB. This bit should remain set through remainder of procedure. Reg 0x48[4:3] should be set to 01. If desired, the auto increment bit (Reg 0x48[2]) may be set to enable the auto-increment function.

2) Write to Reg 0x49 to set the 8-bit register address.

3) Write the 8-bit data to Reg 0x4B. The APB Interface write will occur once this register has been written.

4) If APB auto increment bit is set, the next register location may be written by repeating step 2, otherwise repeat steps 1 and 2 to write another register location.

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Reading EDID SRAM via DDC

- The HDMI DDC interface is a simple I2C interface which allows access to the EDID information for an upstream HDMI Transmitter.

- After initialization, if the DDC interface is enabled, the 256-byte EDID structure can be read using the DDC interface directly.

- By default the EDID structure will be located at a slave address of 0xA0 (8-bit address). This address location can be changed by changing the value in Reg 0x51.

- By default the interface is read-only, but can be made writable by clearing bit 0 of Reg 0x51.

- The interface is a standard I2C slave interface capable at operating with Standard-mode or Fast-mode timing.

- The DDC interface to the EDID SRAM can be disabled by setting Reg 0x4F[0].

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MODE_SEL Pins

- The DS90Ux949/929 support different mode variables decoded from the MODE_SEL[1:0] pins. These values will be latched into register location during power-up.

- In <u>MODE_SEL0</u> there is the option to select the used EDID:
  - Strap low=0, to look for remote EDID, if none found, use internal EDID SRAM. Can be overridden from register 0x4F[0]. Remote EDID address may be overridden from default 0xA0 (8-bit address).
  - Strap high=1, to use external local EDID
  - Can be overridden in Reg 0x4F[0]:
    - 0 = (Default) Enable access to the EDID SRAM via the HDMI DDC interface
    - 1 = Disable access to the EDID SRAM via the HDMI DDC interface

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MODE_SEL Pins

- In <u>MODE_SEL1</u> there is the option to load the remote EDID into the SRAM or not:
  - Strap low=0, EDID SRAM is loaded from eFuse program
  - Strap high=1, EDID SRAM is loaded from remote EDID if available
  - Can be overridden in Reg 0x54[5]:
    - 0 = (Default) The Serializer will check the remote I2C bus for an EEPROM with a valid EDID, and load the EDID data to local EDID SRAM.
    - 1 = Disables automatic load of EDID SRAM from a remote EDID EEPROM.

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MODE_SEL Pins Settings Summery

MODE_SEL 0		MODE_SEL 1		Function	Comment
Strap	Reg 0x4F[0]	Strap	Reg 0x54[5]		
0	0	1	0	Enable access to the EDID SRAM via the HDMI DDC interface & EDID SRAM is loaded from remote EDID if available	The Serializer will check the remote I2C bus for an EEPROM with a valid EDID, and load the data to internal EDID SRAM. If none found, the SoC will use the internal EDID SRAM
1	1	0	1	The EDID SRAM is loaded from eFuse program, but the access to the EDID SRAM via the HDMI DDC interface is disabled	This will disable automatic load of EDID SRAM from a remote EDID EEPROM, so the SoC will use the External local EDID
0	0	0	1	Enable access to the EDID SRAM via the HDMI DDC interface & The EDID SRAM is loaded from eFuse program	No automatic load of EDID SRAM from a remote EDID EEPROM, so the SoC will use the Internal EDID SRAM
1	1	1	0	Disable access to the EDID SRAM via the HDMI DDC interface & EDID SRAM is loaded from remote EDID if available	SoC will have no access to the Internal EDID SRAM, so It must be connected directly to a local EDID EEPROM via I2C

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EDID Configuration Registers

- Reg 0x4F[2:0]
  - [2] EDID_CLEAR: Set to 1 to enable clearing the EDID SRAM. The EDID_INIT bit must be set at the same time for the clear to occur. This bit will be cleared when the initialization is complete.
  - [1] EDID_INIT: Write 1 to start reloading the EDID SRAM from the non-volatile EDID EEPROM. This bit will be cleared when the initialization is complete.
  - [0] EDID_DISABLE: Setting to 1 disables access to the EDID SRAM via the HDMI DDC interface. This value is loaded from the MODE_SEL0 pin at power-up.

- Reg 0x50[3] and [0]
  - [3] REM_EDID_LOAD: Indicates EDID SRAM has been loaded from a remote EDID EEPROM device over the Bidirectional Control Channel.
  - [0] EDID_CKSUM: indicates if the EDID load from a remote EDID EEPROM device during initialization was successful.

EDID Configuration Registers

- Reg 0x51 EDID ID Register: The EDID ID Register provides the I2C address used by the HDMI Transmitter to access the EDID memory structure using the DDC/I2C interface.
  - [7:1] EDID_ID: I2C address used for accessing the EDID information. These are the upper 7 bits in 8-bit format addressing, where the lowest bit is the Read/Write control.
  - [0] EDID Read Only: Set to a 1 puts the EDID SRAM memory in read-only mode for access via the HDMI DDC interface. Setting to a 0 allows writes to the EDID SRAM memory.

- Reg 0x54[5] Disable Remote EDID load: Writing this bit disables the automatic load of EDID SRAM from a remote EDID EEPROM.
  - By default, the device will check the remote I2C bus for an EEPROM with a valid EDID, and load the EDID data to local EDID SRAM. If this bit is set to a 1, the remote EDID load will be bypassed. This value is loaded from the MODE_SEL1 pin at power-up.

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