XIO2001 Power-Up Sequence

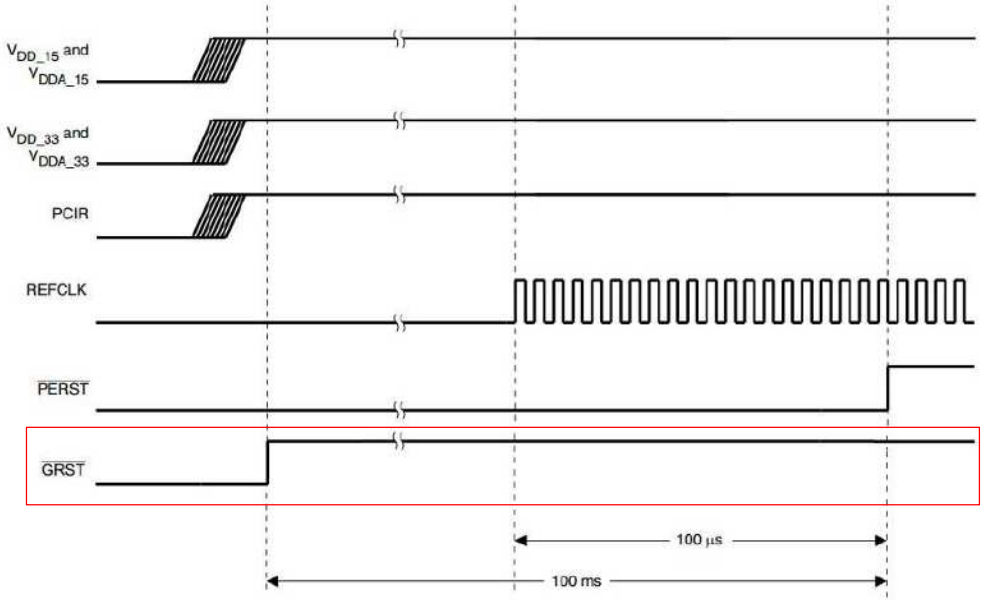

Figure 4. Power-Up Sequence

6.12.1 Power-Up Sequence

1. Assert GRST and PERST to the device.
2. Apply 1.5-V and 3.3-V voltages.
3. Deassert GRST.
4. Apply a stable PCI Express reference clock.
5. To meet PCI Express specification requirements, PERST cannot be deasserted until the following two delay requirements are satisfied:
   - Wait a minimum of 100 µs after applying a stable PCI Express reference clock. The 100-µs limit satisfies the requirement for stable device clocks by the deassertion of PERST.
   - Wait a minimum of 100 ms after applying power. The 100-ms limit satisfies the requirement for stable power by the deassertion of PERST.

XIO31300 Power-Up Sequence

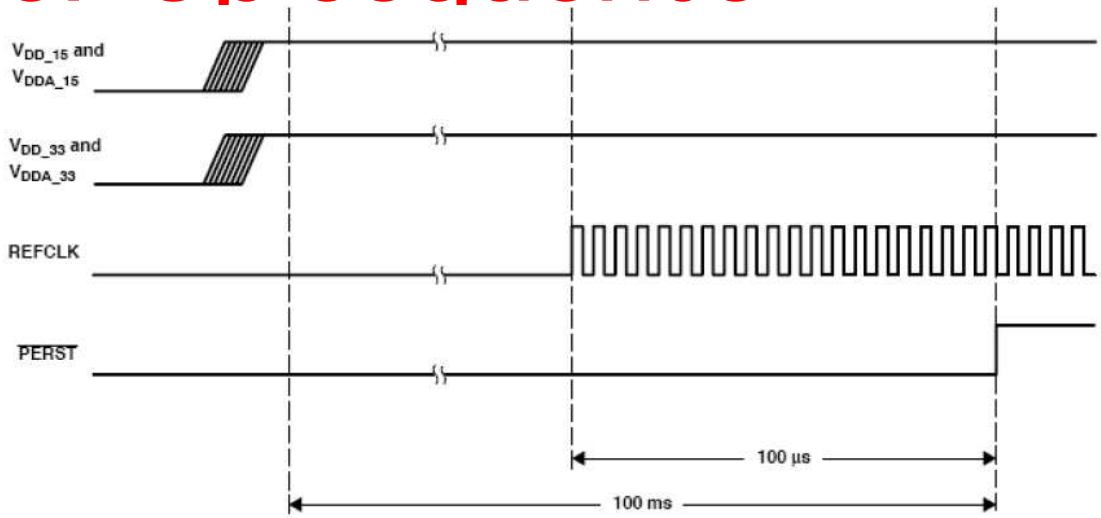

Figure 3-2. Power-Up Sequence Diagram

3.1.1 Power-Up Sequence

1. Assert $\overline{\text{PERST}}$ to the device.
2. Apply 1.5-V and 3.3-V voltages in any order with any time relationship and with any ramp rate.
3. Apply a stable PCI Express reference clock.

To meet PCI Express specification requirements, $\overline{\text{PERST}}$ cannot be de-asserted until the following two delay requirements are satisfied:

- Wait a minimum of 100 µs after applying a stable PCI Express reference clock. The 100-µs limit satisfies the requirement for stable device clocks by the de-assertion of $\overline{\text{PERST}}$.
- Wait a minimum of 100 ms after applying power. The 100-ms limit satisfies the requirement for stable power by the de-assertion of $\overline{\text{PERST}}$.

XIO2001 Power-Down Sequence

6.12.2 Power-Down Sequence

1. Assert $\overline{\text{PERST}}$ to the device.
2. Remove the reference clock.
3. Remove PCIR clamp voltage.
4. Remove 3.3-V and 1.5-V voltages.

See the power-down sequencing diagram in Figure 5. If the $V_{DD\_33\_AUX}$ terminal is to remain powered after a system shutdown, then the bridge power-down sequence is exactly the same as shown in Figure 5.

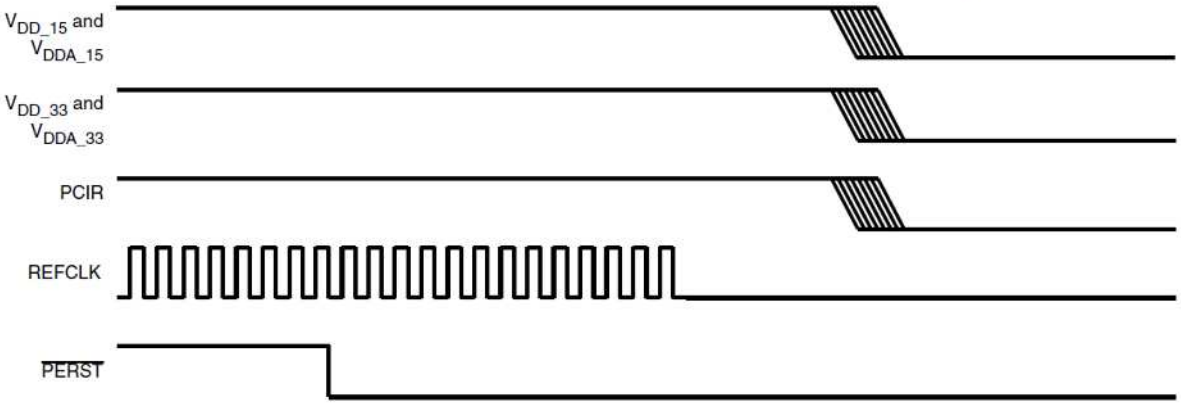

Figure 5. Power-Down Sequence

XIO31300 Power-Down Sequence

3.1.2 Power-Down Sequence

- Assert $\overline{\text{PERST}}$ to the device.
- Remove the reference clock.
- Remove 3.3-V and 1.5-V voltages.

See the power-down sequence diagram in Figure 3-3. If the VAUX33REF terminal is to remain powered after a system shutdown, the switch power-down sequence is exactly the same as shown in Figure 3-3.

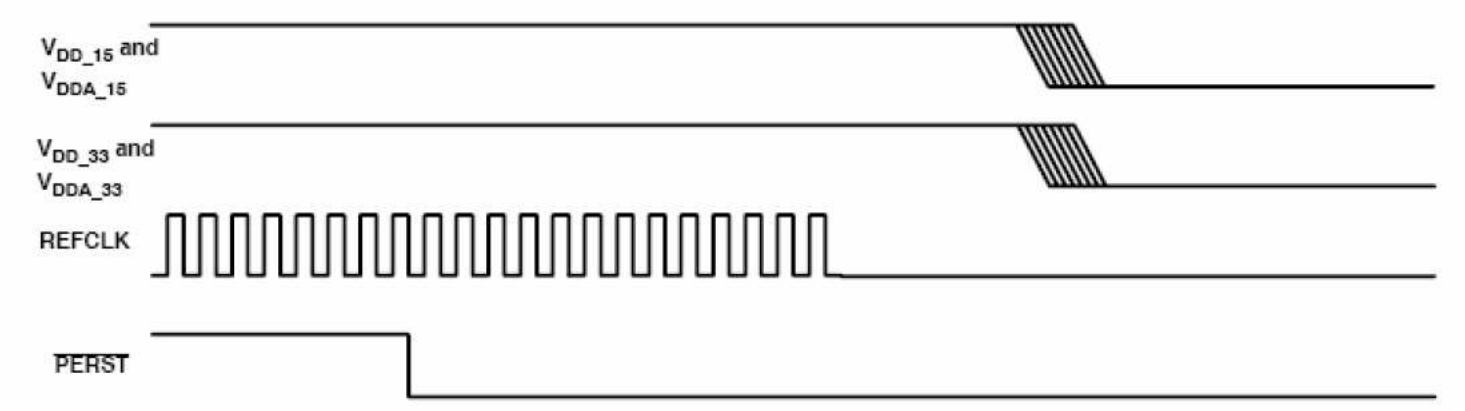

Figure 3-3. Power-Down Sequence Diagram