AN 952: Intel® Arria® 10 and Intel® Stratix® 10 HDMI 2.1 System Design Guidelines

Updated for Intel® Quartus® Prime Design Suite: **22.2**

Contents

1. Terms and Acronyms

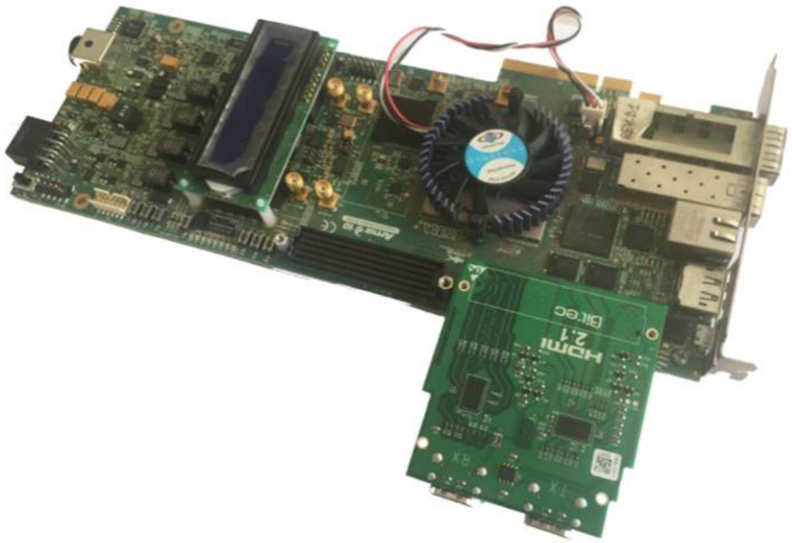
Table 1. Acronyms

Term	Definition
ALA	Advanced Link Analyzer
ATXPLL	ATX Phase Lock Loop
BUJ	Bounded, Uncorrelated Jitter
CTS	Compliance Test Suite
DDC	Display Data Channel
DJ	Deterministic Jitter
ESD	Electrostatic Discharge
FMC	FPGA Mezzanine Connector
FPLL	Fractional Phase Lock Loop
FR4	PCB dielectric material
FRL	Fixed Rate Link
PCA	Power over Cable Assembly
PCB	Printed Circuit Board
PJ	Periodic Jitter
QSF	Quartus Settings File
RJ	Random Jitter
Rogers	PCB dielectric material
SDG	System Design Guidelines
SJ	Sinusoidal Jitter
TI	Texas Instruments
TMDS	Transition Minimized Differential Signaling
TP1	Test Point 1
TTK	Transceiver Toolkit
TTM	Time to Market
Vpp	Peak-to-Peak Voltage
WCM	Worsecase Cable Model
Z	Impedance

2. Introduction

This document guides you on how to design Intel® Arria® 10 and Intel Stratix® 10 devices to meet HDMI 2.1 Compliance Test Specifications (CTS) requirements. You can utilize an Intel Arria 10 GX or an Intel Stratix 10 development kit and a specifically designed daughtercard to support signal conditioning as shown in the figure below.

Figure 1. An Intel Arria 10 GX Development Kit with Daughtercard



3. Prerequisites and Scope

Before you begin, Intel recommends that you do the following:

1. Understand all HDMI 2.1 CTS requirements per HDMI.Org and strive to meet both Protocol and Electrical Specifications.
2. Refer to all existing platform level resources such as Development Kit Guides, Platform Design Guides (PDG), and Application Notes (AN).

You can use an existing development kit together with this system design guide to enable a HDMI 2.1 capable system. If you require an accelerated Time to Market (TTM) product roadmap, you can use the daughtercard design recommendations and Intel development kit. If you choose to create a proprietary design, use this guide to help you develop a compliant design that saves time and cost.

The reference design has passed HDMI 2.1 CTS test suite, with electrical attributes characterized by Electrical Validation and settings optimized to development kit setup.

Protect your silicon from damage caused by Electrostatic Discharge (ESD) events in a typical usage model. Intel Arria 10 and Intel Stratix 10 devices that use redrivers or retimers do not require additional ESD clamp circuitry. Do assess the ESD requirements of your design.

While the recommendations in this guide are based on HDMI 2.1 daughtercard development iterations, they are also applicable to other board topologies. Therefore, in these subsequent pages, this document uses the PCB panel to describe the design in general.

4. System Design Guidelines Requirements

4.1. Enabling PCB panel design

The following guidelines and requirements target general PCB panels. You can use FR4 stack-up to reduce costs or Rogers for better signalling on larger panels. Evaluate your stack-up requirements based on the attributes in the table below.

Ensure that your cables meet HDMI 2.1 certification. HDMI.org provides a list of compliant connectors and cables along with their providers. For the purpose of this guide, Intel uses Belkin cables with HDMI IP running 12-gigabits per second (Gbps) Fixed Rate Link (FRL).

Table 2. Summary of daughtercard PCB general design guidelines

Item	Impedance (Z)/Length	Type/Stack-up	Comment
Trace	90-100 Ω Length matched	FR4, microstrip top/bottom layer	Keep stack-up targeting 90 Ω; to minimize reflection loss
Connectors & Cables	95 Ω	Surface mount	Use compliant connectors such Belkin HDMI 2.1 cables
Components	90 Ω	Surface mount	Reduce void by placement optimization
Power plane	NA Lowest Z possible	2 layers	Partial to full Ground reference; full reference whenever possible
Ground plane	Lowest plane Z	NA	Full reference for signals

HDMI 2.1 accommodates both Transition Minimized Differential Signaling (TMDS) and Fixed Rate Link (FRL) modes.

- TMDS supports legacy HDMI devices running on three data lanes and one clock lane.
- FRL runs on four data lanes.

On the receiver (RX), the TMDS clock path shares the FRL data lane.Therefore, on the PCB panel with Intel FPGA, you need a fanout buffer to split incoming RX signals to drive both paths to support both TMDS and FRL. At the schematic design level, one approach is to use an external fanout buffer. However, this additional fanout buffer increases system costs. Another approach is to use an integrated fanout buffer option with redriver at the RX side to recover signals at 19-decibel (dB) up to 12 Gbps.

HDMI 2.1 operates up to 12 Gbps with cable loss of up to 16dB. For cost optimization, use the redriver at the transmitter side.

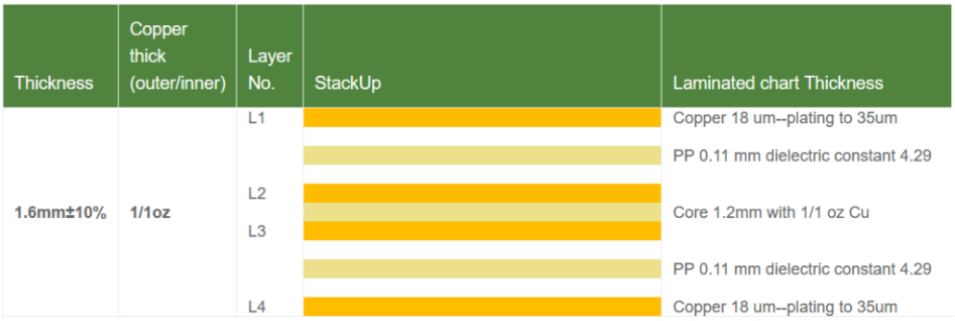
The table below shows a summary of the redrivers for Intel Arria 10 and Intel Stratix 10.

Table 3. Redriver loss compensation and attributes

Component (TI redrivers)	Insertion loss @12 Gbps	Z	Comment
DS125BR820	10dB	90 Ω	TX redriver
DS125MB203	18dB	90 Ω	RX redriver, integrated Fanout buffer

Intel recommends trace impedance (Z) target to be in range 90-100 Ω; do not exceed 100 Ω (not considering fabrication tolerance). This ensures best possible reach on both trace length and signal integrity

Figure 2. Daughtercard panel size



Note: The reference design uses FR4 material due to it is low cost.

The daughtercard panel size is small with high speed traces within 10 inches. If you target larger margin and desire for larger panel, you can opt for Meg6 material. Intel recommends a flex cable topology for signals up to 12 Gbps.

For design with 4 layer (SGPS) FR4 stackup, refer below parameters for microstrip/top layer:

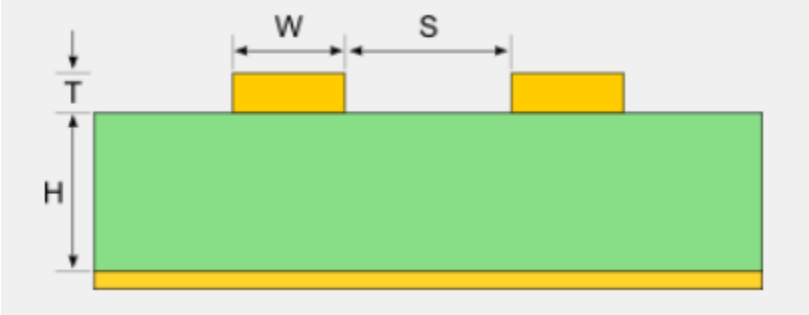
Table 4. FR4 Stack-up Target

Type FR4	Thick (T) um	Width (W) um	Height (H) um	Spacing (S) um	Dieletric Constant (Dk)
Zdiff=100 Ω	35	203.2	110	100	4.3

Note: Z target is 90 to 100 Ω

Figure 3 illustrates the parameters:

Figure 3. PCB fabrication Cross-section Attributes



4.2. PCB Best Practices

1. Connect power (VDD) and ground (GND) pins directly to corresponding power planes on the PCB without passing through any resistor.
2. Keep the thickness of your PCB dielectric layer to a minimum so that the VDD and GND planes create low inductance paths.
3. Mount one low-ESR 0.1 uF decoupling capacitor at each VDD pin. Intel recommends smaller capacitors such as the 0402 package, as the insertion loss is lower. Place the capacitor closest to the VDD pin.
4. Incorporate one capacitor with capacitance in the range of 4.7 uF to 10uF in the power supply decoupling. You can use an ultra-low ESR ceramic. Place the capacitor further away from the FPGA than the 0.1 uF VDD decoupling capacitors.
5. Use specific best practises when designing around Low Dropout Regulators (LDOs), MOSFET and clock (CLK) signals to minimize noise couplings. The purpose is to isolate noise and yield the best signal integrity.
6. Do not let signal lanes pass through voids. Use stitching vias around insufficient ground reference in congested spots.

In addition to the above, here are some tips on designing PCB layouts:

1. Route the high-speed TMDS traces on the top layer to avoid the use of vias (and the introduction of their inductances). This allows for clean interconnects from the HDMI connectors to the redriver inputs and outputs. It is important to match the electrical length of these high-speed traces to minimize both inter-pair and intra-pair skew (Refer to HDMI 2.1 CTS requirements for the measurement).
2. Place a solid ground plane next to the high-speed single layer to establish controlled impedance (targetted Z) for transmission link interconnects and provide a better low–inductance path for the return current flow.
3. Route slower control signals on the bottom layer to allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias and therefore, higher insertion loss. Separate the signals with low voltage swing and single ended types from high speed differential pairs with larger (3x) spacing to minimize attenuation.
4. Place a power plane next to the ground plane to create an additional high-frequency bypass capacitance.
5. If you require an additional supply voltage plane or signal layer, add a second power/ground plane system to the stack to maintain symmetry. This action mechanically stabilises the stack and prevents it from warping. You can significantly increase the high-frequency bypass capacitance by placing the power and ground plane of each power system closer together.

HDMI 2.1 supports the power over cable assembly (PCA cables). Evaluate the voltage drop on the 5 V rail at both TX and RX. In general, the widening traces for 5 V rail can tolerate higher current load since nominal voltage remains at 5 V.

Evaluate the HDMI connector footprint carefully to ensure you use compliant connectors. Strap the Ground pins to the nearest ground plane and do not leave the pins dangling. A good ground reference is critical to have the desired impedance control.

Note: If there is significant change in Loss Profile, Intel recommends that you simulate on Advanced Link Analyzer (ALA) to optimize TX/RX settings based on actual system profiles.

4.3. System Link Budgeting Recommendations

Platform link budgeting helps improve your experience by allocating sufficient loss on main board (with Intel Arria 10 or Intel Stratix 10 FPGA), PCB panel or daughtercard, and HDMI connectors (including cables).

Apply a generic redriver primarily to meet Insertion Loss at 12 Gbps. In a typical use case scenario, there is an estimated cable loss of 19 dB with two connectors.

Table 5. Link Budgeting Distribution

Item	Link Component	Insertion Loss @12 Gbps	Comment
1	FPGA → FMC → TX Redriver	5 dB	TX FFE recommended
2	Redriver → HDMI connector	10 dB (+18 dB)	Minimize lowest loss Budgets for cable loss
3	HDMI cable → Connector → RX Redriver → FPGA RX	19 dB+10 dB	Better Redriver/retimer

Note: Refer to Table 7 on page 11 for jitter tolerance data.

4.3.1. FPGA TX Settings

Intel recommends the settings in Table 6 for your FPGA TX. Both FPLL and ATXPLL apply. In general, ATX PLL has a slightly better margin than FPLL, although this may not be a dominant factor for Intel Arria 10 and Intel Stratix 10.

For a complete list of settings, refer to Transceiver User Guide.

Table 6. FPGA TX Recommended Settings

Item	Value
Vod output swing ctrl	30
Pre emp sign 1st post tap	Fir post 1t neg
Pre emp sign 2nd post tap	Fir post 2t neg
Pre emp switching ctrl 1st post tap	5
Pre emp switching ctrl 2nd post tap	0
Pre emp sign pre tap 1t	Fir pre 1t post
Pre emp sign pre tap 2t	Fir pre 2t neg
Pre emp switching ctrl pre tap 1t	0
Pre emp switching ctrl pre tap 2t	0
Slew rate ctrl	Slew r5

Set TX slew rate to r5 to ensure all four TMDS data channels (three data channels and one clock) are within the 2 UI bonding requirements of Test Point 1 (TP1) and meet inter-lane skew requirements.

Your TX redriver settings are determined by your PCB design profile. Intel recommends a minimum VOD setting of 1.0 on the TX redriver.

Related Information

Knowledge Database

4.3.2. FPGA RX Settings

You must use a redriver on the PCB panel to ensure compliance to RX CTS and HDMI 2.1 cable loss. Intel products do not support non-compliant cables. The equalization is dependent on overall system reach design; in a typical scenario, 16 dB is sufficient, while longer traces on larger PCB panels require higher equalization.

You can use flex cables instead of a large PCB panel for a better cost-to-performance ratio. Use link training methodology to evaluate if such cables match your setup. Validation setup uses generic jitter tolerance methodology to meet HDMI 2.1 CTS requirements.

Below is a summary of targeted loss calibration:

Table 7. Targeted loss calibration

Insertion Loss : 20.11 dB				
	Spec		Calibrated	
Amplitude	800-1200 mV	-		
RJ	0.2 UI	1.31 ps	1.224 ps	0.12 UI
DJ	0.35 UI	29.2 ps	-	-
BUJ	0.15 UI	12.5 ps	12 ps	0.12 UI
SJ/PJ	0.1 UI	8.33 ps	9.33 ps	0.1 UI
Eye Height	100 mV	-	97.1 mV	
Eye Weight	29.17 ps	-	31.5 ps	

The jitter (BUJ) interpretation varies. Focus on the entire system level with all components account for 1 UI budget. HDMI.org provides WCM cable that shows the cable loss parameter. The stressed signal feeds into RX to establish jitter tolerance. The following table lists the recommended settings:

Table 8. FPGA RX Recommended Settings

Component	Intel Arria 10 FPGA	Redriver (TI DS125MB203)	
Adaptation Mode	Manual CTLE, TX FFE	EQ	DeEmp VOD
VGA Gain	2	-	-
DC Gain	1	-	-
AC Gain	3	Level4	Level 0-2 (1) (2)
Vpp Amplitude	-	-	0.8

Do note that a 2 UI TX length at 6 Gbps at Test Point 1 is a mandate by HDMI 2.1 CTS.

All settings listed in this document are available in Intel Quartus® Prime. You can update the settings to reflect the need of each design requirements as well as loss factor.

To mitigate variability in customer loss profiles:

1. Isolate and confirm that the root cause is the transceiver link.
2. Apply link tuning methodology.
3. Refer TTK (transceiver toolkit):

(1) Intel recommends that you start with Level 0 to evaluate link stability. This setting depends on incoming TX Vpp including link setup. The larger the Vpp, the higher the level of deemphasis setting possible.

(2) Refer to Performance and Cost Considerations on page 14.

- Evaluate link stability and robustness by sweeping transceiver analog settings (for loss profiles beyond nominal cases).
- Find the optimal RX analog settings with TTK.
- Apply static values in the QSF file.

Related Information

- Analog Parameter Settings, Intel® Arria® 10 Transceiver PHY User Guide
  More informatino about the analog parameter settings.
- L- and H-Tile Transceiver PHY User Guide
  More information about Intel Stratix 10 transceiver PHY.

4.3.2.1. Intel Stratix 10-specific RX Feature

Intel Stratix 10 supports RX Auto Adaptation capability. This mode does not require you to set RX values manually; rather, Intel Stratix 10 provides you with the optimized settings in real time. To enable this mode, compile your design with Adaptation mode set to Auto. Refer to the Intel Stratix 10 Transceiver User Guide for more details.

This reference design uses a TI Redriver with settings similar to those described in *Table: FPGA RX Recommended Settings* and 8 dB compensation to meet CTS cable loss requirements.

The cables you use must meet HDMI 2.1 specifications. Backplanes are not part of CTS certification. Therefore, you need to ensure your design's overall system link loss profiles are within CTS targets.

The table below outlines the Worsecase Cable Model used in characterization to modulate with the SJ component:

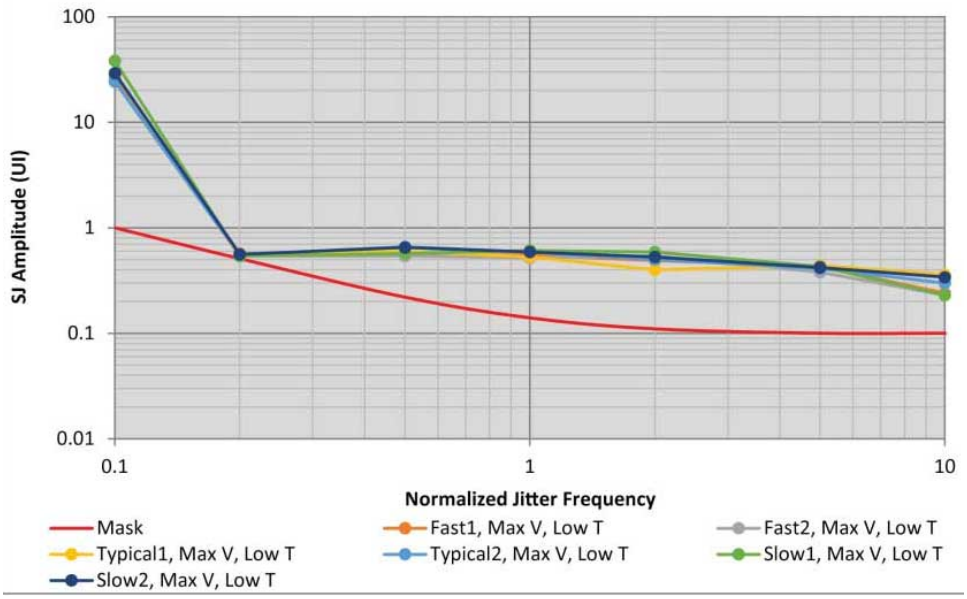
Table 9. Intel Stratix 10 Worsecase Cable Model Target Compensation

Protocol or Sub-protocol	Data Rate (Mbps)	V_{CCR/T_GXB} Voltage Level (V)	Test Channel Insertion Loss (dB)	Redriver Settings		
				EQ Gain	EQ Output VOD	EQ Output DE
HDMI_12000_FRL	12,000	1.03	20.183[2]	8.7 dB at 5 GHz	0.8 Vpp	0 dB

Note: EQ, VOD, and DE denote equalizer, output differential voltage, and de-emphasis, respectively.

As a result, you need to set 8 dB equalization at 12 Gbps to meet HDMI 2.1 CTS requirements. Jitter tolerance on HDMI 2.1 Gbps is met.

Figure 4. Jitter Tolerance for HDMI_12000_FRL (1.03-V_{CCR/T_GXB} Voltage Level)



Note: Measurements at lower jitter frequencies are constrained by the measurement setup. Measurements are obtained without a clock recovery unit to track lower frequency jitter components.

5. HDMI 2.1 Compliance Test Specification

There are two requirements in HDMI 2.1 certification, namely Protocol IP CTS and Electrical CTS.

5.1. Protocol IP Compliance Test Specification

You can achieve protocol compliance by utilizing industry-developed testers.

In this example, a test on the Intel Arria 10 GX development kit with HDMI 2.1 daughtercard using a Lecroy Quantum Data (QD) Protocol Analyzer yields the following overall passes on Error Detection Counters (CED) running on 12 Gbps.

Figure 5. Protocol IP Compliance Test Specification Result

Report Index / Summary					
Test HFR2-17	Pass	Test HFR2-18	Pass	Test HFR2-19	Pass
Test HFR2-20	Pass	Test HFR2-21	Pass	Test HFR2-22	Pass
Test HFR2-48	Pass	Test HFR2-49	Pass	Test HFR2-50	Pass
Test HFR2-51	Pass	Test HFR2-52	Pass	CDF	
Equipment Info					

Note: Refer only to the test result: Pass.

5.2. Electrical Compliance Test Specification

You can achieve electrical compliance by using all test suites from industry vendors.

In this example, the Intel Arria 10 GX development kit undergoes rigorous testing under the HDMI 2.1 CTS test suite. The tests on two types of PLL, ATX PLL and FPLL running on FRL 12 Gbps and TMDS modes yield overall passes on all electrical attributes.

5.3. Performance and Cost Considerations

1. Intel recommends that you enable TX FFE to ensure better interoperability among various HDMI 2.1 devices. However, RX jitter tolerance does not account for FFE usage.
2. You can increase the performance of RX equalization and reduce FPGA dependency by utilizing redrivers or retimers that can compensate for higher loss profiles.
3. Although using external redrivers or retimers can help your design meet CTS compliance, you must ensure that the settings are able to meet the proprietary loss profile setup.

Note: The electrical validation optimization in this document does not cover non-Intel devices. If your profile setup is significantly different from what is shown here, use Link Tuning method to verify link integrity.

4. For PCB designs that do not require Intel Quartus Prime compilation, you can refer to Channel Placement Tools (CPTs) specific to Intel Arria 10 or Intel Stratix 10, which allow you to allocate link topology by designated pinouts.

6. Future System Level Optimization

6.1. Availability of Redrivers or Retimers

Market demand dictates the availability of redrivers and retimers to support electrical reach and compliance. You can choose any available redriver or retimer depending on electrical characteristic of Source and Sink.

Intel recommends that you apply TX FFE and use compliant cables in your setup. It can be advantageous to use better RX equalization designs to recover signal on a PCB panel before feeding them into your FPGA. You can use redrivers or retimers to cater for your link budgeting needs.

6.2. The Intel Agilex® Platform

The card design for the Intel Arria 10 and Intel Stratix 10 families works on a typical level shifters from 1.8 V up to 3.3 V. However, to support future platform families and to extend the time frame for portability, Intel recommends a daughtercard level shifter of 1.0 V for general purpose (GPIO).

Intel recommends a card design that includes DDC lines with proper pullup termination; the signals require mitigating voltage drop along the compliant cables.

7. Document Revision History for AN 952: Intel Arria 10 and Intel Stratix 10 HDMI 2.1 System Design Guidelines

Document Version	Intel Quartus Prime Version	Changes
2022.06.21	22.2	• Updated document title to *AN 952: Intel Arria 10 and Intel Stratix 10 HDMI 2.1 System Design Guidelines*. • Added Intel Stratix 10 throughout this document where applicable. • Updated the *FPGA RX Settings* section to include a section on Intel Stratix 10-specific RX feature.
2021.06.29	21.2	Initial release.