The following is our HW configuration.

[CPU] - (PCIe) - 【XIO2001】 - (pci) - [PCI device: FPGA…etc]



[Problem]

1. When FPGA execute the initial process, it will data transfer to local bus from PCI bus. Because Local bus is 8 bit, which requires 32-bit PCI data is divided into four times writing. When finish the data write in local bus, FPGA will assert the TRDY to low level, inform to the next PCI progress. The FPGA is a low speed PCI device which is a single R/W, no DMA function.
2. At present, the problem encountered by customers is that when multiple consecutive write operations, an odd number of write operations occur successfully, and **even number of write** operations will be **fail**.

From the PCI bus timing waveform, **customer found the FRAME did not wait TRDY assert directly start the next write operation when even number of write times operation.**

Customer initialization operation is writing operation.

Please refer below figure which customer initialization flow chart.



From the PCI bus timing waveform as below:



The first write operation is successful (for offset 0x0800 write 0x0004), the FRAME

will wait TRDY assert then start write command. But the second write operation will

be fail as above description that **the FRAME did not wait TRDY assert directly start**

**the next write operation when even number of write times operation. It will cause**

**the initialization operation fail.**

1. We had tuned the PCI latency timing, but it still fails.