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| Title | | | |
| Block Diagram | | | |
| Size | Document Number | Rev | |
| C | PIS-5600-B | A1 | |
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| Title | | |
| PWR. Map | | |
| Size | Document Number | Rev |
| C | PIS-5600-B | A1 |
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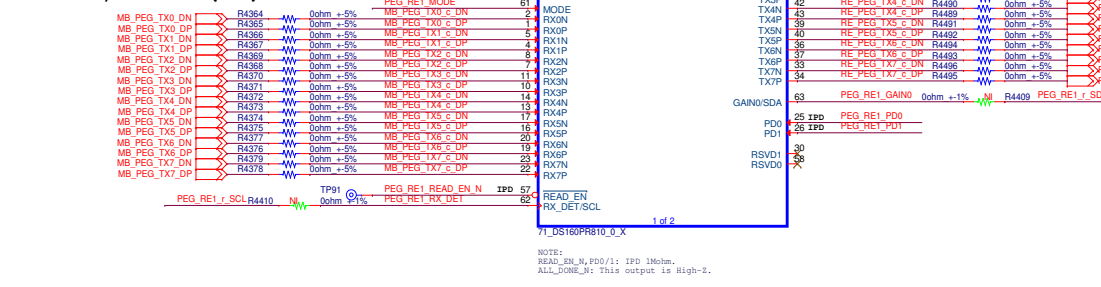
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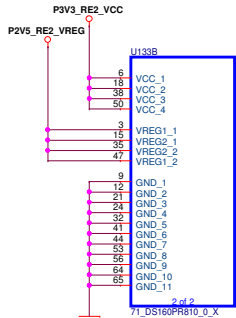
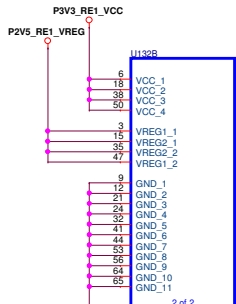
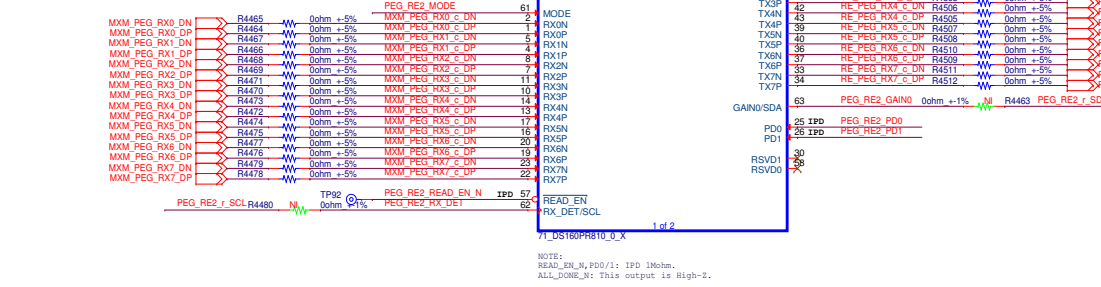
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PEG TX FROM J1, J2 CN. (MB)



PEG RX FROM MXM



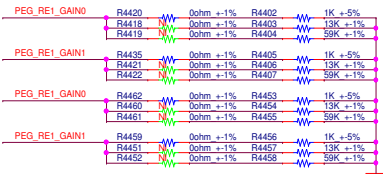
| 4-Level Control Pin Settings | |
|------------------------------|--------------------|
| LEVEL | SETTINGS |
| L0 | Tie 1kohm to GND. |
| L1 | Tie 13kohm to GND. |
| L2 | Tie 50kohm to GND. |
| L3 | F (Float) |

| Mode | Pin Level | HDMI Mode | Source Termination |
|------|-----------|-------------|---|
| L0 | | Slave Mode | device control configuration is done solely by atep pins. |
| L1 | | Master Mode | device control configuration is read from external EEPROM. |
| L2 | | Slave Mode | device control configuration is done by an external controller. |
| L3 | | RESERVED | TI internal test mode. |



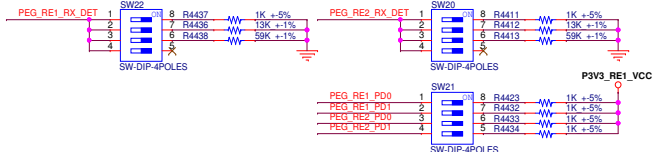
GAIN Settings

| GAIN0/L Pin Level | FLAT-GAIN | EQ-MAX (dB) | DCGAIN (VAR) | EQGAIN (VAR) |
|-------------------|-----------|-------------|--------------|--------------|
| L0 | -4.2db | - | - | - |
| L1 | -1.8db | - | - | - |
| L2 | 0.25db | - | -2.3-1.7db | -3.3-3.7db |
| L3 | 2db | 18db | - | - |

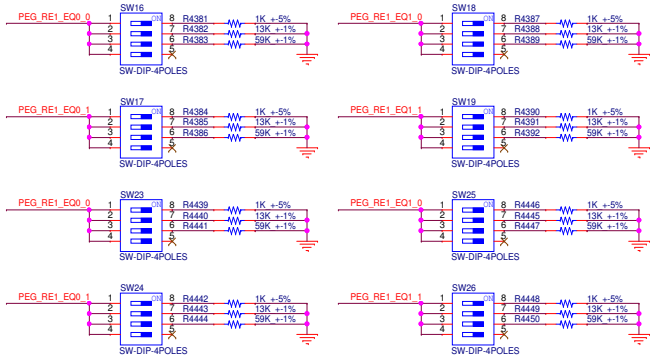


Receiver Detect State Machine Settings

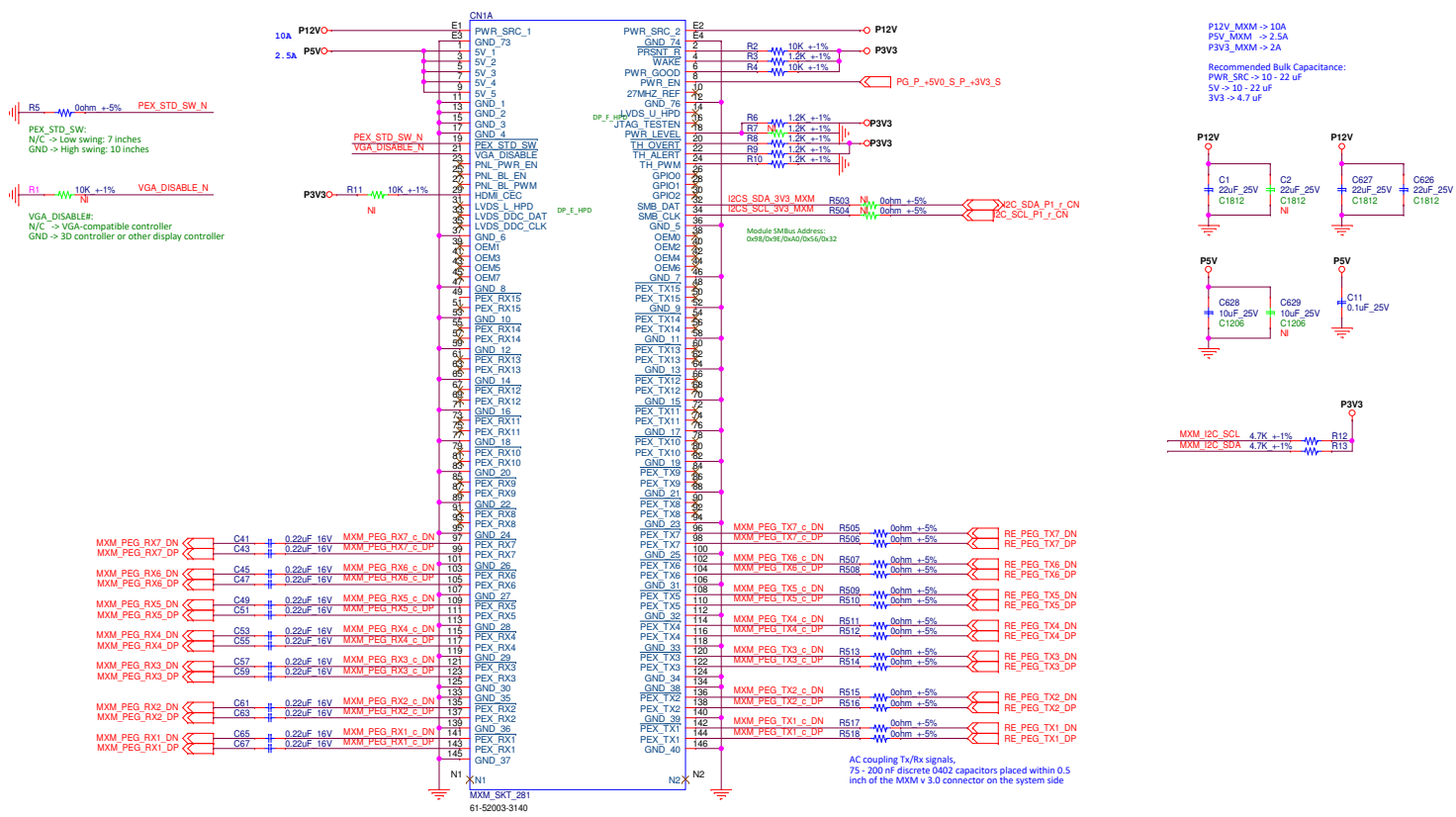
| PDO | PD1 | RX DET | Channels 0-3 RX Common-mode Impedance | Channels 4-7 RX Common-mode Impedance | COMMENTS |
|-----|-----|--------|---------------------------------------|---------------------------------------|--|
| L | L | L0 | Always 50Ω | Always 50Ω | PEI Express RX detection state machine is disabled. Recommended for non PCIe interface use cases where the DS160PR810 is used as buffer with equalization. |
| L | L | L3 | Pre Detect: Hi-Z Post Detect: 50 Ω | Pre Detect: Hi-Z Post Detect: 50 Ω | RX pull up every ~150ns until valid termination is detected. RX CM impedance held at Hi-Z until detection Reset by asserting PDO1 high for 200ns then low. |
| H | L | X | Hi-Z | Pre Detect: Hi-Z Post Detect: 50 Ω | Reset Channels 0-3 signal path and set their RX impedance to Hi-Z |
| L | H | X | Hi-Z | Pre Detect: Hi-Z Post Detect: 50 Ω | Reset Channels 4-7 signal path and set their RX impedance to Hi-Z |



Equalization Control Settings

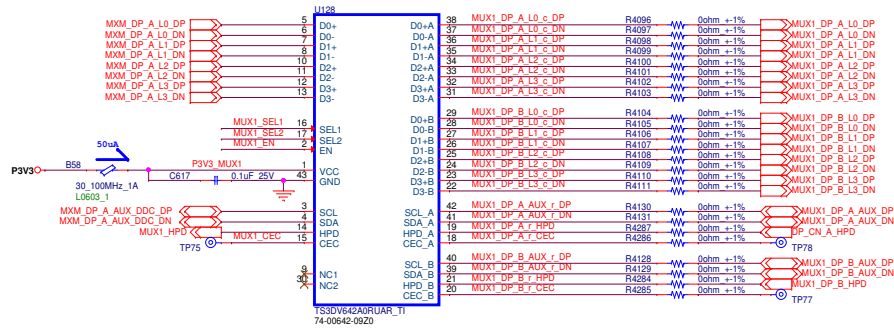


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DP++ To DP/HDMI OF MUX 1

FROM MXM PORT A

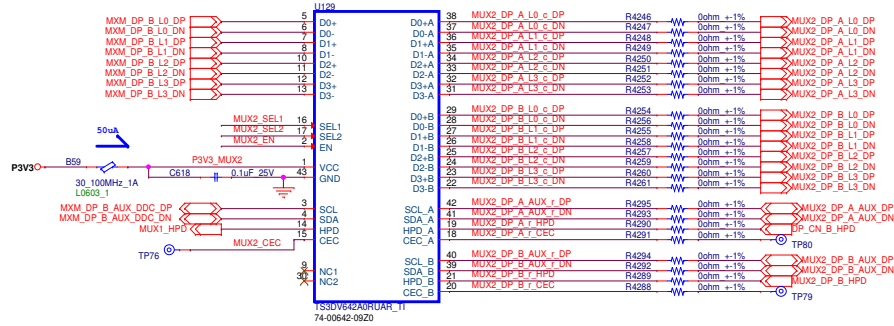


TO Front DP CN.A

TO Rear RTM DP Port

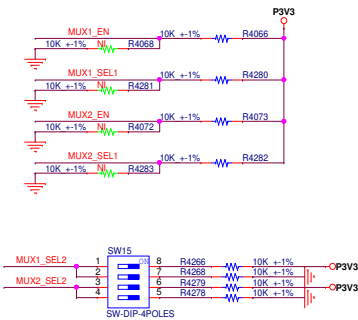
DP++ To DP/HDMI OF MUX 2

FROM MXM PORT B



TO Front DP CN.B

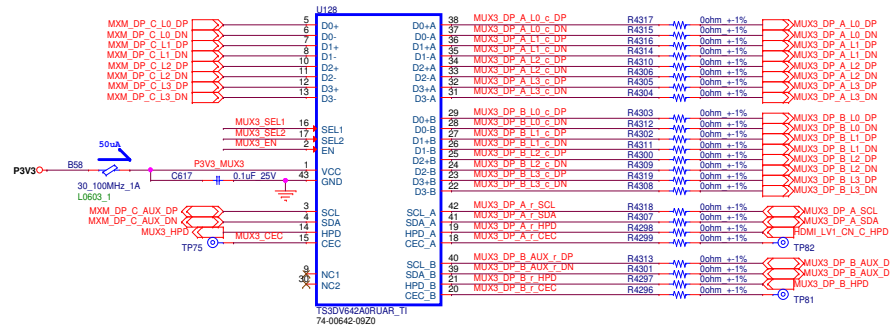
TO Rear RTM DP Port



| EN | SEL1 | SEL2 | FUNCTION |
|----|------|------|---|
| L | X | X | Switch disabled. All channels are Hi-Z. |
| H | L | L | Channel D0+/D0- to D0+/D0-A is ON. All the other channels (D1+/D1-, D2+/D2-, D3+/D3-, SCL, SDA, HPD, CEC) are Hi-Z. |
| H | L | H | Channel D0+/D0- to D0+/D0-B is ON. All the other channels (D1+/D1-, D2+/D2-, D3+/D3-, SCL, SDA, HPD, CEC) are Hi-Z. |
| H | H | L | All A channels are enabled. All B channels are Hi-Z. |
| H | H | H | All B channels are enabled. All A channels are Hi-Z. |

DP++ To DP/HDMI OF MUX 3

FROM MXM PORT C

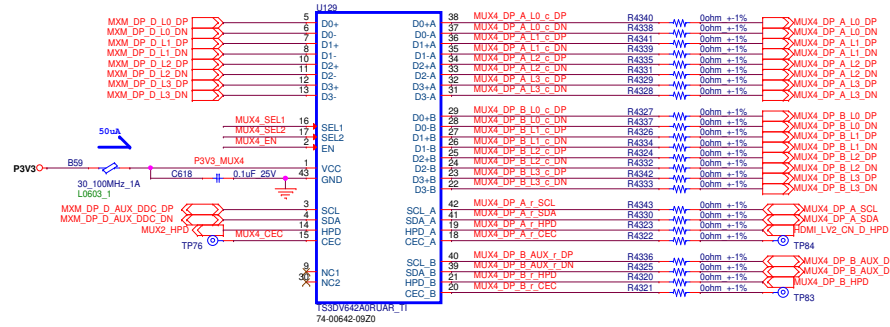


TO Front HDMI CN.C
(Path HDMI Level-Shifter1)

TO Rear RTM DP PORT

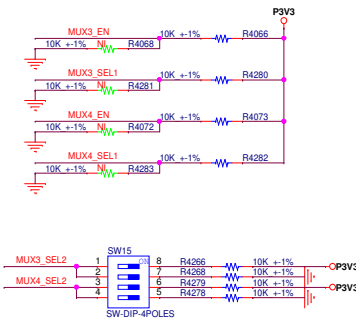
DP++ To DP/HDMI OF MUX 4

FROM MXM PORT D

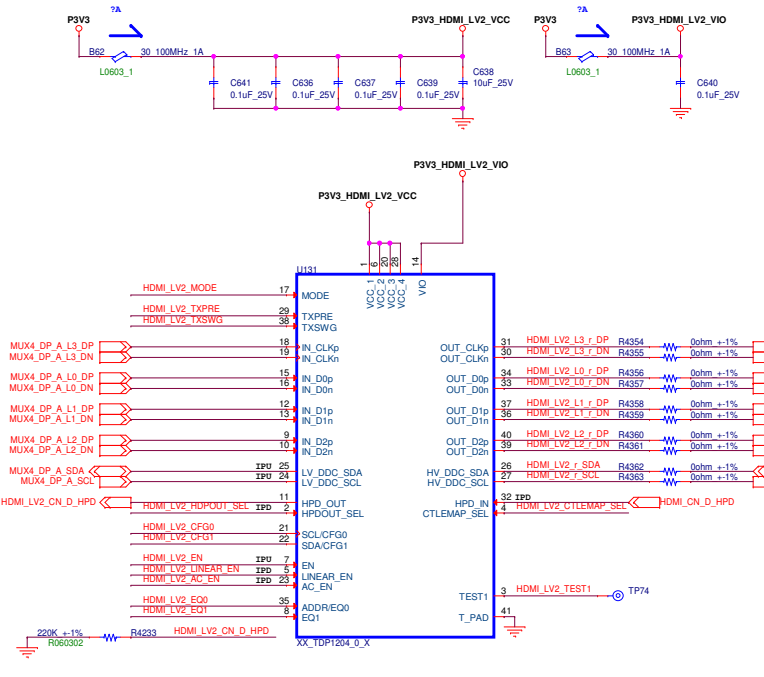
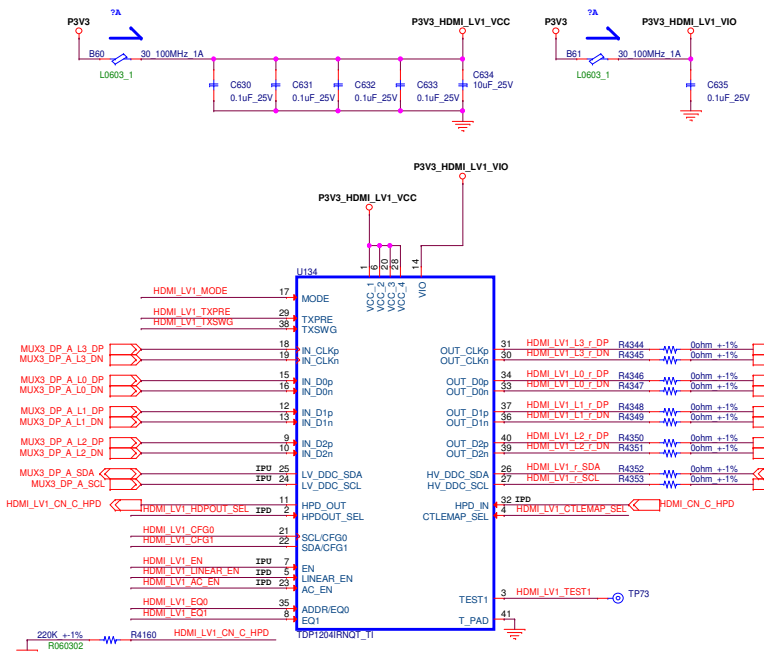


TO Front HDMI CN.D
(Path HDMI Level-Shifter2)

TO Rear RTM DP PORT

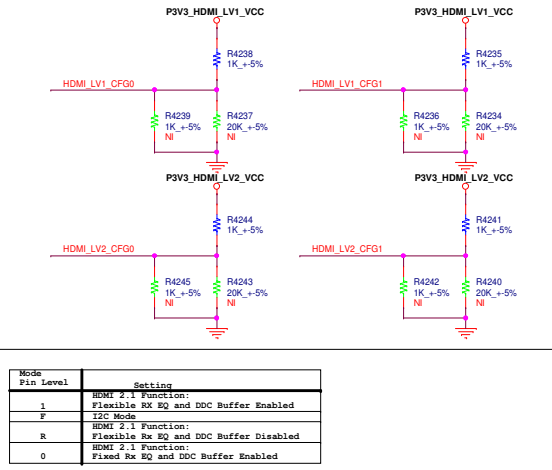


| EN | SEL1 | SEL2 | FUNCTION |
|----|------|------|--|
| L | X | X | Switch disabled. All channels are Hi-Z. |
| H | L | L | Channel D0+/D0- to D0+/D0- is ON. All the other channels (D1+/D1-, D2+/D2-, D3+/D3-, SCL, SDA, HPD, CEC) are Hi-Z. |
| H | L | H | Channel D0+/D0- to D0+/D0- is ON. All the other channels (D1+/D1-, D2+/D2-, D3+/D3-, SCL, SDA, HPD, CEC) are Hi-Z. |
| H | H | L | All A channels are enabled. All B channels are Hi-Z. |
| H | H | H | All B channels are enabled. All A channels are Hi-Z. |

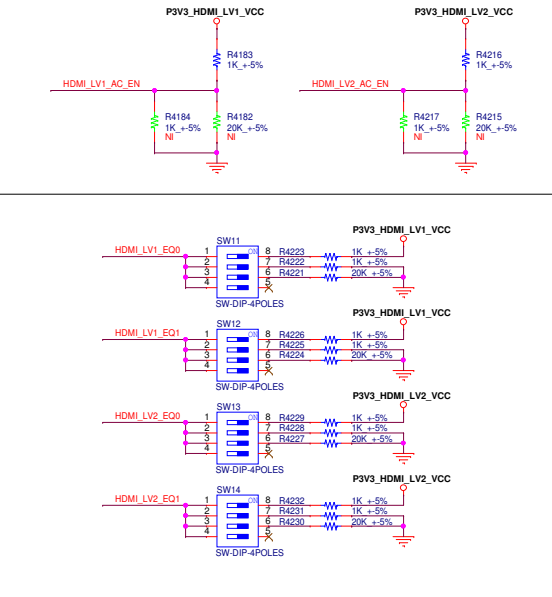


| SCL/CFG0 Pin Level | AC_EN | Function |
|--------------------|-------|--|
| 0 | 0 | HDMI 1.4 termination is open if HDMI clock frequency <= FHDmi14_open |
| 0 | 0 | HDMI 1.4 termination is open if HDMI clock frequency >= FHDmi14_open |
| 1 | 0 | HDMI 1.4 termination is ~300ohm |
| 0 | 1 | Normal HDMI Function determined by MODE pin. |
| 0 | 1 | DisplayPort mode, DDC emp disabled. |
| 1 | 1 | All four lanes enabled when HPD_LV is high. 12 Gbps CTELE used. |

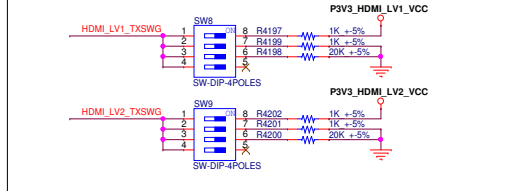
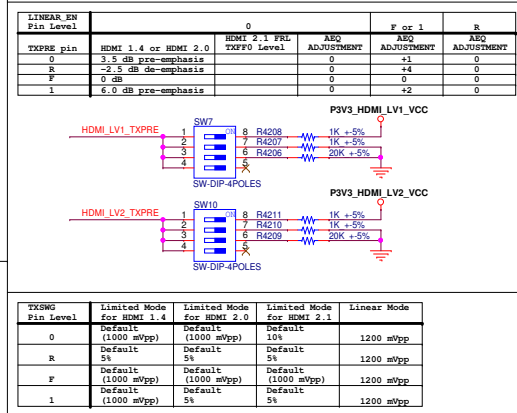
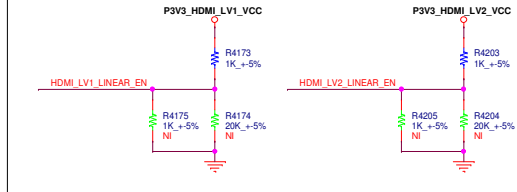
| SDA/CFG1 Pin Level | Function |
|--------------------|----------------------|
| 0 | Normal Lane ordering |
| 1 | Lane Swap enabled |



| AC_EN Pin Level | HDMI Mode | Source Termination |
|-----------------|-----------|---|
| 0 | HDMI 1.4 | None or parallel -> 300-Ω across P and N depending on state of SCL/CFG0 pin |
| 0 | HDMI 2.0 | Parallel -> 100-Ω across P and N |
| 1 | HDMI 1.4 | -> 150-Ω to supply (VCC) on both P and N |
| 1 | HDMI 2.0 | -> 50-Ω to supply (VCC) on both P and N |

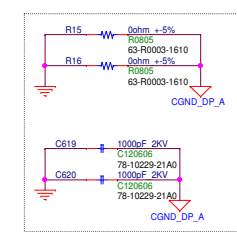
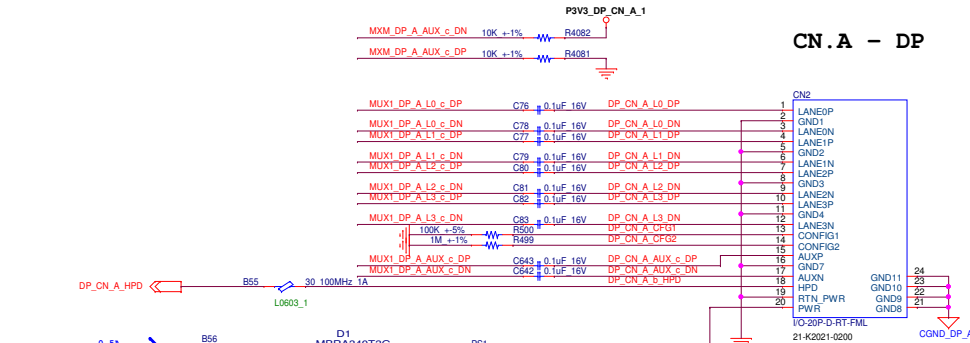
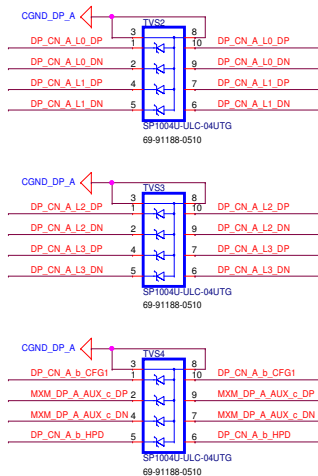
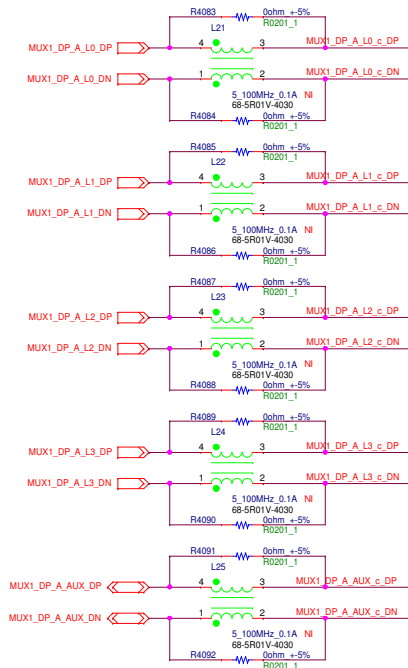


| LINEAR_EN Pin Level | HDMI 1.4, 2.0 or IP | HDMI 2.1 FRL |
|---------------------|-----------------------------------|-----------------------------------|
| 1 | Limited Enabled | Linear Enabled |
| F | Linear Enabled | Linear Enabled |
| R | For DP and HDMI sink application. | For DP and HDMI sink application. |
| R | Reserved | Reserved |
| 0 | Linear Enabled | Linear Enabled |
| 0 | For HDMI source application. | For HDMI source application. |

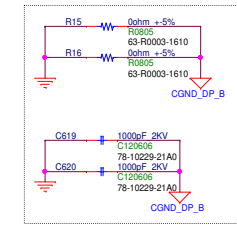
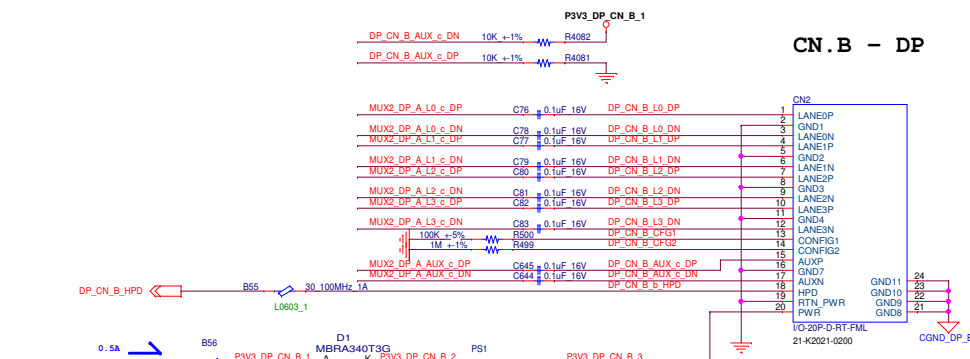
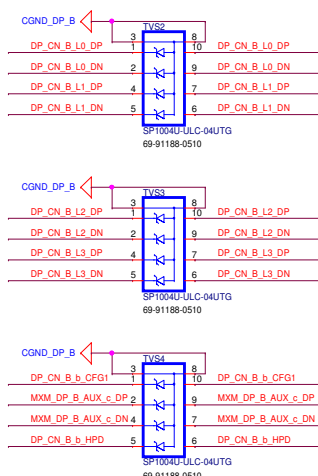
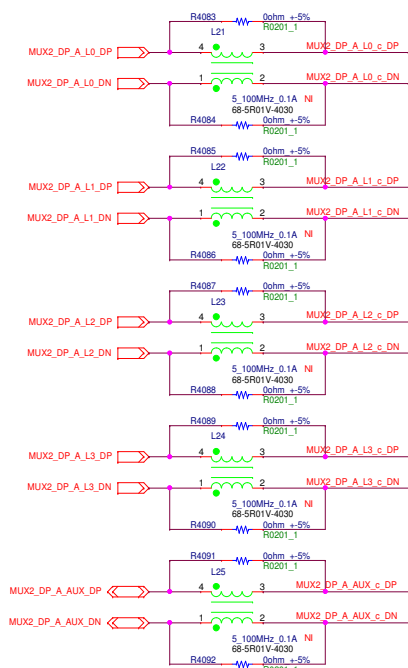


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|-------|---------------------------|--------------------------|----------------------------|
| Title | | HDMI Level Shifter 1 & 2 | |
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CN.A - DP



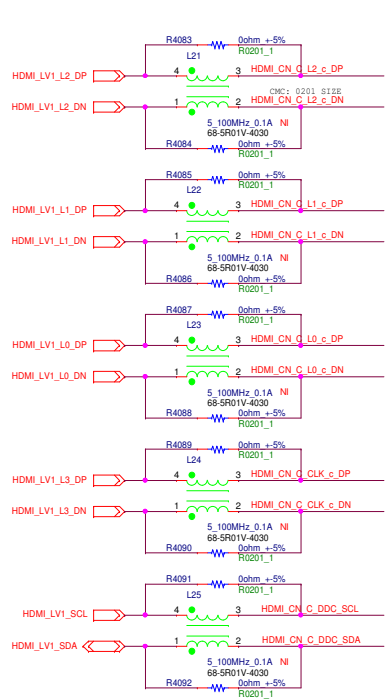
CN.B - DP

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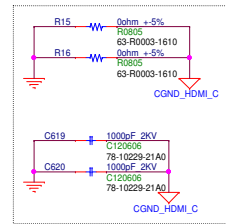
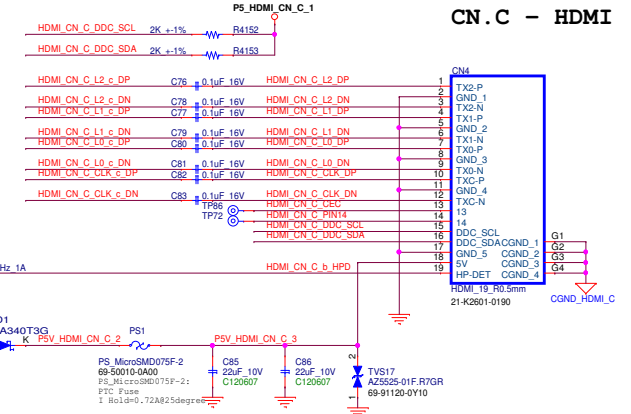
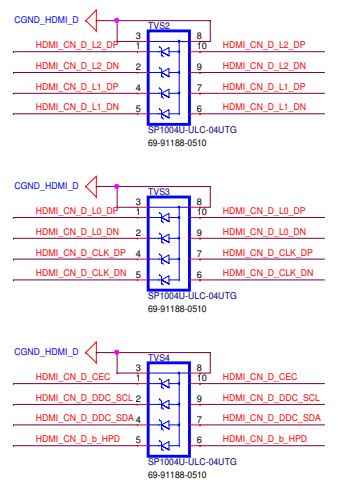
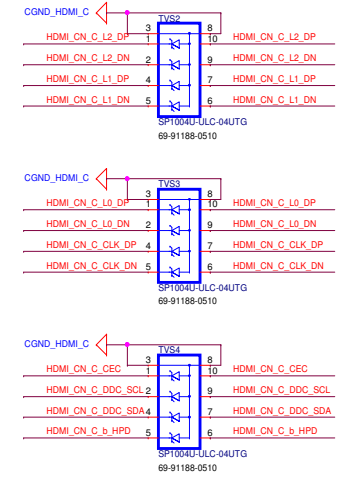
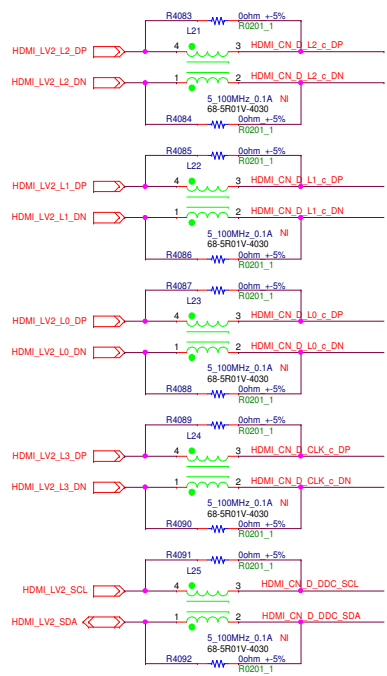
DP_CONN. A & B

Keyight N4 Carrier Board

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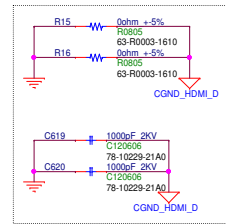
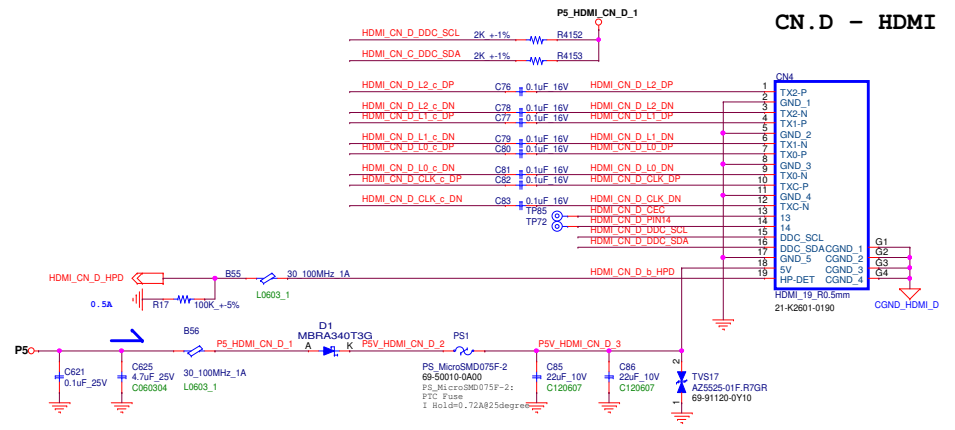


CNC: 0201 SIZE



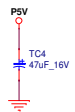
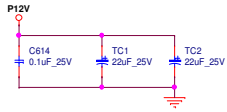
CN.C - HDMI

CN.D - HDMI

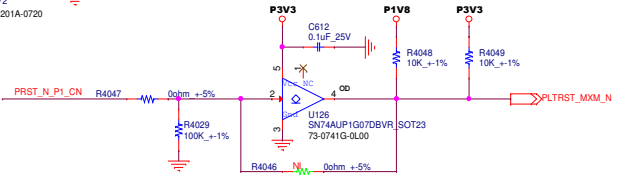
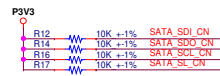
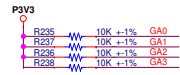
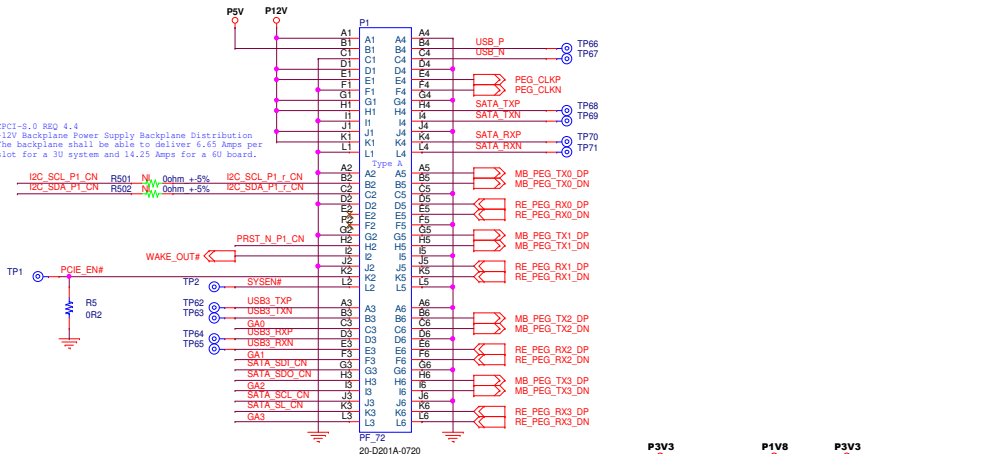


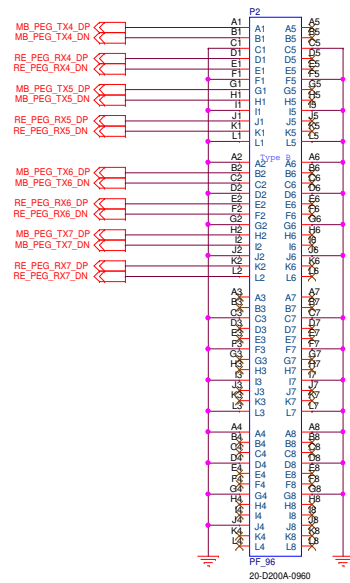
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| Title | | HDMI_CN_C & D | |
| Size | Document Number | KeySight N4 Carrier Board | |
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cPCI-5.0 REQ 4.4
 +12V Backplane Power Supply Backplane Distribution
 The backplane shall be able to deliver 6.55 Amps per slot for a 3U system and 14.25 Amps for a 6U Board.





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| cPCI_P5 | | | |
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| PSV | | |
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| Size | Document Number | Rev | |
| C | cPCI-A3TP | A1 | |
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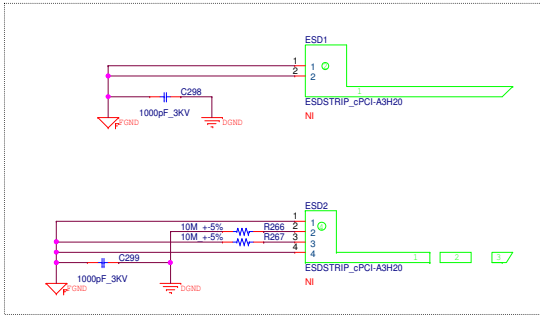
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FOR EMC



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| Title SCREW HOLE | | |
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A2 Change List

| <i>Item No.</i> | <i>Page</i> | <i>Bug No.</i> | <i>Bug / Change Descriptoin</i> | <i>SCH design change action</i> |
|-----------------|-------------|----------------|---------------------------------|---------------------------------|
| D001 | 63 | | | |
| D002 | 63 | | | |
| D003 | 67 | | | |
| | | | | |
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| Title Change List | | | |
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