DP83867E

A101-2: Change PHY from DP83867(RGMII) to DP83867E(SGMII)

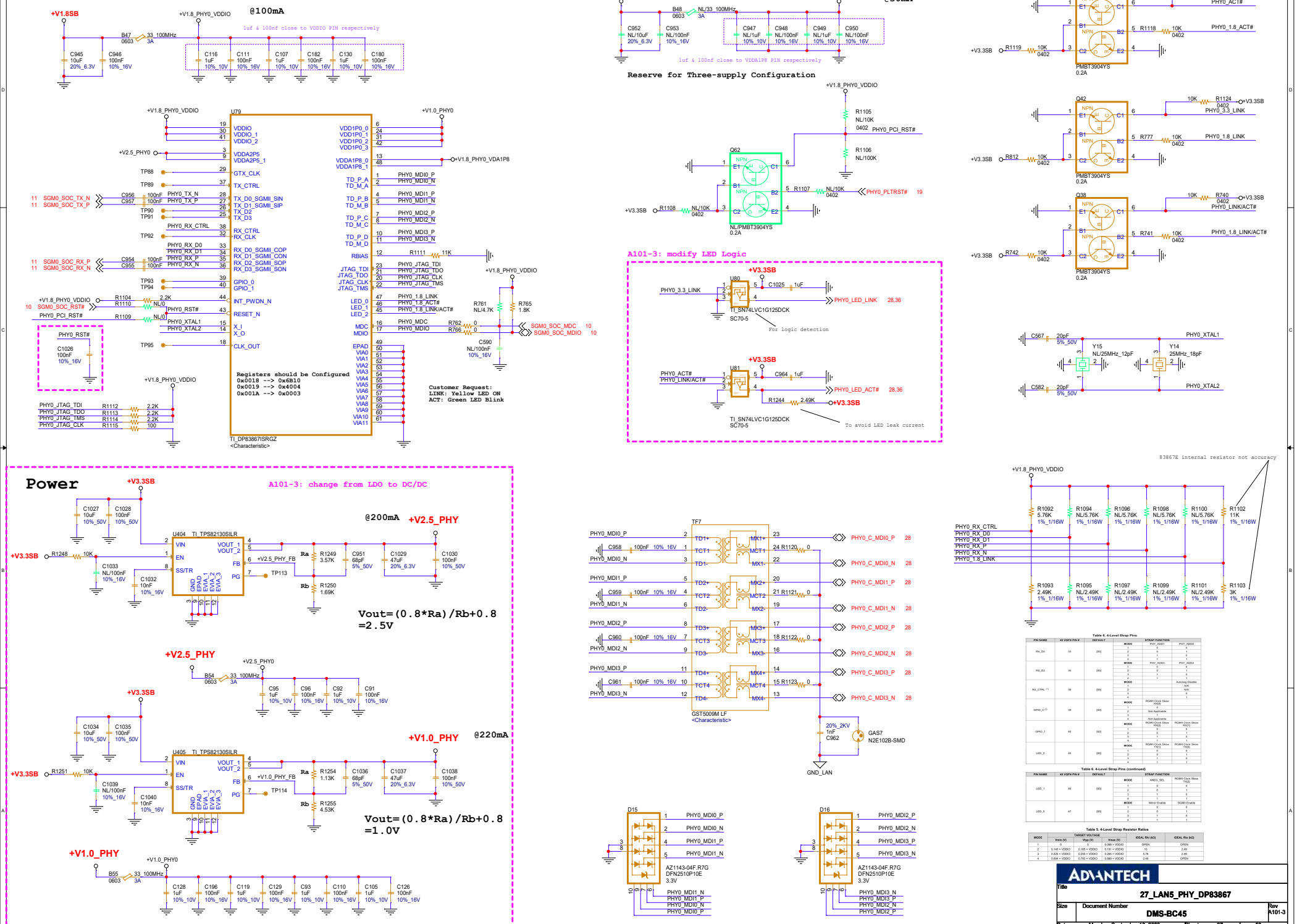

Table 6. 4-Level Strap Pins

PIN NAME	48 VQFN PIN #	DEFAULT	STRAP FUNCTION		
			MODE	PHY_ADD1	PHY_ADD0
RX_D0	33	[00]	1	0	0
			2	0	1
			3	1	0
			4	1	1
			MODE	PHY_ADD3	PHY_ADD2
RX_D2	36	[00]	1	0	0
			2	0	1
			3	1	0
			4	1	1
			MODE		Autoneg Disable
RX_CTRL (1)	38	[00]	1		N/A
			2		N/A
			3		0
			4		1
			MODE	RGMII Clock Skew RX[0]	
GPIO_0 (1)	39	[00]	1	0	
			2	Not Applicable	
			3	1	
			4	Not Applicable	
			MODE	RGMII Clock Skew RX[1]	RGMII Clock Skew TX[0]
GPIO_1	40	[00]	1	0	0
			2	0	1
			3	1	0
			4		
			MODE	RGMII Clock Skew TX[1]	RGMII Clock Skew TX[2]
LED_2	46	[00]	1	0	0
			2	0	1
			3	1	0
			4	1	1

Table 6. 4-Level Strap Pins (continued)

PIN NAME	48 VQFN PIN #	DEFAULT	STRAP FUNCTION		
			MODE	AMCC_SEL	RGMII Clock Skew TX[3]
LED_1	48	[00]	1	0	0
			2	0	1
			3	1	0
			4	1	1
			MODE	Mirror Enable	SGMII Enable
LED_0	47	[00]	1	0	0
			2	0	1
			3	1	0
			4	1	1

Table 5. 4-Level Strap Resistor Ratios

MODE	TARGET VOLTAGE			IDEAL Rh (kΩ)	IDEAL Rlo (kΩ)
	Vmin (V)	Vtyp (V)	Vmax (V)		
1	0	0	0.068 × VDDIO	OPEN	OPEN
2	0.140 × VDDIO	0.165 × VDDIO	0.191 × VDDIO	10	2.49
3	0.229 × VDDIO	0.255 × VDDIO	0.284 × VDDIO	5.76	2.49
4	0.654 × VDDIO	0.703 × VDDIO	0.883 × VDDIO	2.49	OPEN

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