Schematic Review Form

DS100DF410 Review for Feras

Pin #	Name	Info	Violations	*Description*
1, 2, 4, 5, 8, 9, 11, 12	RXPn, RXNn			Inverting and non-inverting CML-compatible differential inputs to the equalizer. Nominal differential input impedance = 100Ω. Must be AC coupled.
36, 35, 33, 32, 29, 28, 26, 25	TXPn, TXNn			Inverting and non-inverting CML-compatible differential outputs from the driver. Nominal differential output impedance = 100Ω. Must be AC coupled.
47, 48, 38, 37, 23, 24, 14, 13	LPF_CP_n, LPF_REF_n			Loop filter connection. Place a 22 nF ± 10% Capacitor between

				LPF_CP_0 and LPF_REF_n
19	REFCLK_IN		I checked FNETHE025 and it looks like this is a 3.3V oscillator. You should confirm if your oscillator is 2.5V and choose a different oscillator if necessary.	Input is 2.5 V, 25 MHz ± 100 ppm reference clock from external oscillator. No stringent phase noise requirement
42	REFCLK_OUT	If you wish to only use 1 oscillator, you can connect REFCLK_OUT from 1 retimer to REFCLK_IN of the other retimer. There are no issues using 2 oscillators if you prefer this configuration.		Output is 2.5 V, buffered replica of reference clock input for connecting multiple DS1xxDF410s on a board
45, 40, 21, 16	LOCK_n			Output is 2.5 V, the pin is high when CDR lock is attained on the corresponding channel. Note that these pins are shared with SMBus address strap input functions read at startup.
41	ALL_DONE	ALL_DONE is don't care in SMBus slave mode. If you wish to use SMBus master mode, tie ALL_DONE of 1 retimer to READ_EN of the other retimer to prevent bus contention.		Output is 2.5 V, the pin goes low to indicate that the

				SMBus master EEPROM read has been completed.
44	READ_EN	Pulling READ_EN low is correct for SMBus slave mode. If you wish to use SMBus master mode, a transition from high to low starts the load from the EEPROM.		Input is 2.5 V, a transition from high to low starts the load from the external EEPROM. The READ_EN pin must be tied low when in SMBus slave mode
43	INT			Used to signal horizontal or vertical eye opening out of tolerance, loss of signal detect, or CDR unlock. External 2KΩ to 5KΩ pull-up resistor is required. Pin is 3.3 V LVCMOS tolerant.
20	EN_SMB	EN_SMB is pulled high on both retimers which configures SMBus slave mode. This means the EEPROMs will not be used and retimer registers can be configured via SMBus register reads and writes. If you wish to use EEPROMs to program the retimers in SMBus master mode, leave EN_SMB floating.		Input is 2.5 V, selects SMBus master mode or SMBus slave mode EN_SMB = High for slave mode EN_SMB =

				Float for master mode Tie READ_EN pin low for SMBus slave mode.
18	SDA		SDA requires an external pull-up resistor somewhere along the line.	Data Input / Open Drain Output External 2KΩ to 5KΩ pull-up resistor is required. Pin is 3.3 V LVCMOS tolerant.
17	SDC		SDC requires an external pull-up resistor somewhere along the line.	Clock Input / Open Drain Clock Output External 2KΩ to 5KΩ pull-up resistor is required. Pin is 3.3 V LVCMOS tolerant.
45, 40, 21, 16	ADDR_n		Address pins cannot be pulled both high and low at the same time. The retimers should be assigned different addresses so SMBus reads/writes can target each retimer separately.	Input is 2.5 V, the ADDR_[3:0] pins set the SMBus address for the retimer. These pins are strap inputs. Their state is read on power-up to set the SMBus address in SMBus control

				mode. High = 1KΩ to VDD, Low = 1KΩ to GND Note that these pins are shared with the lock indicator functions.
3, 6, 7, 10, 15, 46	VDD	You should confirm your power networks are configured correctly to output 2.5V. Your bypass capacitor scheme does not match our recommendation in the "power supply recommendations" section of the datasheet. If you wish to use a custom bypass capacitor scheme, you should verify that it maintains low power supply noise.		VDD = 2.5 V ± 5%
22, 27, 30, 31, 34, 39	GND			Ground reference.
PAD	DAP			Ground reference. The exposed pad at the center of the package must be connected to ground plane of the board with at least 4 vias to lower the ground impedance and improve the thermal performance of the package.

Comments