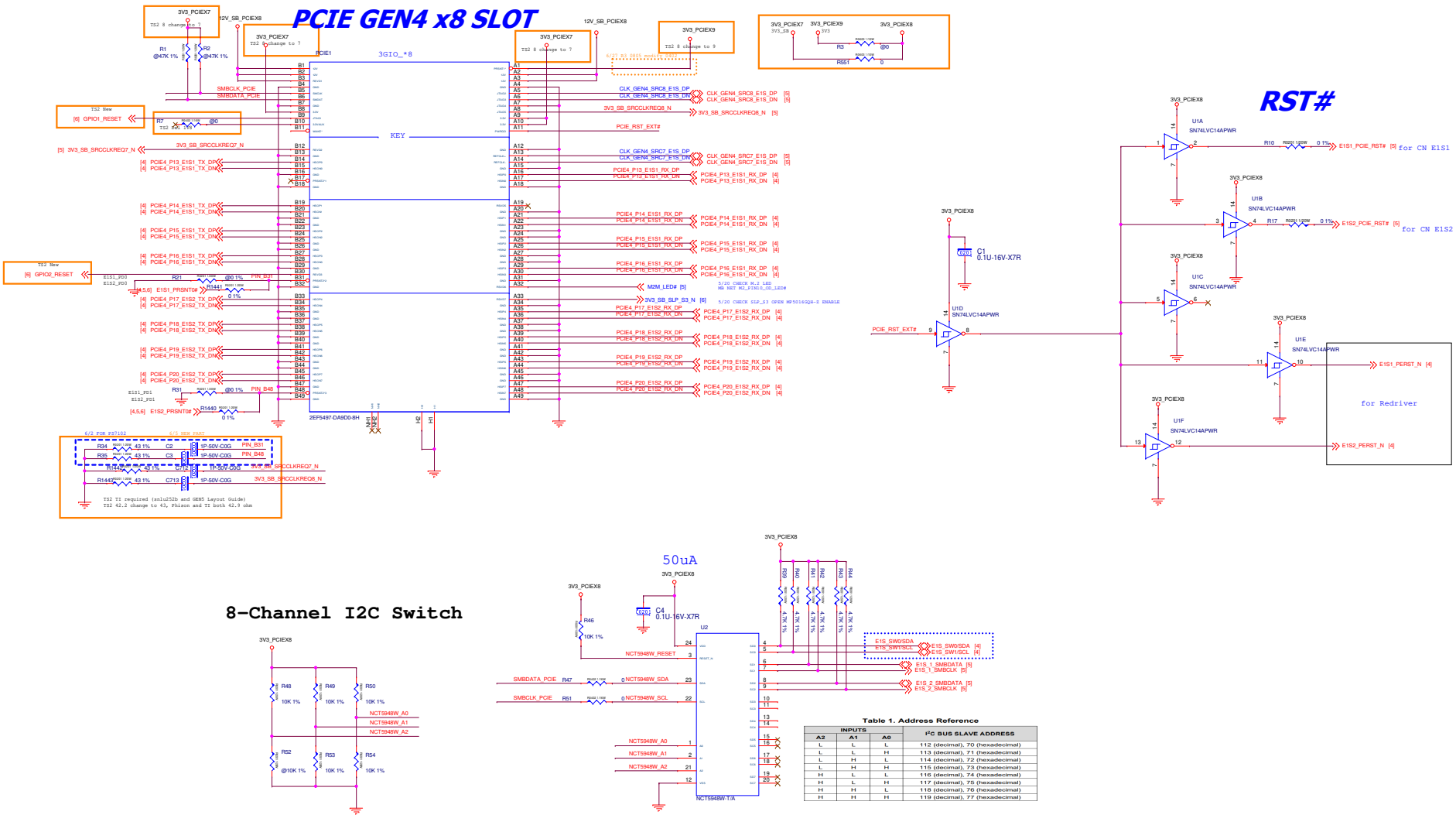
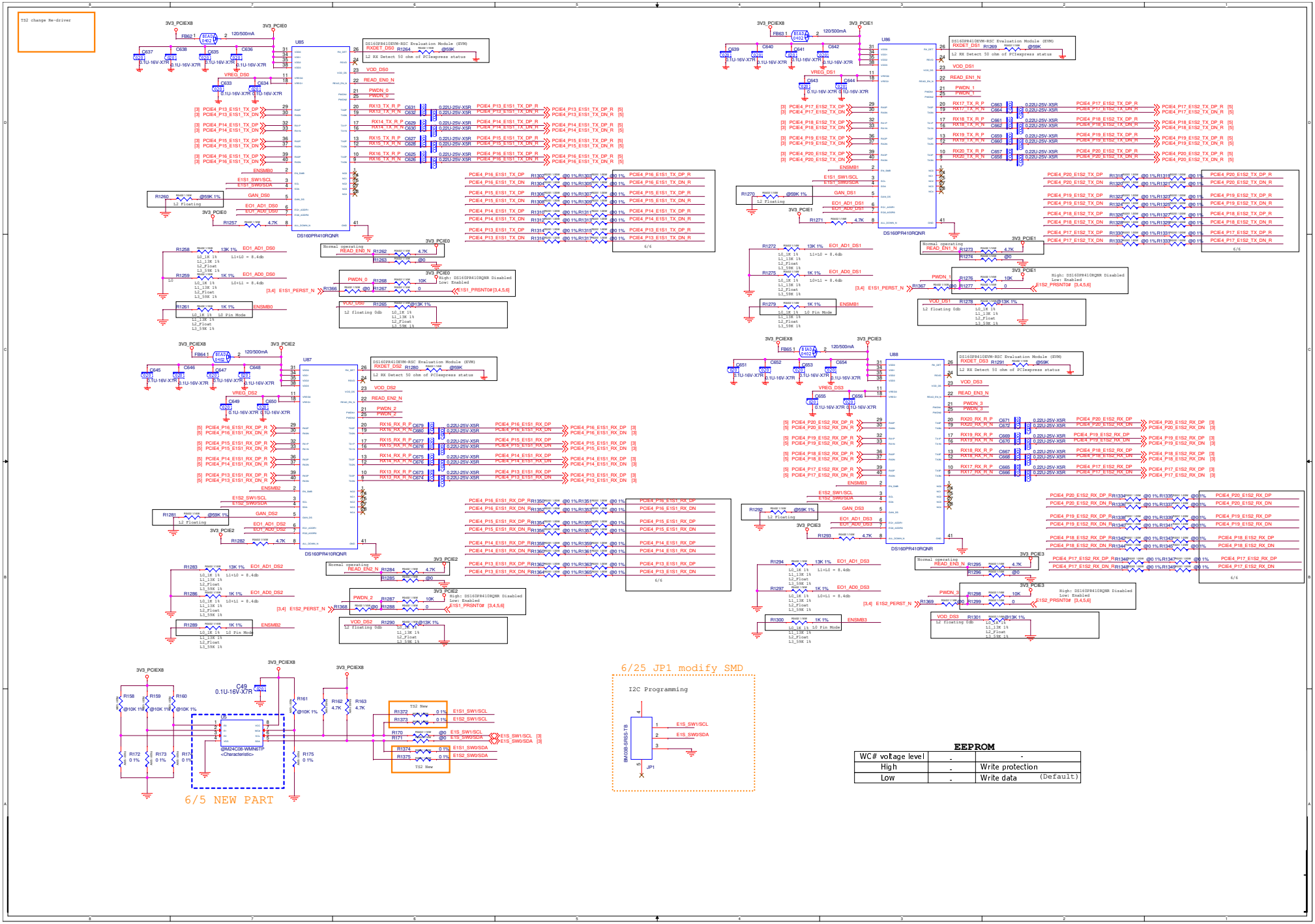
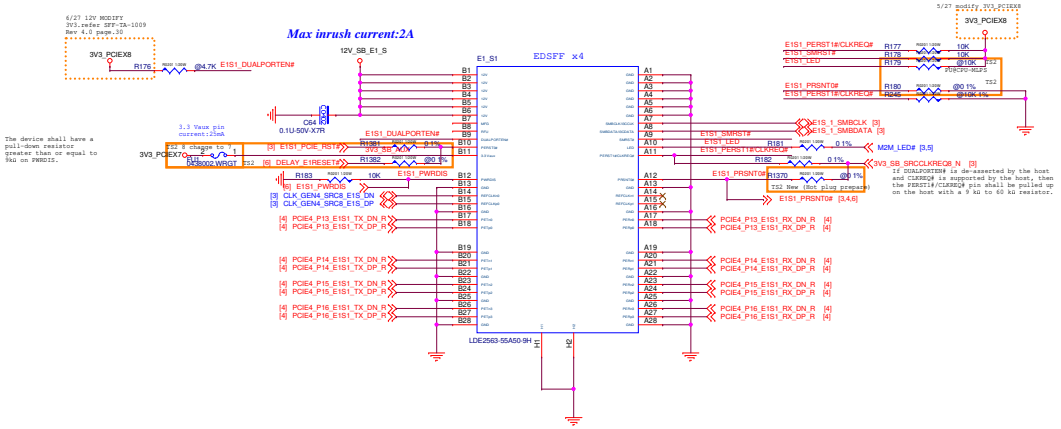


Table 1. Address Reference

INPUTS			I²C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)


TS2 change Re-driver
U85
U86
U87
U88
DS160PR410RQNR
DS160PR410EVM-RSC Evaluation Module (EVM)
L2 RX Detect 50 ohm of PCIexpress status
6/25 JP1 modify SMD
I2C Programming
6/5 NEW PART
EEPROM
WC# voltage level
High
Low
Write protection
Write data
(Default)

E1.S EDSFF x4 (1C) Connector



6.3 3.3 V Logic Signal Requirements

The 3.3 V device logic levels for single-ended digital signals (PERST[0..1]#, CLKREQ#, PRSNT[0..2]#, SMBCLK, SMBDATA, SMRST#, DUALPORTEN#, LED, PWRDIS) are defined in Table 6-4. Inputs and outputs are referenced from the device standpoint.