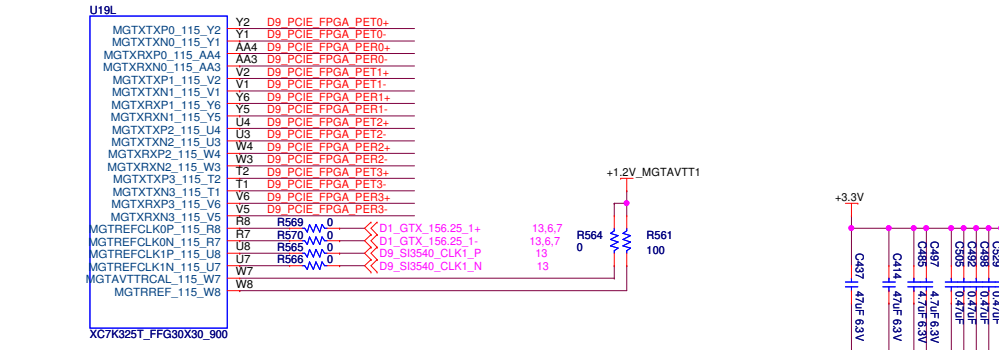
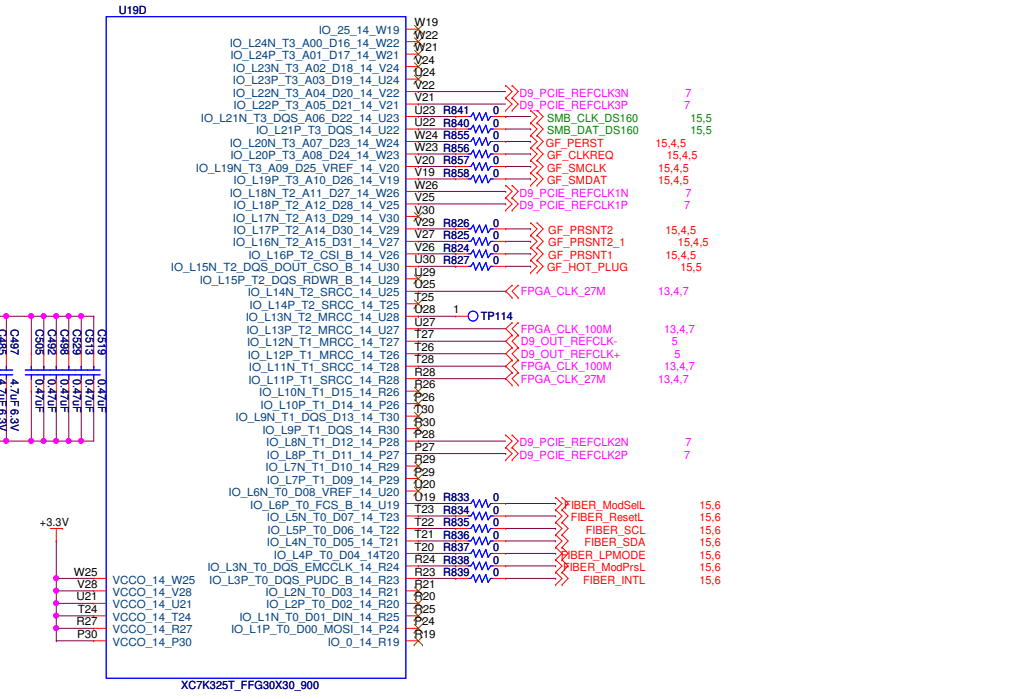
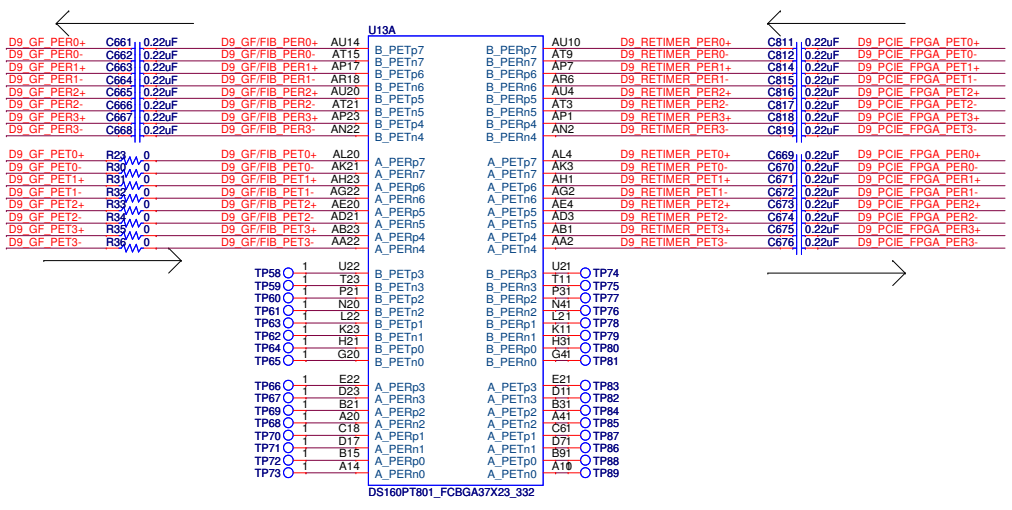
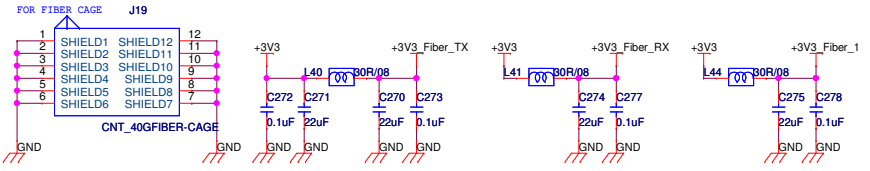


GTX 整個BAND 跟BAND 可以調換
 MGTXIX = DATA OUT
 MGTXRX = DATA IN

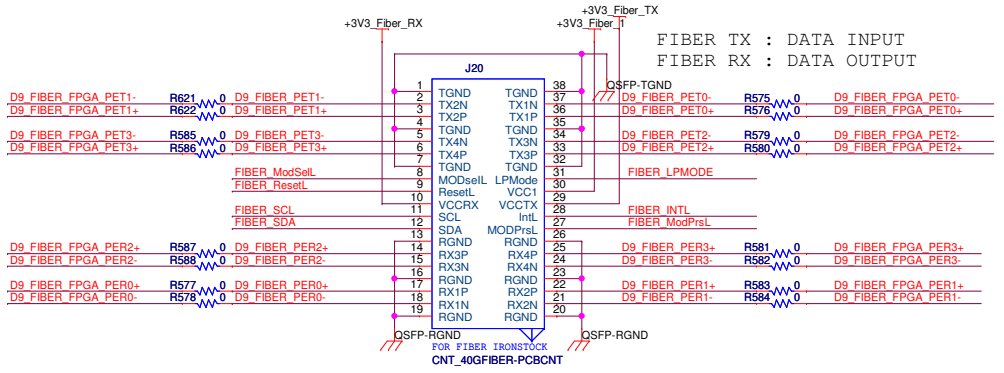


GTX 整個BAND 跟BAND 可以調換
 MGTXIX = DATA OUT
 MGTXRX = DATA IN
 GTX 預留 P/N 倆倆相放



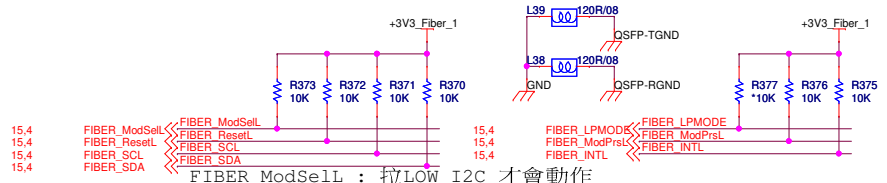


GTX 整個BAND 跟BAND 可以調換
 MGTXTX = DATA OUT
 MGTXRX = DATA IN



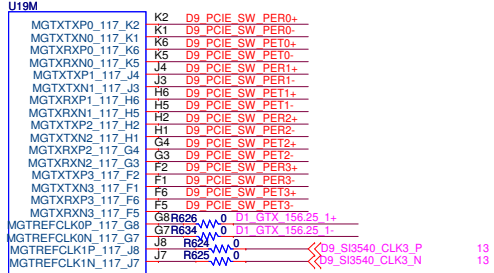
U19N		
D9 FIBER FPGA PET0+	P2	MGTXTXP0_116_P2
D9 FIBER FPGA PET0-	P1	MGTXTXN0_116_P1
D9 FIBER FPGA PER0-	T6	MGTXRXN0_116_T6
D9 FIBER FPGA PER0+	T5	MGTXRXP0_116_T5
D9 FIBER FPGA PET1+	N4	MGTXTXN1_116_N4
D9 FIBER FPGA PET1-	N3	MGTXTXN1_116_N3
D9 FIBER FPGA PER1+	R4	MGTXRXP1_116_R4
D9 FIBER FPGA PER1-	R3	MGTXRXP1_116_R3
D9 FIBER FPGA PET2+	M2	MGTXTXP2_116_M2
D9 FIBER FPGA PET2-	M1	MGTXTXN2_116_M1
D9 FIBER FPGA PER2-	P6	MGTXRXN2_116_P6
D9 FIBER FPGA PER2+	P5	MGTXRXP2_116_P5
D9 FIBER FPGA PET3+	L4	MGTXTXN2_116_L4
D9 FIBER FPGA PET3-	L3	MGTXTXP3_116_L4
D9 FIBER FPGA PER3+	M6	MGTXRXP3_116_M6
D9 FIBER FPGA PER3-	M5	MGTXRXN3_116_M5
D1 GTX_156.25_1+	L8	MGTXREFCLKOP_116_L8
D1 GTX_156.25_1-	L7	MGTXREFCLKON_116_L7
D9_S19540_CLK2_P	N8	MGTXREFCLKIP_116_N8
D9_S19540_CLK2_N	N7	MGTXREFCLKIN_116_N7

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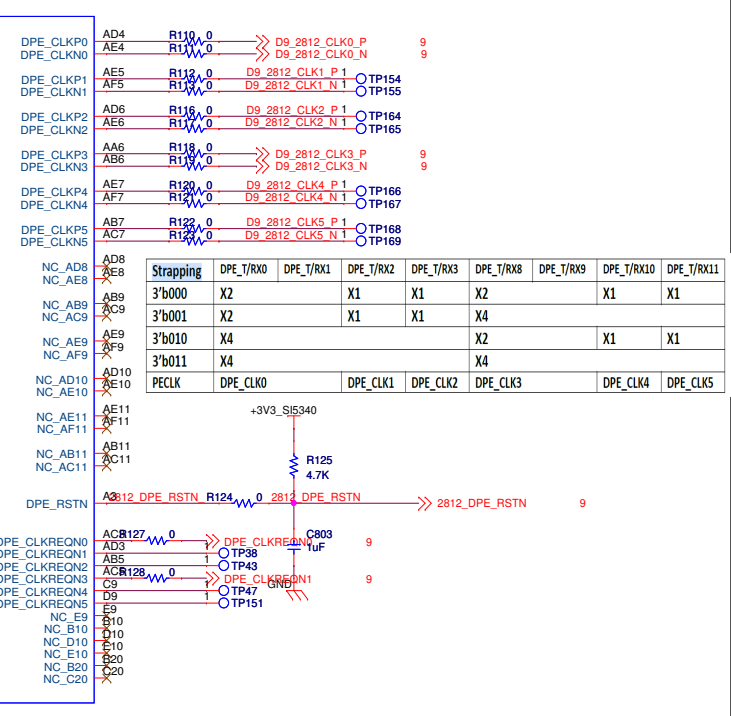
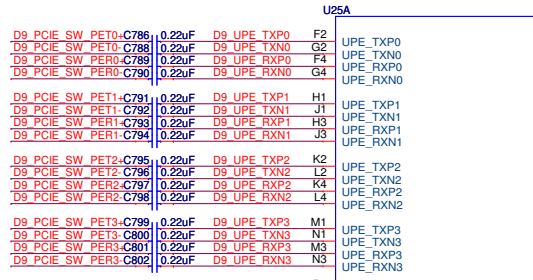


FIBER_ModSel : 拉LOW I2C 才會動作
 FIBER_ResetL : LOW RESET
 FIBER_LPMODE : PULL UP 省電
 FIBER_ModPrsL : 偵測模組插上, 插上模組內部pull low
 FIBER_INTL : 有error 會拉low / rx 沒有插上也會拉low

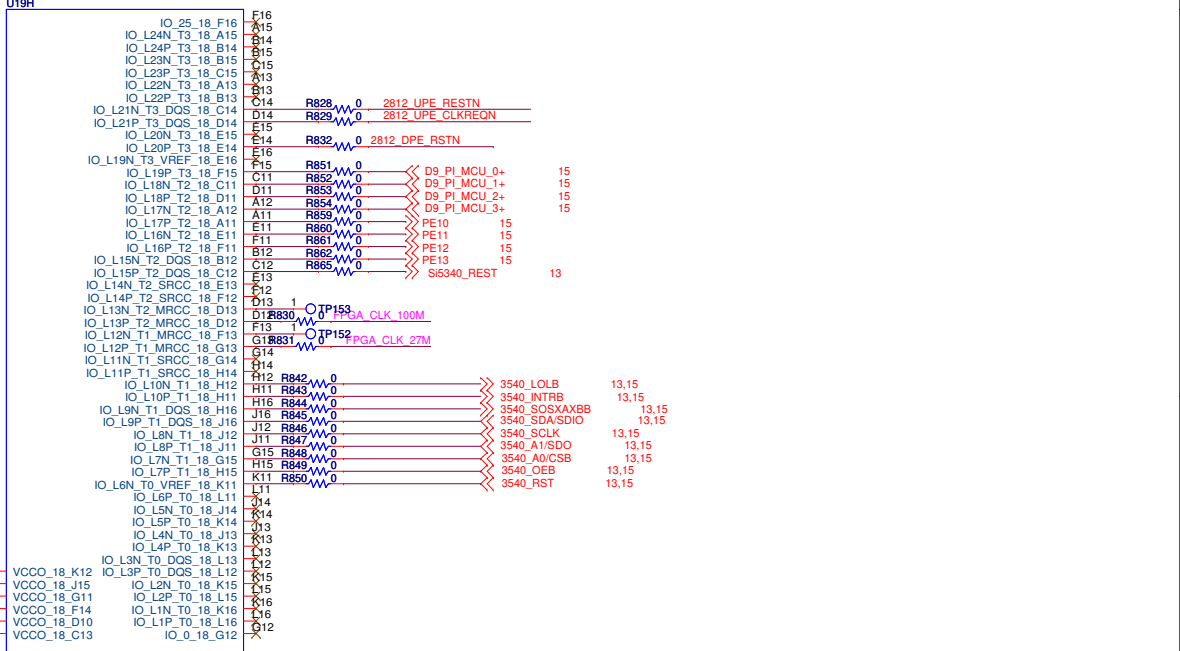
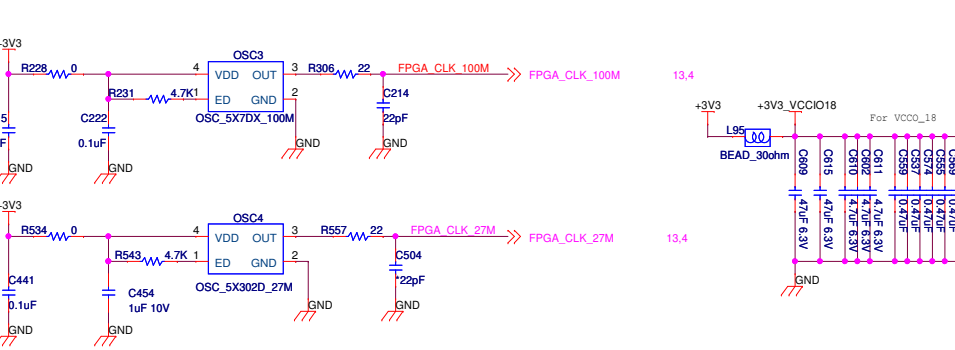
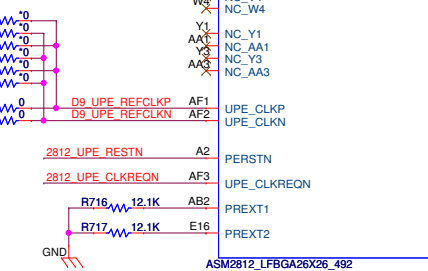
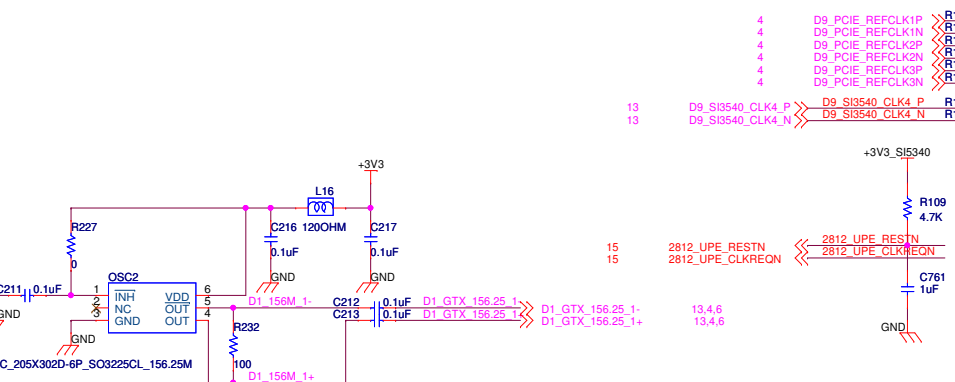
GTX 整個BAND 跟BAND 可以調換
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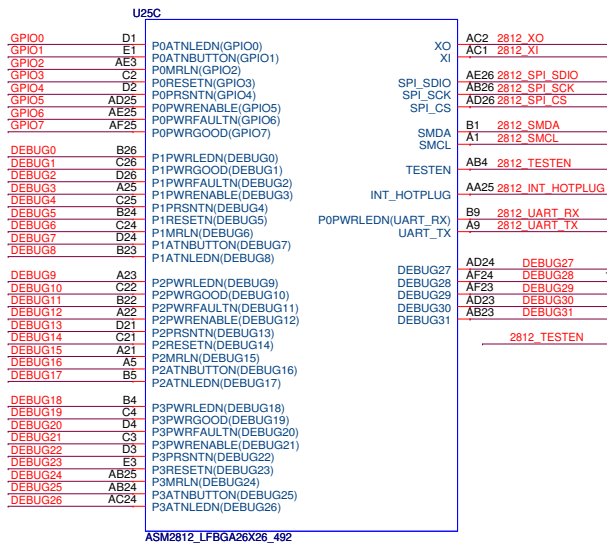
XC7K325T_FFG30X30_900



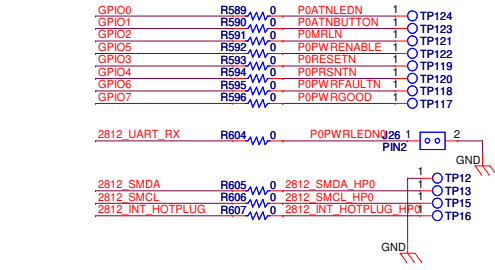
Strapping	DPE_T/RX0	DPE_T/RX1	DPE_T/RX3	DPE_T/RX8	DPE_T/RX9	DPE_T/RX10	DPE_T/RX11
3'b000	X2		X1	X2		X1	X1
3'b001	X2		X1	X1	X4		
3'b010	X4				X2	X1	X1
3'b011	X4			X4			



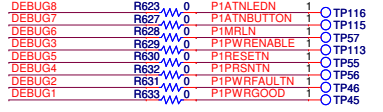
XC7K325T_FFG30X30_900



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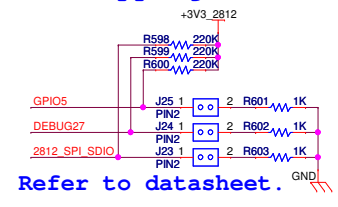
HOTPLUG Header



H/W Strapping

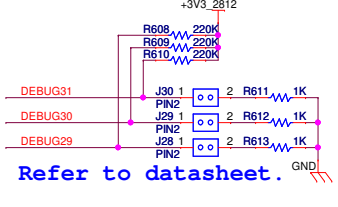
ASM2824 First 8 lane group PCIe lane configuration:

Strapping bits	LANE0	LANE1	LANE2	LANE3	LANE4	LANE5	LANE6	LANE7
gpi05, debug27, spi_sdio								
FBCLK Mapping	LANE0	LANE1	LANE2	LANE3	LANE4	LANE5	LANE6	LANE7
0 0 0	x2	x1	x1		x2	x1	x1	
0 0 1	x2	x1	x1		x4			
0 1 0		x4			x2	x1	x1	
0 1 1		x4				x4		
1 0 0				x8				



ASM2824 Second 8 lane group PCIe lane configuration:

Strapping bits	LANE8	LANE9	LANE10	LANE11	LANE12	LANE13	LANE14	LANE15
debug31, debug30, debug29								
FBCLK Mapping	LANE6	LANE7	LANE8	LANE9	LANE10	LANE11	LANE12	LANE13
0 0 0	x2	x1	x1		x2	x1	x1	
0 0 1	x2	x1	x1		x4			
0 1 0		x4			x2	x1	x1	
0 1 1		x4				x4		
1 0 0				x8				



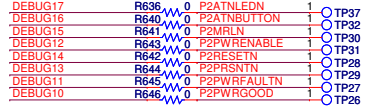
Clock mode select: SPI_SCK, UART_TX

Strapping bit	Upstream Clock
SPI_SCK	0 : 100MHz diff 1 : OSC
Strapping bit	Downstream Clock
UART_TX	0 : 100MHz diff 1 : OSC

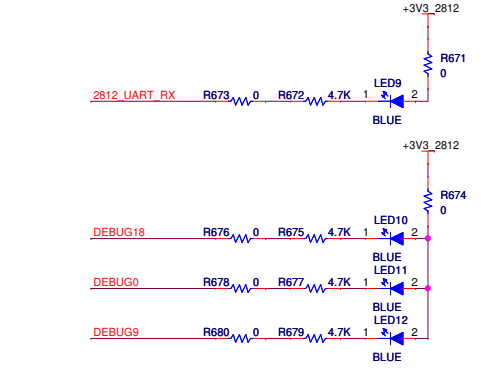
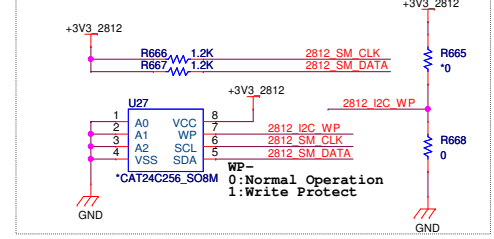
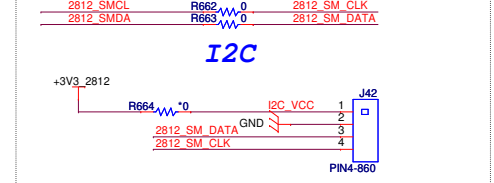
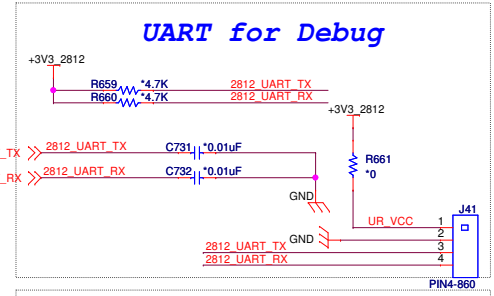
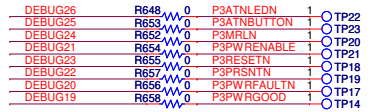


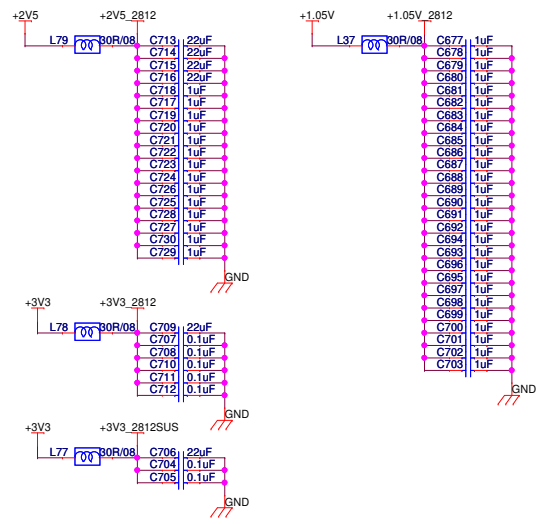
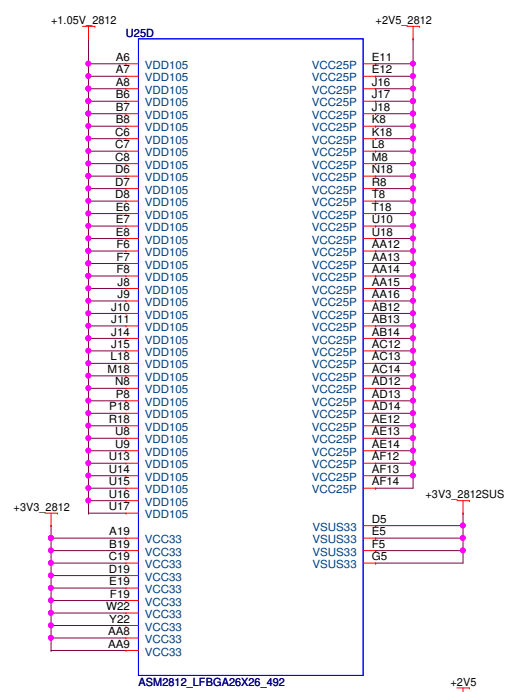
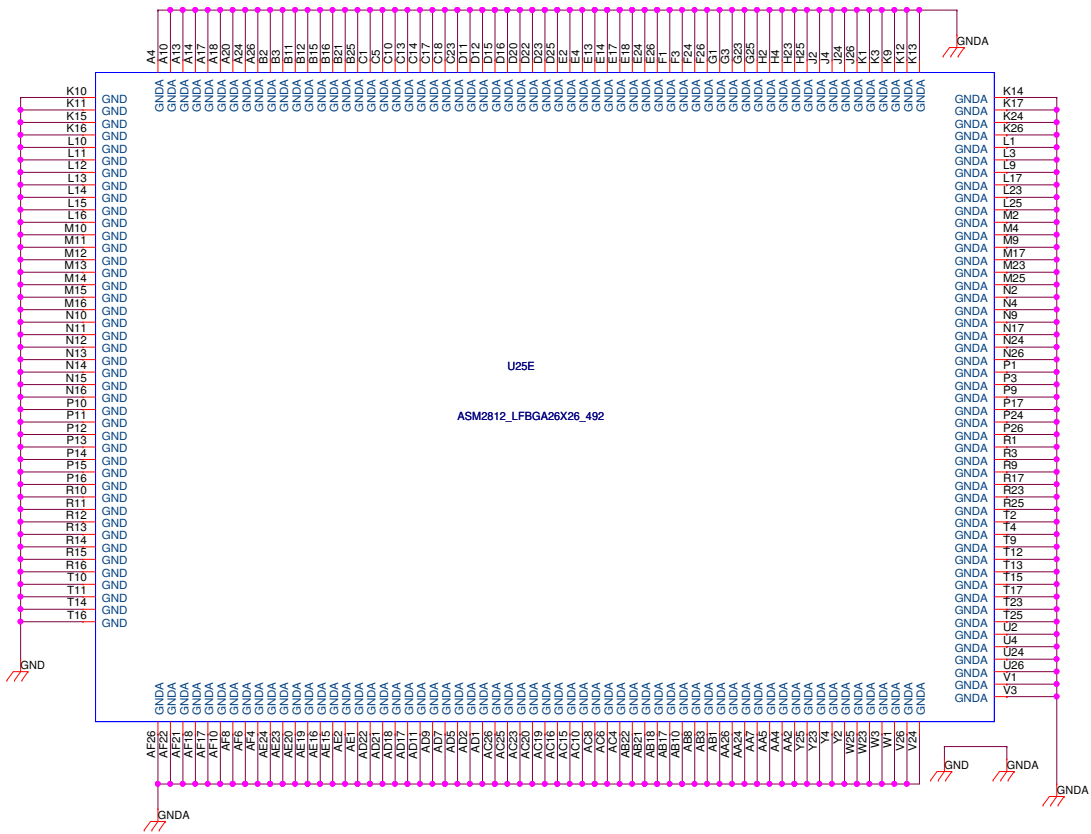
Refer to datasheet.

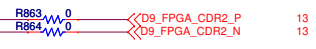
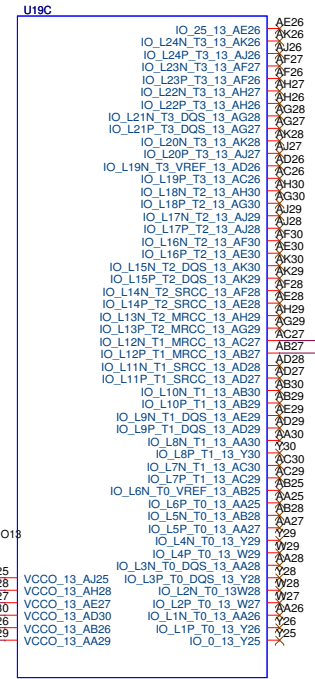
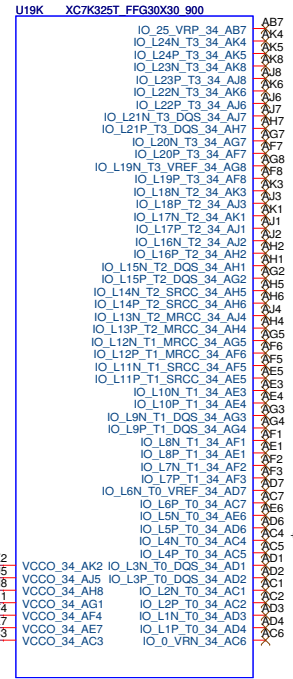
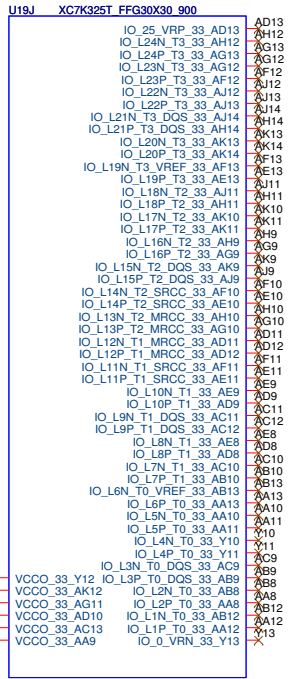
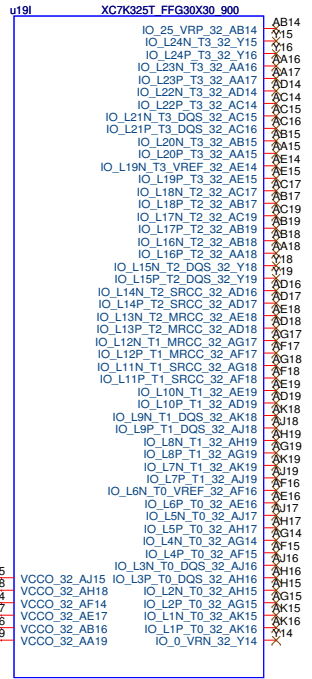
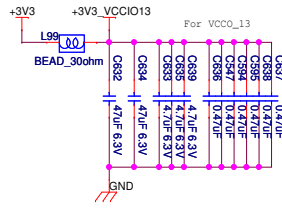
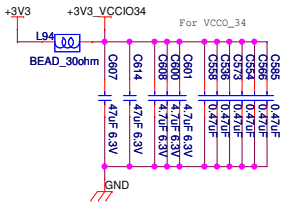
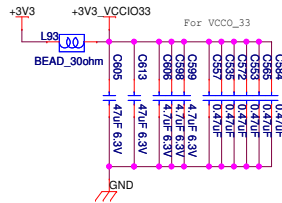
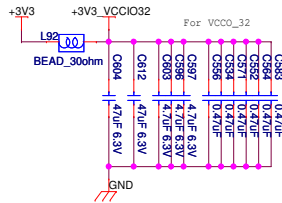
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