

DS42BR400 Single Channel Hspice Simulations

2006-01-19

Readme file for the DS42BR400 single channel hspice simulation.

1. The file singleChannel.sp contains the hspice model for a single channel of the DS42BR400. It models a switch side to line side buffer with loop back. The inputs are the SIA_0N and SIA_0P, the line side outputs are LO_0N and LO_0P and the switch side loop back outputs are SOA_0N and SOA_0P. The model includes the MUXL and MUXS inputs that control the output multiplexors. They select the SIA_0N/P inputs if they are high and a DC state (the loop back path) if they are low. The on chip decode for the output pre-emphasis is not included in this model. Use the following table to determine the output pre-emphasis:

PE Level	PRE9L/S	PRE6L/S	PRE3L/S
0db	1	1	1
-3db	1	1	0
-6db	1	0	0
-9db	0	0	0

PRE#L/S should be expanded to PRE#L or PRE#S

2. The hspice subcircuit name is SINGLECHANNEL.
3. This model has been verified at:

Temperature:	65°C
Voltage:	3.3V
Models:	typical
Resistors:	typical
4. The CMOS input levels are 0V for a low and VCC for a high.
5. The INH_BPM subckt pin should be tied high to VCC.
6. See the attached netlist and the example.pdf schematic for a simulation example.

* # FILE NAME: /HOME/DS40XB400/WORK/WORK_DLB/NETLISTS/SINGLECHANNELSIM/
* HSPICES/CONFIG/NETLIST/SINGLECHANNELSIM.C.RAW
* NETLIST OUTPUT FOR HSPICES.
* GENERATED ON JAN 17 12:09:01 2006

* GLOBAL NET DEFINITIONS
.GLOBAL VDD!
* FILE NAME: DS42BR400HSPICE_SINGLECHANNELSIM_SCHEMATIC.S.
* SUBCIRCUIT FOR CELL: SINGLECHANNELSIM.
* GENERATED FOR: HSPICES.
* GENERATED ON JAN 17 12:09:03 2006.

* Top Level Cell Instantiation *
XI260 VSS VSS LO_ONPIN LO_OPPIN MUXL MUXS SIA_ONPIN SIA_OPPIN SOA_ONPIN
+SOA_OPPIN VCC PRE3DBL PRE3DBS PRE6DBL PRE6DLBS PRE9DBL PRE9DBS VDD!
SINGLECHANNEL

V119 PRE9DBS VSS PULSE +0.00000000E+00 +3.30000000E+00 60E-9 100E-12 100E-12
+19.9E-9 80E-9
V120 PRE6DLBS VSS PULSE +0.00000000E+00 +3.30000000E+00 40E-9 100E-12 100E-12
+39.9E-9 80E-9
V109 PRE3DBL VSS PULSE +0.00000000E+00 +3.30000000E+00 20E-9 100E-12 100E-12
+59.9E-9 80E-9
V108 PRE6DBL VSS PULSE +0.00000000E+00 +3.30000000E+00 40E-9 100E-12 100E-12
+39.9E-9 80E-9
V118 PRE3DBS VSS PULSE +0.00000000E+00 +3.30000000E+00 20E-9 100E-12 100E-12
+59.9E-9 80E-9
V107 PRE9DBL VSS PULSE +0.00000000E+00 +3.30000000E+00 60E-9 100E-12 100E-12
+19.9E-9 80E-9
V0 A449 0 AC 100E-3 SIN 0.0 100E-3 1E9
V1 0 A452 AC 100E-3 SIN 0.0 100E-3 1E9
V117 MUXS VSS +3.30000000E+00
V110 MUXL VSS +3.30000000E+00
V102 A517 0 +3.30000000E+00
V103 VCC A517 0.0
V104 VSS 0 0.0
R79 VCC OUT2 50.0
R80 VCC OUT2Z 50.0
R60 VCC OUT1 50.0
R61 VCC OUT1Z 50.0
R51 A449 A531 50.0
R52 A452 A533 50.0
C32 LO_ONPIN VSS 60E-15
C35 SOA_OPPIN OUT2Z 1E-6
C36 SOA_ONPIN VSS 60E-15
C33 LO_OPPIN VSS 60E-15
C37 SOA_OPPIN VSS 60E-15
C20 LO_ONPIN OUT1 1E-6
C34 SOA_ONPIN OUT2 1E-6
C21 LO_OPPIN OUT1Z 1E-6
C38 A531 0 10E-18
C39 A533 0 10E-18
C1 A533 SIA_OPPIN 100E-9
C0 A531 SIA_ONPIN 100E-9

* INCLUDE FILES

.include "ds42br400_x1.sp"

```
* END OF NETLIST
.TRAN 2.00000E-10 3.00000E-07 START= 0.
.TEMP 65.0000
.OP
.save
.OPTION INGOLD=2 ARTIST=2 PSF=2
+ PROBE=0
.END
```