unsigned char ds90ub941\_pre\_init[] =

{

/\*register,value\*/

0x66,0x1A,

0x67,0x09, //M=9

0x66,0x03,

0x67,0x50, //200MHz Clock divider, N=80, 90MHz

0x66,0x04,

0x67,0x10, //least 8 bit of Total Horizontal frame size

0x66,0x05,

0x67,0x88, //Least 4 bit TV + Most 4 bit TH

0x66,0x06,

0x67,0x2F, //Most 8 bit of Total Vertical frame size

0x66,0x07,

0x67,0x80, //least 8 bit of active Horizontal frame size

0x66,0x08,

0x67,0x07, //Least 4 bit AV + Most 4 bit AH

0x66,0x09,

0x67,0x2D, //Most 8 bit of active Vertical frame size

0x66,0x0A,

0x67,0x0C, //Horizontal Sync Width

0x66,0x0B,

0x67,0x03, //Vertical Sync Width

0x66,0x0C,

0x67,0x20, //Horizontal back porch

0x66,0x0D,

0x67,0x18, //Vertical back porch

0x65,0x04, //using internal timing and internal clock

0x64,0xe1, //enable PG

0x30,0x01, //map interrupt pins

0x1e,0x01, //set i2c alias name for ep33 panel

0x03,0x9a, //port0 0x12 map to 0x14

0x1e,0x02, //port1 0x12 map to 0x13

0x03,0x9a,

0x1e,0x01,

0x07,0x24,

0x08,0x28,

0x1e,0x02,

0x07,0x24,

0x08,0x26,

0x70,0xd6,

0x77,0xd6,

0x71,0xd6,

0x78,0xd8,

0x1e,0x01, //passthrough i2c dev to soc side

0x17,0x9e,

0x0d,0x37, //config for gpio0

0x1e,0x02,

0x17,0x9e,

0x0d,0x37, //config for dgpio0

0x1e,0x04,

0x17,0x9e,

};

unsigned char ds90ub941\_split\_mode\_720p[] =

{

/\*register, value\*/

0x01,0xff, //Reset 941& Disable DSI

0x1E,0x01, //Select FPD-Link III Port 0

0x4F,0x8C, //Set DSI\_CONTINUOUS\_CLOCK, 4 lanes, DSI Port 0

0x5B,0x07, //Force Splitter mode

0x56,0x80, //Enable Left/Right 3D processing to allow superframe splitting

0x1E,0x02, //Select FPD-Link III Port 1

0x4F,0x8C, //Set DSI\_CONTINUOUS\_CLOCK, 4 lanes, DSI Port 1

0x5B,0x07, //Force Splitter mode

0x56,0x80, //Enable Left/Right 3D processing to allow superframe splitting

0x32,0x00, //Set the line size to 1280(LSB)

0x33,0x05, //Set the line size to 1280 (MSB)

0x1E,0x01, //Select FPD-Link III Port 0

0x36,0x00, //Set crop start X position to 0 (LSB)

0x37,0x80, //Set crop start X position to 0 (MSB) and enable cropping

0x38,0xFF, //Set crop stop X position to 1279 (LSB)

0x39,0x04, //Set crop stop X position to 1279 (MSB)

0x3A,0x00, //Set crop start Y position to 0 (LSB)

0x3B,0x00, //Set crop start Y position to 0 (MSB)

0x3C,0xCF, //Set crop stop Y position to 719 (LSB)

0x3D,0x02, //Set crop stop Y position to 719 (MSB)

0x1E,0x02, //Select FPD-Link III Port 1

0x36,0x00, //Set crop start X position to 0 (LSB)

0x37,0x80, //Set crop start X position to 0 (MSB) and enable cropping

0x38,0xFF, //Set crop stop X position to 1279 (LSB)

0x39,0x04, //Set crop stop X position to 1279 (MSB)

0x3A,0x00, //Set crop start Y position to 0 (LSB)

0x3B,0x00, //Set crop start Y position to 0 (MSB)

0x3C,0xCF, //Set crop stop Y position to 719 (LSB)

0x3D,0x02, //Set crop stop Y position to 719 (MSB)

0x40,0x04, //Select DSI Port 0 digital registers

0x41,0x05, //Select DPHY\_SKIP\_TIMING register

0x42,0x14, //Write TSKIP\_CNT value for 300 MHz DSI clock frequency

0x30,0x01, //Disable port1 remote interrupt due to we use same hw panel for touch interrupt

0x01,0x00, //enable DSI

0x30,0x01, //map interrupt pins

0x1e,0x01, //set i2c alias name for ep33 panel

0x03,0x9a, //port0 0x12 map to 0x14

0x1e,0x02, //port1 0x12 map to 0x13

0x03,0x9a,

0x1e,0x01,

0x07,0x24,

0x08,0x28,

0x1e,0x02,

0x07,0x24,

0x08,0x26,

0x70,0xd6,

0x77,0xd6,

0x71,0xd6,

0x78,0xd8,

0x1e,0x01,

0x17,0x9e,

0x0d,0x37, //config for gpio0

0x1e,0x02,

0x17,0x9e,

0x0d,0x37, //config for dgpio0

0x1e,0x04,

0x17,0x9e,

};