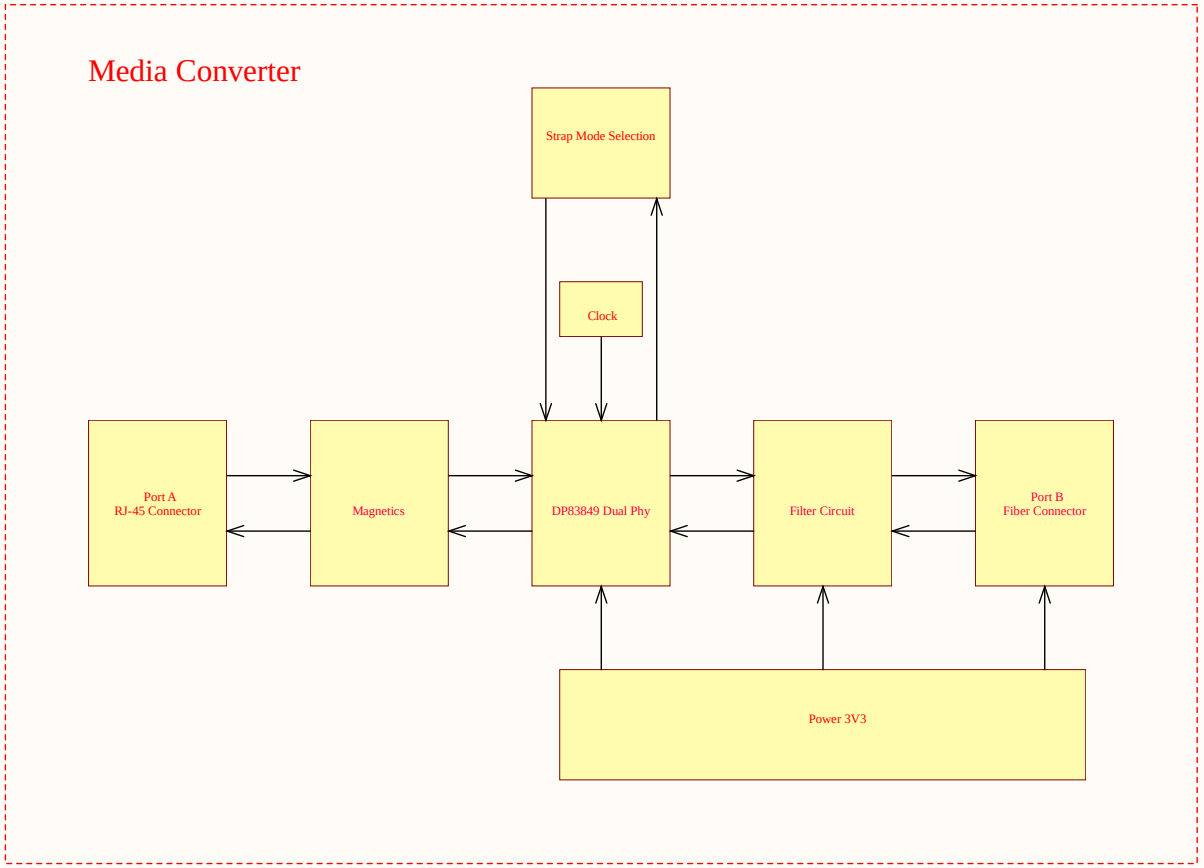
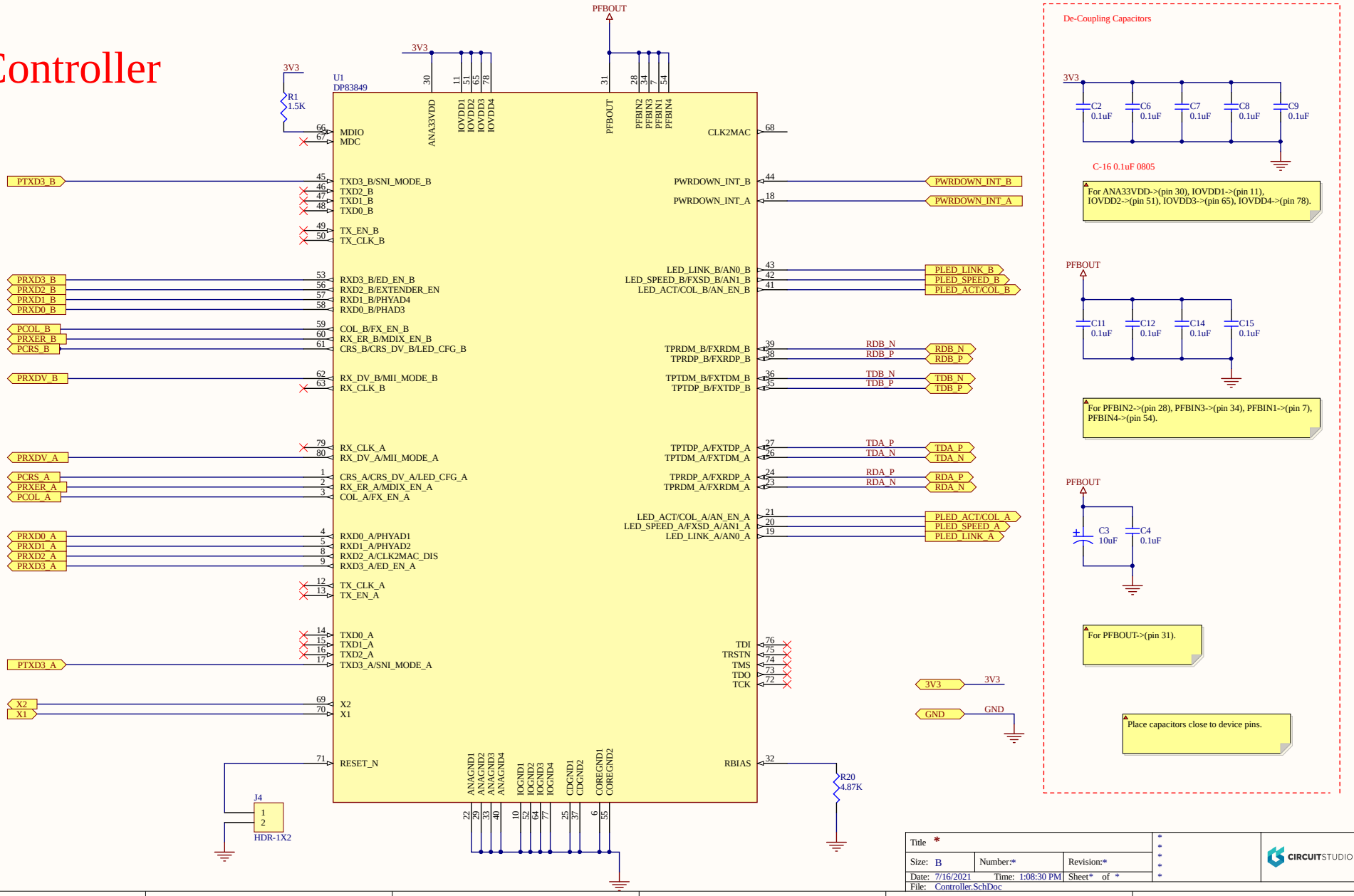
Block Diagram



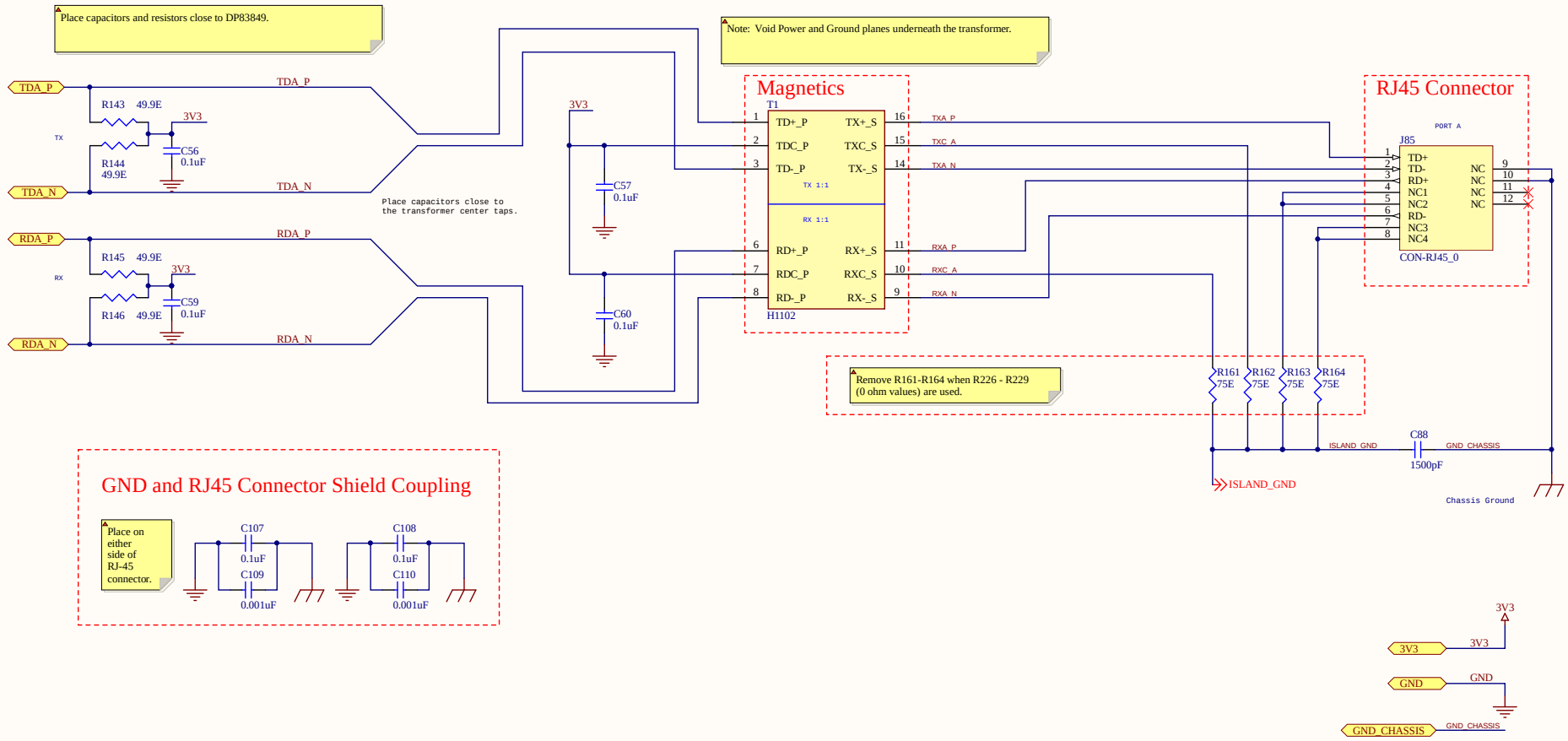
Title	***Ethernet to Fiber (Media Converter)***		*Axxonet System Technologies* *Christ School Road* *Bangalore* *India* *axxonet.com*
Size: B	Number:0	Revision:V1.0	
Date: 7/16/2021	Time: 1:08:30 PM	Sheet0 of 7	
File: Block Diagram.SchDoc			

CIRCUITSTUDIO

Controller


U1
DP83849
3V3
R1
1.5K
MDIO
MDC
PTXD3_B
TXD3_B/SNI_MODE_B
TXD2_B
TXD1_B
TXD0_B
TX_EN_B
TX_CLK_B
PRXD3_B
PRXD2_B
PRXD1_B
PRXD0_B
RXD3_B/ED_EN_B
RXD2_B/EXTENDER_EN
RXD1_B/PHYAD4
RXD0_B/PHAD3
PCOL_B
PRXER_B
PCRS_B
COL_B/FX_EN_B
RX_ER_B/MDIX_EN_B
CRS_B/CRS_DV_B/LED_CFG_B
PRXDV_B
RX_DV_B/MII_MODE_B
RX_CLK_B
PRXDV_A
RX_CLK_A
RX_DV_A/MII_MODE_A
PCRS_A
PRXER_A
PCOL_A
CRS_A/CRS_DV_A/LED_CFG_A
RX_ER_A/MDIX_EN_A
COL_A/FX_EN_A
PRXD0_A
PRXD1_A
PRXD2_A
PRXD3_A
RXD0_A/PHYAD1
RXD1_A/PHYAD2
RXD2_A/CLK2MAC_DIS
RXD3_A/ED_EN_A
TX_CLK_A
TX_EN_A
PTXD3_A
TXD0_A
TXD1_A
TXD2_A
TXD3_A/SNI_MODE_A
X2
X1
RESET_N
J4
HDR-1X2
ANA33VDD
IOVDD1
IOVDD2
IOVDD3
IOVDD4
PFBOUT
PFBIN2
PFBIN3
PFBIN1
PFBIN4
CLK2MAC
PWRDOWN_INT_B
PWRDOWN_INT_A
LED_LINK_B/AN0_B
LED_SPEED_B/FXSD_B/AN1_B
LED_ACT/COL_B/AN_EN_B
TPRDM_B/FXRDM_B
TPRDP_B/FXRDP_B
TPTDM_B/FXTDM_B
TPTDP_B/FXTDP_B
TPTDP_A/FXTDP_A
TPTDM_A/FXTDM_A
TPRDP_A/FXRDP_A
TPRDM_A/FXRDM_A
LED_ACT/COL_A/AN_EN_A
LED_SPEED_A/FXSD_A/AN1_A
LED_LINK_A/AN0_A
TDI
TRSTN
TMS
TDO
TCK
RBIAS
R20
4.87K
ANAGND1
ANAGND2
ANAGND3
ANAGND4
IOGND1
IOGND2
IOGND3
IOGND4
CDGND1
CDGND2
COREGND1
COREGND2
PWRDOWN_INT_B
PWRDOWN_INT_A
PLED_LINK_B
PLED_SPEED_B
PLED_ACT/COL_B
RDB_N
RDB_P
TDB_N
TDB_P
TDA_P
TDA_N
RDA_P
RDA_N
PLED_ACT/COL_A
PLED_SPEED_A
PLED_LINK_A
GND
De-Coupling Capacitors
C2 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C-16 0.1uF 0805
For ANA33VDD->(pin 30), IOVDD1->(pin 11), IOVDD2->(pin 51), IOVDD3->(pin 65), IOVDD4->(pin 78).
C11 0.1uF
C12 0.1uF
C14 0.1uF
C15 0.1uF
For PFBIN2->(pin 28), PFBIN3->(pin 34), PFBIN1->(pin 7), PFBIN4->(pin 54).
C3 10uF
C4 0.1uF
For PFBOUT->(pin 31).
Place capacitors close to device pins.
Title *
Size: B
Number:*
Revision:*
Date: 7/16/2021
Time: 1:08:30 PM
Sheet* of *
File: Controller.SchDoc
CIRCUITSTUDIO

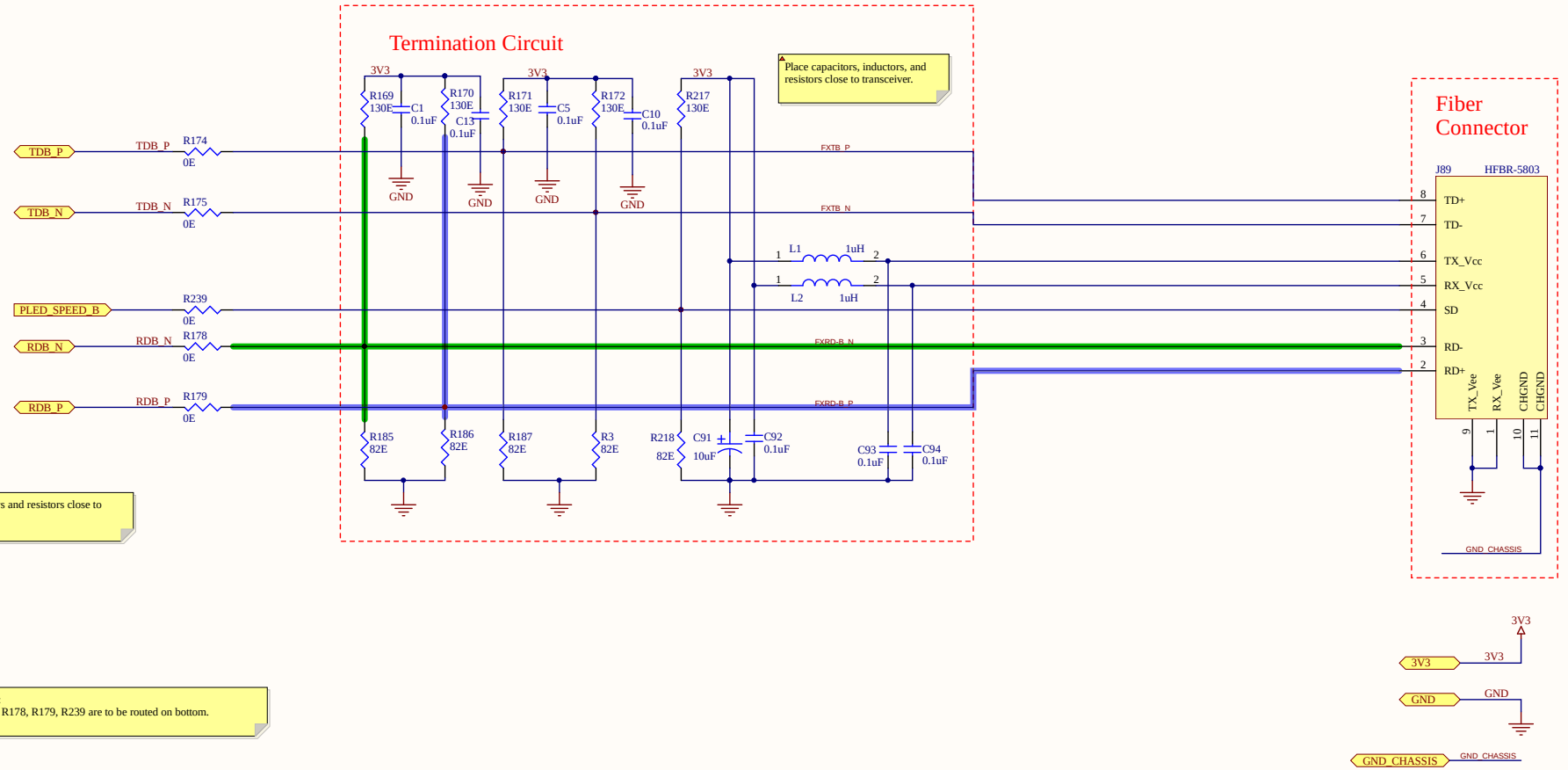
Port A Ethernet



Title *			
Size: B	Number:*	Revision:*	
Date: 7/16/2021	Time: 1:08:30 PM	Sheet* of *	
File: Port A Ethernet.SchDoc			

CIRCUITSTUDIO

Port B Fiber

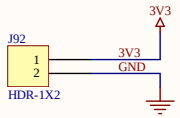


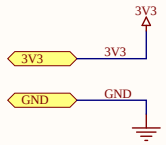
Title *			
Size: B	Number:*	Revision:*	
Date: 7/16/2021	Time: 1:08:30 PM	Sheet* of *	
File: Port B Fiber.SchDoc			

CIRCUITSTUDIO

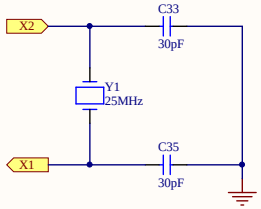
Power Connector and Clock

Power Connector





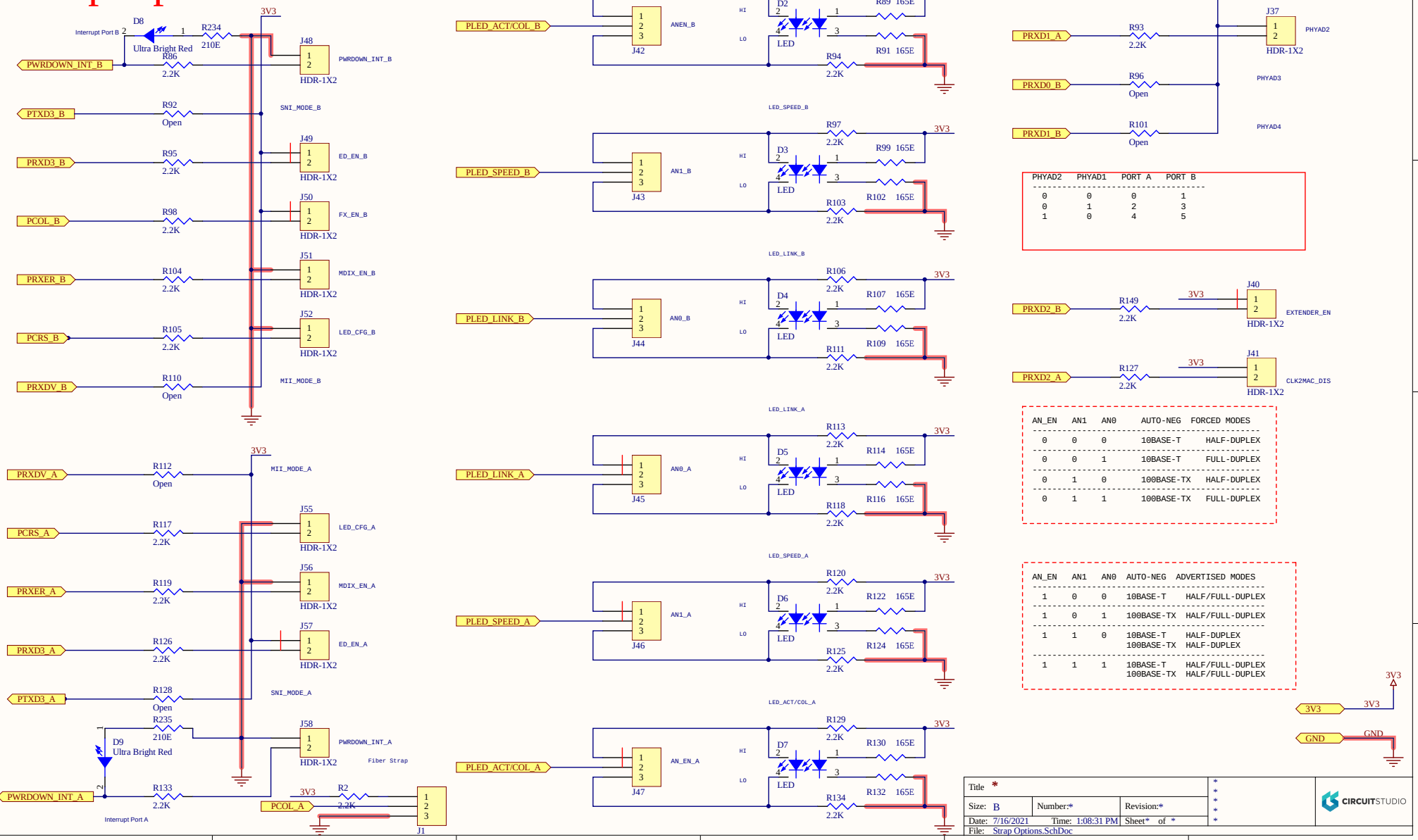
Clock (Crystal)



Title *			
Size: B	Number:*	Revision:*	
Date: 7/16/2021	Time: 1:08:31 PM	Sheet* of *	
File: Power and Clock.SchDoc			

CIRCUITSTUDIO

Strap Options



PHYAD2	PHYAD1	PORT A	PORT B
0	0	0	1
0	1	2	3
1	0	4	5

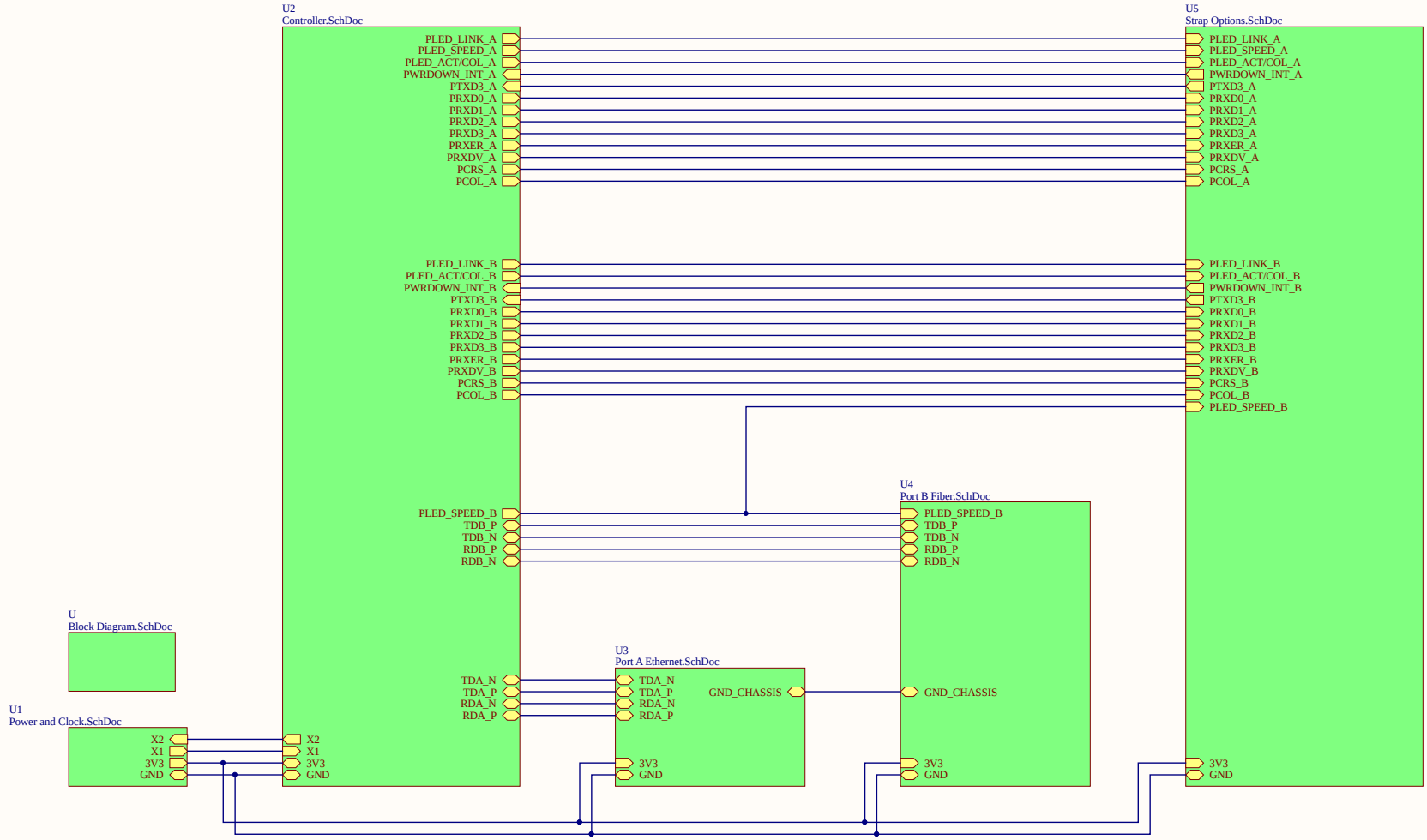
AN_EN	AN1	AN0	AUTO-NEG	FORCED MODES
0	0	0	10BASE-T	HALF-DUPLEX
0	0	1	10BASE-T	FULL-DUPLEX
0	1	0	100BASE-TX	HALF-DUPLEX
0	1	1	100BASE-TX	FULL-DUPLEX

AN_EN	AN1	AN0	AUTO-NEG	ADVERTISED MODES
1	0	0	10BASE-T	HALF/FULL-DUPLEX
1	0	1	100BASE-TX	HALF/FULL-DUPLEX
1	1	0	10BASE-T 100BASE-TX	HALF-DUPLEX HALF-DUPLEX
1	1	1	10BASE-T 100BASE-TX	HALF/FULL-DUPLEX HALF/FULL-DUPLEX

Title *			
Size: B	Number:*	Revision:*	
Date: 7/16/2021	Time: 1:08:31 PM	Sheet* of *	
File: Strap Options.SchDoc			

CIRCUITSTUDIO

Top Sheet



Title *			
Size: B	Number:*	Revision:*	
Date: 7/16/2021	Time: 1:08:31 PM	Sheet* of *	
File: Top Sheet.SchDoc			

CIRCUITSTUDIO