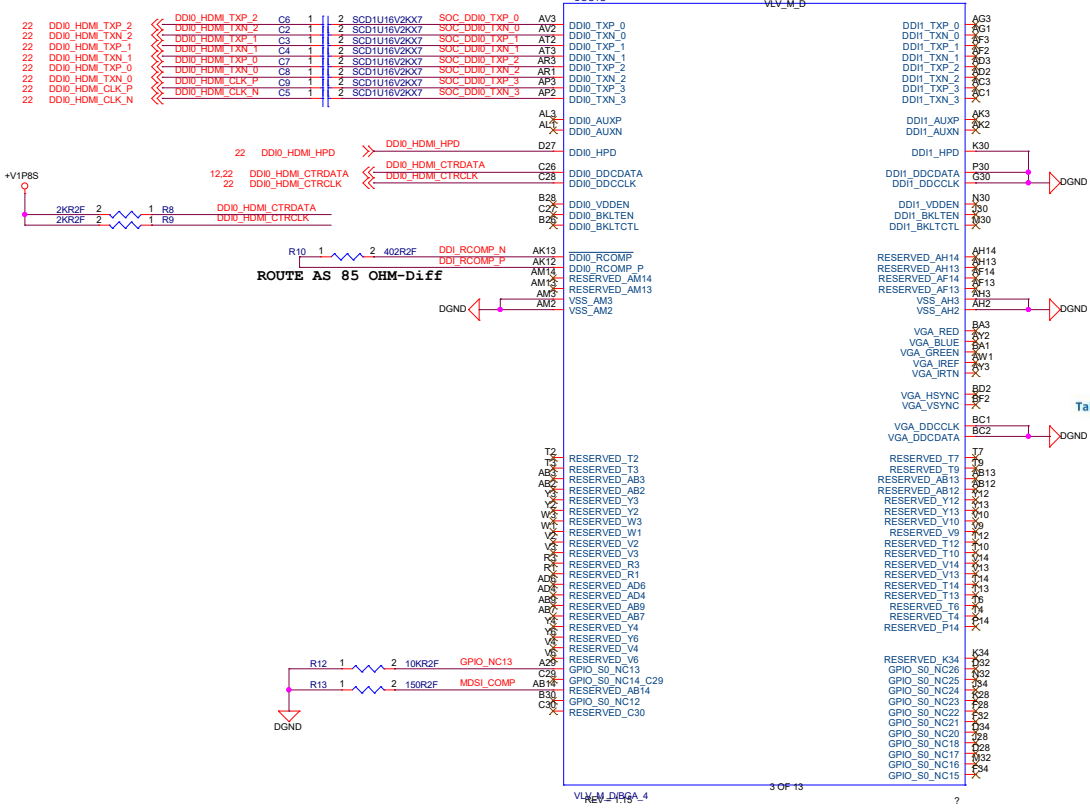


```

HDMI/DVI_DAT_2 <=> DDI_TX_0
HDMI/DVI_DAT_1 <=> DDI_TX_1
HDMI/DVI_DAT_0 <=> DDI_TX_2
HDMI/DVI_CLK_ <=> DDI_TX_3
eDP/DP_DAT_0 <=> DDI_TX_0
eDP/DP_DAT_1 <=> DDI_TX_1
eDP/DP_DAT_2 <=> DDI_TX_2
eDP/DP_DAT_3 <=> DDI_TX_3

```



7.2.6 DDI Disable Guidelines

Table 7-19 shows the recommended termination when DDI interface is not implemented.

Table 7-19. DDI Disable Guidelines

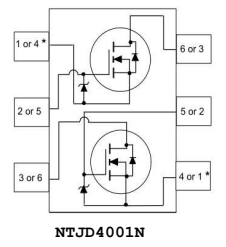
Signal	Recommendation
DDIx_TXP[3:0] DDIx_TXN[3:0]	NC
DDIx_AUXP DDIx_AUXN	NC
DDIx_HPDP DDIx_DDCCLK DDIx_DDCDATA	GND
DDIx_VDDEN DDIx_BKLTEN DDIx_BKLCTL	NC
DDI_RCOMP_P/N	NC

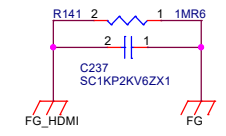
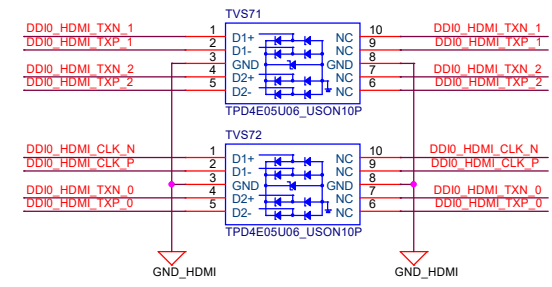
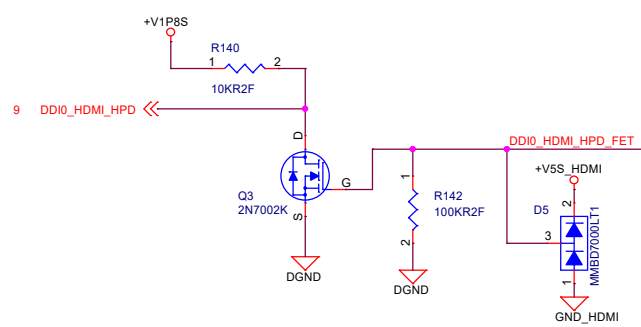
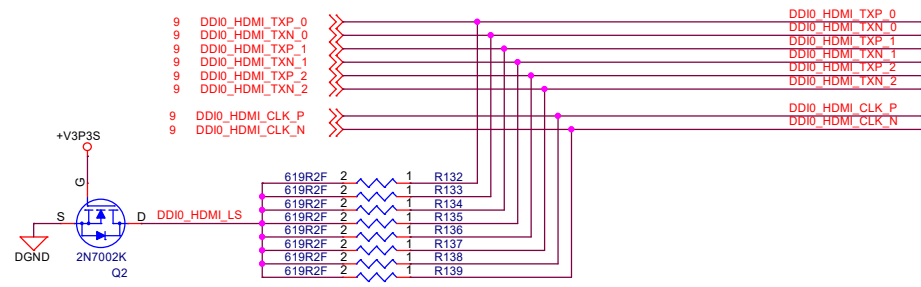
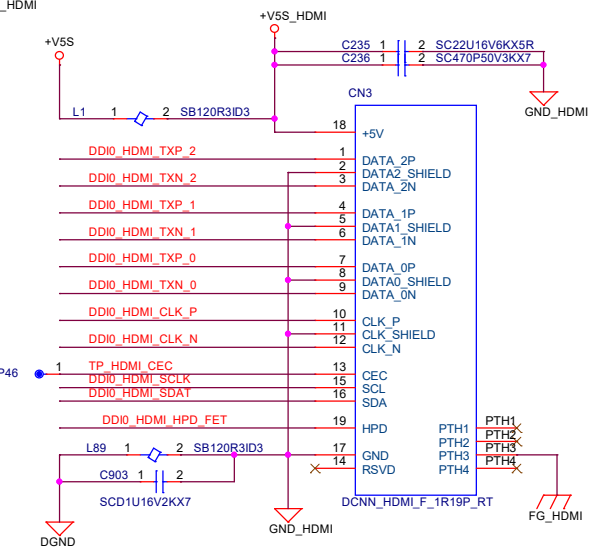
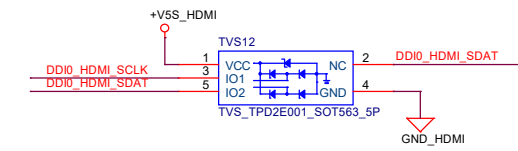
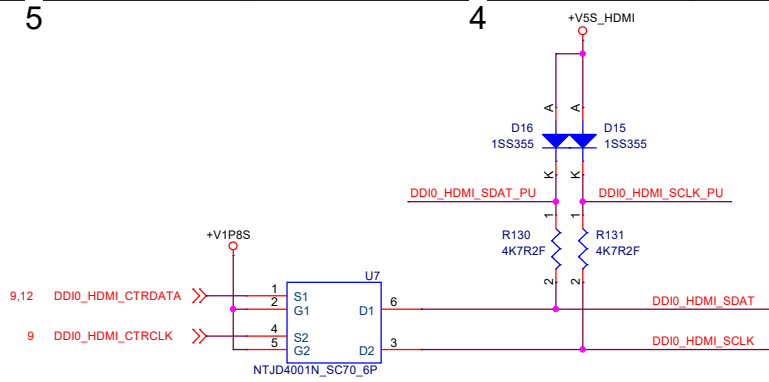
Table 8-9. VGA/CRT Disable Guideline

Signal	Recommendation
VGA_RED VGA_GREEN VGA_BLUE VGA_HSYNC, VGA_VSYNC VGA_IRTN, VGA_IREF	NC
VGA_DDCCLK, VGA_DDCDATA	GND

Configuration Pin Mapping for DDI Ports

PORT	DDI Pin Names	DisplayPort* Mapping	HDMI Mapping
PORT-0	DDIO_TXP[0]	DPO_MAINP[0]	TMDS0_DATAP[2]
	DDIO_TXN[0]	DPO_MAINN[0]	TMDS0_DATAN[2]
	DDIO_TXP[1]	DPO_MAINP[1]	TMDS0_DATAP[1]
	DDIO_TXN[1]	DPO_MAINN[1]	TMDS0_DATAN[1]
	DDIO_TXP[2]	DPO_MAINP[2]	TMDS0_DATAP[0]
	DDIO_TXN[2]	DPO_MAINN[2]	TMDS0_DATAN[0]
	DDIO_TXP[3]	DPO_MAINP[3]	TMDS0_CLKP
	DDIO_TXN[3]	DPO_MAINN[3]	TMDS0_CLKN
	DDIO_AUXP	DPO_AUXP	NA
	DDIO_AUXN	DPO_AUXN	NA
	DDIO_HPDP	DPO_HPDP	TMDS0_HPDP
	DDIO_DDCCLK	NA	TMDS0_DDCCLK
	DDIO_DDCDATA	DPO_EN	TMDS0_DDCDATA
	DDIO_VDDEN	EDPO_VDDEN	NA
	DDIO_BKLTEN	EDPO_BKLTEN	NA
	DDIO_BKLCTL	EDPO_BKLCTL	NA
	DDI_RCOMP_P	NA	NA
	DDI_RCOMP_N	NA	NA





台達電子工業股份有限公司
Delta Electronics, Inc.

Date: Thursday, December 12, 2019 REV: <LY.REV> Drawn: <Drawn>

PWB:<PWB> FILE NAME: MH2-P10N-N00D0

DESCRIPTION:
22_HDMI CONN

Checked Approved PART NO: REV SHEET

<PART NO> R00 22 OF 39

THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF SYN-TEK AUTOMATION, INC. AND SHALL NOT BE REPRODUCED OR USED AS THE BASIS FOR THE MANUFACTURE OR SELL OF APPARATUS OR DEVICES WITHOUT PERMISSION