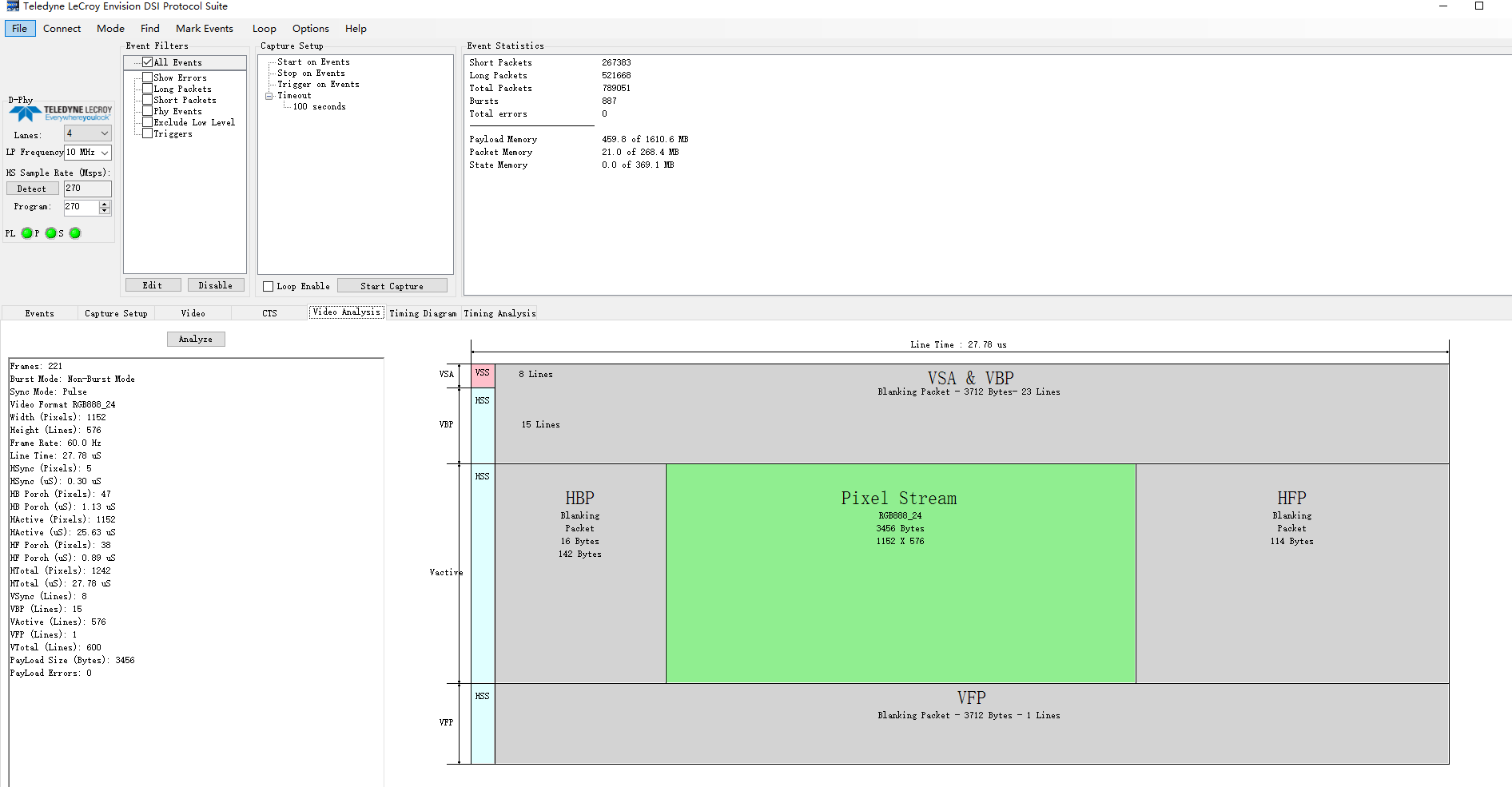
Refer to snla356-DS90UB941AS-Q1 DSI Bringup Guide-->4.3 Incorrect DSI Packet Timing, use mipi analyzer to analyze and adjust imx8 dsi stream, but the backend dlpc230 still reports an error and cannot display: "Open LDI total pixels per line are unstable "

1. Attached are the dsi source events we captured through the mipi analyzer. The hfp, hbp, hsync timings are very close to the theoretical values. Please help analyze whether the front-end dsi source still has problems, why the back-end dlpc230 still reports an error of Open LDI total pixels per line are unstable.
2. Please help to provide a dsi source events with a front-end resolution of 1152\*576, 60Hz, which can be displayed normally on the dlpc230 for our reference.



Mipi analyzer screenshot 1--video\_analysis



Mipi analyzer screen shot 2--events

Block diagram：

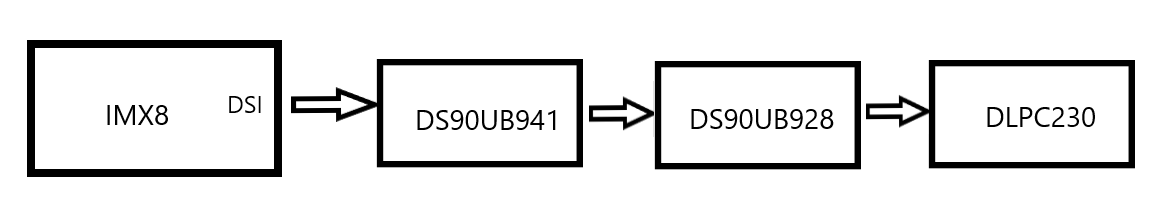


Fig 3. Block diagram

I.MX8 SoC timing configuration ：

       clock = 45000,

       hdisplay = 1152,

       hfront\_porch = 40,

       hsync\_len = 8,

       hback\_porch = 50, （but on last line HBP has been tested having 35 more clocks）

       vdisplay = 576,

       vfront\_porch = 1,

       vsync\_len =  8,

       vback\_porch = 15,

       vrefresh = 60,

dsi source timing test result：

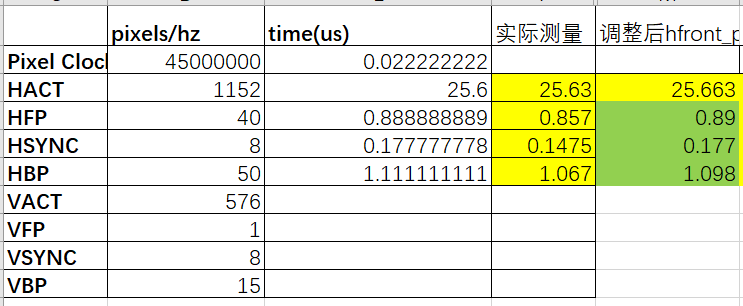
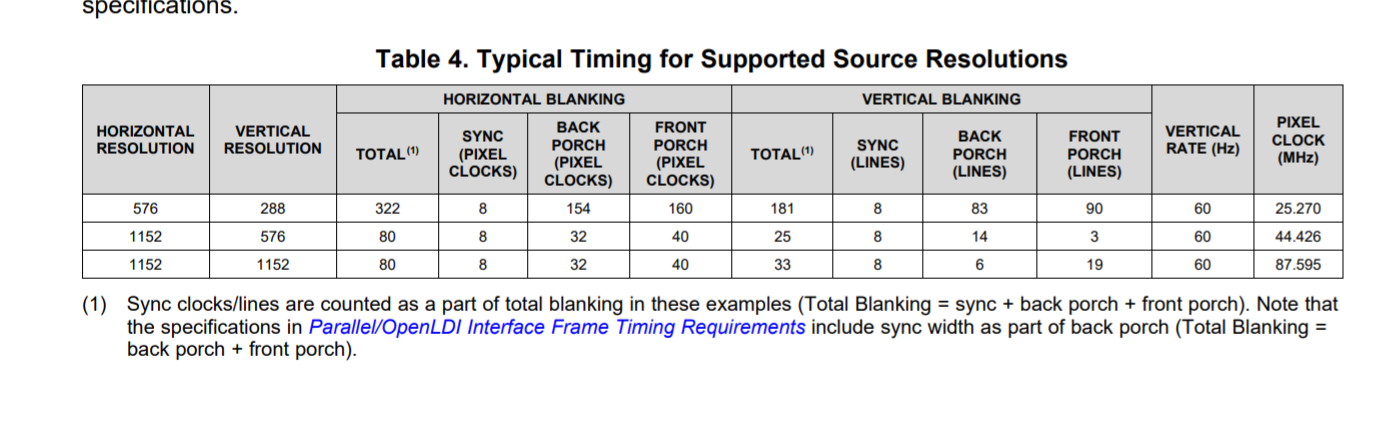


Fig 4--dsi source test data, the 4th column means actual test result and the 5th column means value test after adjusting SoC configuration

Using ds90ub941 patgen test result:

1. ds90ub941 internal timing(0x65: 0x0C)，dsi clock，display normally;
2. ds90ub941 external timing(0x65: 0x08)，dsi clock，display abnormally;

Display resolution requirement:



Could you please tell us how to configure the correct timing with I.mx 8 to 941AS then 941AS could output a qualified timing to DLPC230?