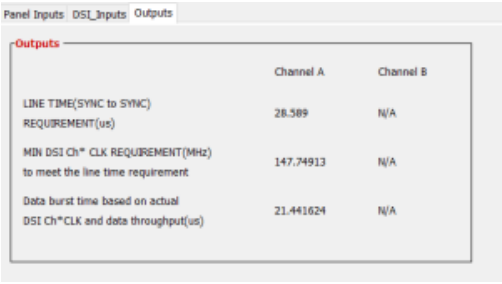
Link-Loss & Line-fault

Simulation of the link-loss and its impact on Display

We’re able to simulate the three Error Bits, the observations are captured below:

1. [BIT:3] CHA_LLP_ERR :

Simulation: By changing the display bridge register configuration using tuner tool. We're easily able to reproduce the error LLP error.



dmesg:

[1.964460] sn65dsi84: status reg init done.
[1.964960] sn65dsi84: SN65DSI84_CHA_ERR [0xE5] ->[0x0C]
[1.966710] [sn65dsi84_irq_handler]:
[1.980328] sn65dsi84: SN65DSI84_CHA_ERR [0xE5] [0x0C]

Observation: Display is blank

Recovery: We're making sure the correct display register configuration we're doing

At the bridge Init sequence. Still if the issues produce, we'll reconfigure the register and restart the chip.

Note:- This will be very rare case to reproduce the issues at run time. As, we're making sure all register configurations are correct.

2. [BIT:0] PLL_UNLOCK :

Simulation: We're disabling the internal source PLL by setting the register configuration 0x0D
(cmd: i2cset -f -y 10 0x2c 0x0d 0x01 b).

dmesg:

[57139.667847] [sn65dsi84_irq_handler]:
[57139.668164] [sn65dsi84_irq_handler]: ERROS STATUS REGISTER 0xE5 = 0x01

Observation: Display is blank

Recovery: Making sure the internal clock setting Is correct. If required re-configure the clock and enable the pll.

3. [BIT:2] CHA_SOT_BIT_ERR: This bit configured from tuner tool itself as SoT bit tolerated. So, this will not be taking any effect to display at run time. PHY itself will take care.

8.6.1.6.3 Register 0xE5

Figure 47. Register 0xE5

7	6	5	4	3	2	1
CHA_SYNCH_ERR	CHA_CRC_ERR	CHA_UNC_ECC_ERR	CHA_COR_ECC_ERR	CHA_LLP_ERR	CHA_SOT_BIT_ERR	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. Register 0xE5 Field Descriptions

Bit	Field	Type	Reset	Description
7	CHA_SYNCH_ERR	R/W	0	When the DSI channel A packet processor detec synchronization error, that is, an unexpected syn bit is set; this bit is cleared by writing a '1' value.
6	CHA_CRC_ERR	R/W	0	When the DSI channel A packet processor detec stream CRC error, this bit is set; this bit is cleare '1' value.
5	CHA_UNC_ECC_ERR	R/W	0	When the DSI channel A packet processor detec uncorrectable ECC error, this bit is set; this bit is writing a '1' value.
4	CHA_COR_ECC_ERR	R/W	0	When the DSI channel A packet processor detec ECC error, this bit is set; this bit is cleared by wri
3	CHA_LLP_ERR	R/W	0	When the DSI channel A packet processor detec protocol error, this bit is set; this bit is cleared by value. Low level protocol errors include SoT and EoT sy Escape Mode entry command errors, LP transmi errors, and false control errors. Lane merge error by this status condition.
2	CHA_SOT_BIT_ERR	R/W	0	When the DSI channel A packet processor detec leader sequence bit error, this bit is set; this bit is writing a '1' value.
1	Reserved	R		Reserved
0	PLL_UNLOCK	R/W	1	This bit is set whenever the PLL Lock status tran LOCK to UNLOCK.

Fig:1

Table 10. Register 0x10 Field Descriptions

Bit	Field	Type	Reset	Description
0	SOT_ERR_TOL_DIS	R/W	0	0 – Single bit errors are tolerated for the start of t leader sequence (default) 1 – No SoT bit errors are tolerated

Fig:2